GETTING STARTED GUIDE

PXIe-7899

PXIe, XC Network Controller, AO and DO Position Emulation

This document explains how to install, configure, and troubleshoot the PXIe-7899. It also includes installation instructions for the PXIe-7899 Socketed CLIP which you must install into LabVIEW before programming the PXIe-7899. Refer to *FPGA I/O Node Reference and Programming Notes* on page 13 for programming notes and a list of the FPGA I/O node signal names and descriptions.

Before you begin:

- Install and configure your chassis and controller. For detailed chassis and controller installation instructions, refer to the Getting Started Guide for your product, accessible by search at *ni.com/manuals*.
- Refer to the readme for PXIe-7899 API and Design Files to ensure that your development computer meets the minimum system requirements. To access, search for the readme by name at *ni.com/manuals*.

Contents

Unpacking the Kit

Notice To prevent electrostatic discharge (ESD) from damaging the module, ground yourself using a grounding strap or by holding a grounded object, such as your computer chassis.

1. Touch the antistatic package to a metal part of the computer chassis.
2. Remove the module from the package and inspect it for loose components or other signs of damage.

   Notice Never touch the exposed pins of connectors.

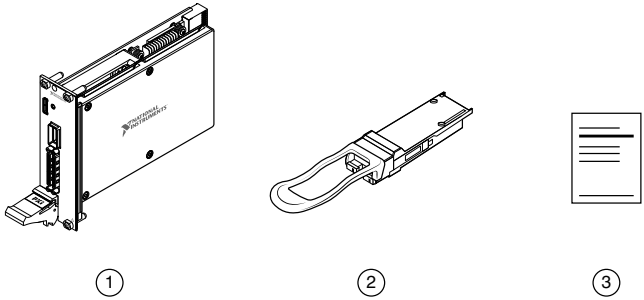
   Note Do not install a module if it appears damaged in any way.

3. Unpack any other items and documentation from the kit.

Store the module in the antistatic package when the module is not in use.

Verifying the Kit Contents

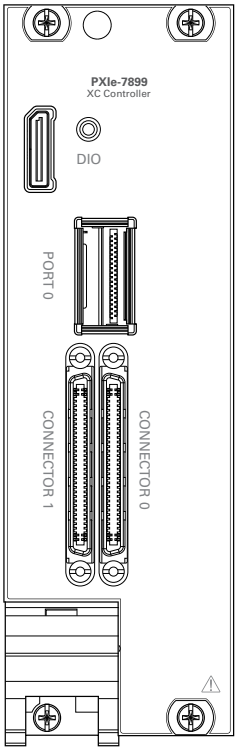
Figure 1. PXIe-7899 Kit Contents



1. PXIe-7899 Module
2. QSFP+ Optical Transceiver Module
3. PXIe-7899 Safety, Environmental, and Regulatory Information Document

Note A QSFP+ module must meet certain specifications to operate with the PXIe-7899. Do not attempt to replace the QSFP+ module included in this kit with a third-party QSFP+ module. Should a replacement QSFP+ module be necessary, contact the NI support team at *ni.com/support*.

PXIe-7899 Front Panel



Note Connector 0 and Connector 1 appear on the module in reverse of standard left-to-right numerical order.

Table 1. Front Panel Connector Descriptions and Functions

Connector	Description	Function
DIO	Nano-Pitch DIO connector	Multi-signal DIO connector that provides access to FPGA multi-gigabit transceivers (MGTs) and general-purpose LVCMOS signals
PORT 0	QSFP+ connector, SFF-8436 compliant	High-speed serial interfacing port

Table 1. Front Panel Connector Descriptions and Functions (Continued)

Connector	Description	Function
CONNECTOR 0	Dual stack 68 pin VHDCI receptacle	Mixed signal connector with analog input, analog output, and digital outputs
CONNECTOR 1		

Cable Recommendations

Table 2. Cable Recommendations and NI Part Numbers

Front Panel Connector	Cable	Description	NI Part Number
DIO	Nano-Pitch cable	Nano-Pitch Male to Nano-Pitch Male OCuLink x4 Cable	785486-01
PORT 0	MPO to 4 LC Breakout Cable	40GB MPO to 4x LC Duplex Breakout Fiber Patch Cable	755099-02
CONNECTOR 0 and CONNECTOR 1	NI SHC68-68-RMIO	RMIO Shielded Cable, 68 Pin D-Type to 68 pin VHDCI	189588-01 (1 m) 189588-02 (2 m)

Connector Pinouts

Figure 2. Digital I/O (DIO) Connector

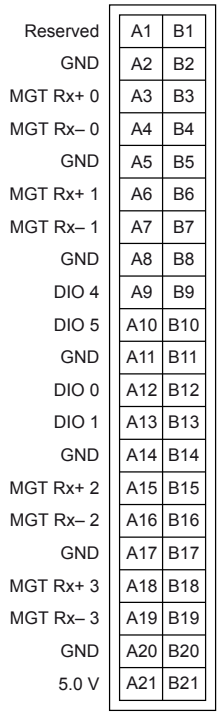


Table 3. Pin Descriptions for DIO Connector

Signal	Type	Direction
MGT Tx± <0..3>	Xilinx UltraScale GTH	Output
MGT Rx± <0..3>	Xilinx UltraScale GTH	Input
DIO <0..7>	Single-ended	Bidirectional
5.0 V	DC	Output
GND	Ground	—

Notice The maximum input signal levels are valid only when the module is powered on. To avoid permanent damage to the PXIe-7899, do not apply a signal to the device when the module is powered down.

Notice Connections that exceed any of the maximum ratings of any connector on the PXIe-7899 can damage the device and the system. NI is not liable for any damage resulting from such connections.

Figure 3. PORT 0 Connector

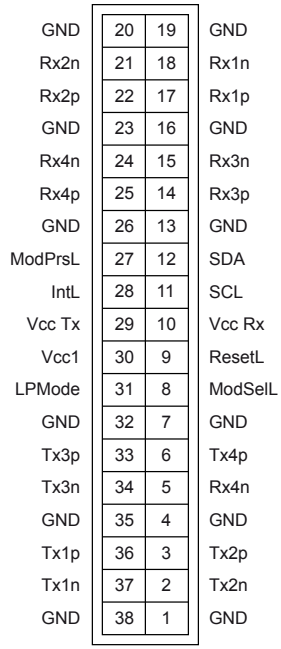


Table 4. Pin Descriptions for PORT 0 Connector

Symbol	Signal Name
Txn <1..4>	Transmitter Inverted Data Input
Txp <1..4>	Transmitter Non-Inverted Data Input
Rxn <1..4>	Receiver Inverted Data Output
Rxp <1..4>	Receiver Non-Inverted Data Output
SCL	2-Wire Serial Interface Clock
SDA	2-Wire Serial Interface Data
ModPrsL	Module Present
ModSelL	Module Select

Table 4. Pin Descriptions for PORT 0 Connector (Continued)

Symbol	Signal Name
ResetL	Module Reset
IntL	Interrupt
LPMode	Low Power Mode
Vcc Rx	+3.3 V Power Supply Receiver
Vcc Tx	+3.3 V Power Supply Transmitter
Vcc1	+3.3 V Power Supply
GND	Ground

Figure 4. CONNECTOR 0 and CONNECTOR 1

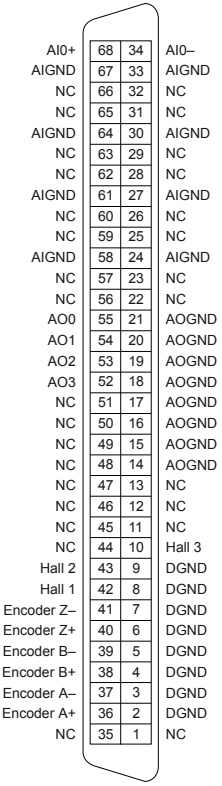


Table 5. Pin Descriptions for CONNECTOR 0 and CONNECTOR 1

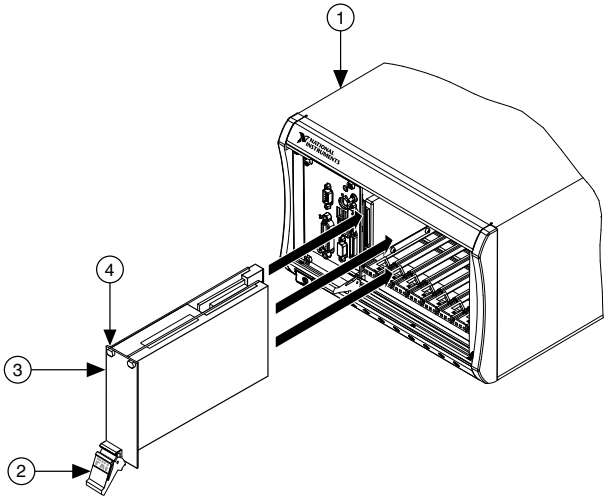
Symbol	Description	Signal Name in LabVIEW
AI0+	Positive analog input	Conn0 AI0, Conn1 AI0
AI0-	Negative analog input	Conn0 AI0, Conn1 AI0
AIGND	Ground reference for analog input	—
AO <0..3>	Analog output	Conn0<AO 0..3>, Conn1<AO 0..3>
AOGND	Ground reference for analog output	—
Hall <1..3>	Hall Effect sensor output	Conn0 Hall<1..3>, Conn1 Hall<1..3>
Encoder <A/B/Z>±	Quadrature Encoder output	Conn0 EncoderA/B/Z, Conn1 EncoderA/B/Z
DGND	Ground reference for the Hall Effect or Quadrature Encoder	—
NC	No connection	—

Installing the PXIe-7899

1. Ensure the AC power source is connected to the chassis before installing the module.

   The AC power cord grounds the chassis and protects it from electrical damage while you install the module.
2. Power off the chassis.
3. Inspect the slot pins on the chassis backplane for any bends or damage prior to installation. Do not install a module if the backplane is damaged.
4. Remove the black plastic covers from all the captive screws on the module front panel.
5. Identify the slots you will use in the chassis.
6. Touch any metal part of the chassis to discharge static electricity.
7. Place the module edges into the module guides at the top and bottom of the chassis. Slide the module into the slots until it is fully inserted.

Figure 5. PXIe-7899 Installation



1. PXI Express Chassis
2. Ejector Handle in Downward (Unlatched) Position
3. PXI Express Two-Slot Module
4. Captive Screw

8. Secure the module front panel to the chassis using the front-panel mounting screws.

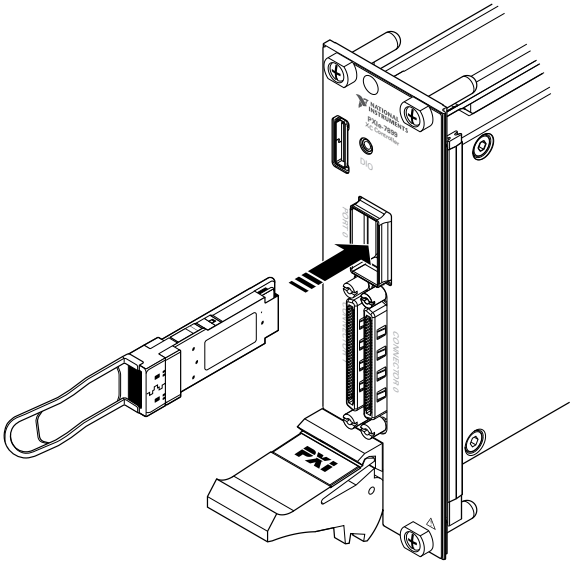
Note Tightening the top and bottom mounting screws increases mechanical stability and also electrically connects the front panel to the chassis, which can improve the signal quality and electromagnetic performance.

9. Cover all empty slots using EMC filler panels or fill using slot blockers to maximize cooling air flow, depending on your application.
10. Leave the chassis powered off until you have installed the QSFP+ module.

Installing the Hot Pluggable QSFP+ Module

1. Hold the QSFP+ module with the pull-tab facing the left.
2. Remove the protective cover from the opposite end of the pull-tab. Leave the dust plug inserted in the pull-tab end.

Figure 6. QSFP+ Module Install



3. With the pull-tab facing the left, align the QSFP+ module with the socket opening at PORT 0 on the PXIe-7899. Carefully slide the QSFP+ module into PORT 0.
4. Use your thumb to press firmly on the QSFP+ module until it fully seats into PORT 0.

Note The QSFP+ module must be fully seated in PORT 0 for the PXIe-7899 to detect a connection. To test the QSFP+ module presence at PORT 0, refer to *What Should I Do if the PXIe-7899 Cannot Communicate with XC Devices?* on page 13.

5. Power on the chassis.

To protect the QSFP+ module from dust and debris, NI recommends leaving the dust plug inserted in the pull-tab end of the module until you are ready to connect a cable.

Installing the Software

Download the following software from *ni.com/downloads*.

Note NI software includes NI Package Manager to handle the installation. Refer to the NI Package Manager Manual at *ni.com/r/nipmmanual* for more information about installing, removing, and upgrading NI software using NI Package Manager.

- LabVIEW
- LabVIEW FPGA Module

- PXIe-7899 API and Design Files
- (Optional) LabVIEW FPGA Compilation Tool for Vivado

Note Install LabVIEW FPGA Compilation Tool for Vivado if you want to use the local compile server to compile a LabVIEW FPGA bitfile.

Configuring the PXIe-7899 in MAX

Use Measurement & Automation Explorer (MAX) to configure your NI hardware. MAX informs other programs about which NI hardware products are in the system and how they are configured. MAX is automatically installed with the FlexRIO driver.

1. Launch MAX.
2. In the configuration tree, expand **Devices and Interfaces** to see the list of installed NI hardware.

   Installed modules appear under the name of their associated chassis.
3. Expand your **Chassis** tree item.

   MAX lists all modules installed in the chassis. Your default names may vary.
4. Record the identifier MAX assigns to the hardware. Use this identifier when programming the PXIe-7899.

   Note Depending on your software version and operating system, MAX may misidentify the PXIe-7899 as the PXIe-7985. If you notice this error in MAX, record the chassis and slot location of the PXIe-7899 to use as identifiers.

   Note If you do not see your module listed, press <F5> to refresh the list of installed modules. If the module is still not listed, power off the system, ensure the module is correctly installed, and restart.
5. Self-test the hardware by selecting the item in the configuration tree and clicking **Self-Test** in the MAX toolbar.

   The MAX self-test performs a basic verification of hardware resources.

Adding the Socketed CLIP to a New LabVIEW Project

Before you begin, ensure that you have installed your hardware into the chassis and completed the steps in *Installing the Software* on page 10.

1. Open LabVIEW and select **File** »**Create Project.**
2. In the **Create Project** dialog box, select **Blank Project** and click **Finish**.
3. In the **Project Explorer** window, right-click `My Computer` and select **New** »**Targets and Devices.**
4. In the **Add Targets and Devices on My Computer** dialog box, select the **Existing target or device** and **Discover an existing target(s) or device(s)** option buttons.

5. Expand the `FPGA Target` folder, then expand the `FlexRIO FPGA Modules` folder and wait for LabVIEW to detect the module.

   Note LabVIEW recognizes the PXIe-7899 as the PXIe-7985. Once detected, the PXIe-7899 FPGA module name appears in the format: `PXI(X)Slot(Y) (PXIe-7985)`. You must identify the PXIe-7899 by the chassis location `(X)` and slot location `(Y)` where you installed the module.

6. Click the `PXI(X)Slot(Y) (PXIe-7985)` option that corresponds to the chassis and slot location of the PXIe-7899 in your hardware setup, then click **OK**.
7. In the **Project Explorer** window, expand the `PXI(X)Slot(Y) (PXIe-7985)` item tree.
8. Right-click the **IO Socket** item and select **Properties** from the menu.
9. In the **IO Socket Properties** dialog box, choose **General** from the Category listbox, then select the **Enable IO Socket** checkbox.
10. From the **IO Configuration** listbox, choose **NI 7899**. Then, from the **Component Level IP** listbox, choose **NI 7899 CLIP**. Click **OK**.
11. In the **Project Explorer** window, confirm that the `IO Socket` item name now reads `IO Socket (NI 7899: NI 7899 CLIP)`.

Troubleshooting

If an issue persists after you complete a troubleshooting procedure, contact NI technical support or visit *ni.com/support*.

What Should I Do if the PXIe-7899 Does Not Appear in MAX?

1. In the MAX configuration tree, expand **Devices and Interfaces**.
2. Expand the **Chassis** tree to see the list of installed hardware, and press <F5> to refresh the list.

   Note Depending on your software version and operating system, MAX may misidentify the PXIe-7899 as the PXIe-7985. If you notice this error in MAX, you must identify the PXIe-7899 in MAX by slot location. The PXIe-7899 will appear in MAX as the PXIe-7985 located in the chassis slots where the PXIe-7899 module is installed.

3. If the module is still not listed, power off the system, ensure that all hardware is correctly installed, and restart the system.
4. Navigate to the Device Manager.

Operating System	Description
Windows 10/8.1	Right-click the **Start** button and select **Device Manager**.
Windows 7	Select **Start»Control Panel»Device Manager**.

5. Under an NI entry, confirm that a PXIe-7899 entry appears in the Device Manager.

6. If you are using a PC with a device for PXI remote control system, under **System Devices**, confirm that no error conditions appear for the **PCI-to-PCI Bridge**.

   If error conditions appear, reinstall FlexRIO.

What Should I Do if the PXIe-7899 Fails the Self-Test?

1. Restart the system.
2. Launch MAX, and perform the self-test again.
3. Power off the chassis.
4. Reinstall the failed module in a different slot.
5. Power on the chassis.
6. Perform the self-test again.

What Should I Do if the PXIe-7899 Cannot Communicate with XC Devices?

Confirm that the PXIe-7899 detects a connection to the QSFP+ module installed at PORT 0.

1. In LabVIEW, right-click the block diagram and select **NI 7899 User API** »**Diagnose QSFP.vi** .
2. Double click the **Diagnose QSFP** VI to view the front panel.
3. In the **resource name** field, click the arrow button to browse target devices.
4. In the **Browse RIO Devices** window, select the PXIe-7899 as it is identified in NI Measurement and Automation Explorer.
5. In the **LvFPGA bitfile path** field, click the folder icon to browse for a compiled LabVIEW FPGA bitfile.
6. Select a compiled LabVIEW FPGA bitfile from your machine.

   Note For detailed instructions on compiling LabVIEW FPGA bitfiles, refer to the *LabVIEW FPGA Module Help* available from the Start menu on your development machine or at *ni.com/manuals*.

7. On the block diagram, click **Run**. If the **QSFP module present** indicator does not turn on, ensure the QSFP+ module is fully seated in PORT 0.

FPGA I/O Node Reference and Programming Notes

Notice When programming XC communication, always plug a cable into Lane 0 before you plug into Lane 1, 2, or 3. Lanes 1, 2, and 3 depend on Lane 0 to

communicate, and the use of Lane 1, 2, or 3 without Lane 0 may result in data corruption.

Tip Use the `Lane x Error` signal listed below to monitor for communication errors in the connections at Lanes 0, 1, 2, and 3.

Note

- You must choose calibrated analog input and analog output or raw analog input and analog output; they cannot be used simultaneously.
- You must choose the Quadrature Encoder digital output or the Hall Effect digital output; they cannot be used simultaneously.

Table 6. FPGA I/O Node Signal Names and Descriptions

Signal Name	Data Type	Direction	Clock Domain	Signal Description
`Motor Clock 100 MHz`	N/A	From Socketed CLIP	100 MHz	100 MHz motor clock signal derived from PXIe 100 MHz clock for analog input, analog output, quadrature encoder digital output and Hall effect digital output.
`Conn x AI y Ready`	Boolean	From Socketed CLIP	Motor Clock	This signal must indicate ready high before you assert `Conn x AI y Start`.
`Conn x AI y Start`	Boolean	To Socketed CLIP	Motor Clock	Assert high for one clock cycle to start analog input data conversion.
`Conn x AI y Valid`	Boolean	From Socketed CLIP	Motor Clock	Assert high for one clock cycle to read new analog input data.
`Conn x AI y Data`	FXP	From Socketed CLIP	Motor Clock	Returns a fixed-point data range <-10..+10>.
`Conn x Raw AI y Ready`	Boolean	From Socketed CLIP	Motor Clock	This signal must indicate ready high before you assert `Conn x Raw AI y Start`.

Table 6. FPGA I/O Node Signal Names and Descriptions (Continued)

Signal Name	Data Type	Direction	Clock Domain	Signal Description
`Conn x Raw AI y Start`	Boolean	To Socketed CLIP	Motor Clock	Assert high for one clock cycle to start raw analog input data conversion.
`Conn x Raw AI y Valid`	Boolean	From Socketed CLIP	Motor Clock	Assert high for one clock cycle to read new analog input data.
`Conn x Raw AI y Data`	I 16	From Socketed CLIP	Motor Clock	Two's complement I16 raw data for analog input.
`Conn x AO y Ready`	Boolean	From Socketed CLIP	Motor Clock	This signal must indicate ready high before you assert `Conn x AO y Valid`.
`Conn x AO y Valid`	Boolean	To Socketed CLIP	Motor Clock	Assert high for one clock cycle to write new analog output data.
`Conn x AO y Data`	FXP	To Socketed CLIP	Motor Clock	Sends a fixed-point data range <-10..+10> to analog output.
`Conn x Raw AO y Ready`	Boolean	From Socketed CLIP	Motor Clock	This signal must indicate ready high before you assert `Conn x Raw AO y Valid .`
`Conn x Raw AO y Valid`	Boolean	To Socketed CLIP	Motor Clock	Assert high for one clock cycle to write new analog output raw data.
`Conn x Raw AO y Data`	I 16	To Socketed CLIP	Motor Clock	Two's complement I 16 raw data for analog output.
`Conn x Encoder Ready`	Boolean	From Socketed CLIP	Motor Clock	This signal must indicate ready high before you assert `Conn x Encoder Valid .`

Table 6. FPGA I/O Node Signal Names and Descriptions (Continued)

Signal Name	Data Type	Direction	Clock Domain	Signal Description
Conn *x* Encoder Valid	Boolean	To Socketed CLIP	Motor Clock	Assert high for one clock cycle to write new quadrature encoder data.
Conn *x* Encoder *A/B/Z*	Boolean	To Socketed CLIP	Motor Clock	Writes boolean data for quadrature encoder. You must update *A/B/Z* encoder data when asserting this signal.
Conn *x* Hall Ready	Boolean	From Socketed CLIP	Motor Clock	This signal must indicate ready high before you assert Conn *x* Hall Valid .
Conn *x* Hall Valid	Boolean	To Socketed CLIP	Motor Clock	Assert high for one clock cycle to write new Hall effect data.
Conn *x* Hall *1/2/3*	Boolean	To Socketed CLIP	Motor Clock	Writes boolean data for Hall effect. You must update *1/2/3* Hall data when asserting this signal.
Conn *x* AI *y* LSB Weight	I 32	From Socketed CLIP	Motor Clock	Returns I 32 data for the calibration LSB weight.
Conn *x* AI *y* Offset	I 32	From Socketed CLIP	Motor Clock	Returns I 32 data for the calibration offset.
Conn *x* AO *y* LSB Weight	I 32	From Socketed CLIP	Motor Clock	Returns I 32 data for the calibration LSB weight.
Conn *x* AO *y* Offset	I 32	From Socketed CLIP	Motor Clock	Returns I 32 data for the calibration offset.
IO Ready	Boolean	From Socketed CLIP	N/A	Indicates successful configuration of the I/O module using the default configuration.

Table 6. FPGA I/O Node Signal Names and Descriptions (Continued)

Signal Name	Data Type	Direction	Clock Domain	Signal Description
`IO Error`	I 32	From Socketed CLIP	N/A	Returns I/O module errors.
`XC Clock 62.5 MHz`	N/A	From Socketed CLIP	XC Clock	62.5 MHz derived from I/O module 125 MHz oscillator for XC communication.
`Lane x Clear Error`	Boolean	To Socketed CLIP	XC Clock	Assert on one clock cycle to clear the `Lane x Error`.
`Lane x Ready`	Boolean	From Socketed CLIP	XC Clock	`Lane x Ready` high indicates that an Aurora connection is established on this lane, and the lane is ready to transfer XC data.
`Lane x Error`	I 32	From Socketed CLIP	XC Clock	Returns error code from data communication. Bit 0: Aurora Hard Error Bit 1: Aurora Soft Error Bit 2: Aurora Frame Error Bit 3: Reserved (0) Bit 4: Tx FIFO Overflow Error Bit 5: Tx FIFO Underflow Error Bit 6: Rx FIFO Overflow Error Bit 7: Rx FIFO Underflow Error Bit [31:8]: Reserved (0)

Table 6. FPGA I/O Node Signal Names and Descriptions (Continued)

Signal Name	Data Type	Direction	Clock Domain	Signal Description
`Lane x POF y Tx Index`	U 32	To Socketed CLIP	XC Clock	Writes Tx Index from XC stream. Bit 0: POF index valid Bit 1: Reserved (0) Bit [31:2]: POF index [31:2]
`Lane x POF y Tx Data`	U 8	To Socketed CLIP	XC Clock	Writes Tx Data from XC stream. Bit [3:0]: POF data Bit 4: POF data valid Bit 5: POF is null Bit [7:6]: Reserved (0)
`Lane x POF y Rx Index`	U 32	From Socketed CLIP	XC Clock	Returns Rx Index from XC stream. Bit 0: POF index valid Bit 1: Reserved (0) Bit [31:2]: POF index [31:2]
`Lane x POF y Rx Data`	U 8	From Socketed CLIP	XC Clock	Returns Rx Data from XC stream. Bit [3:0]: POF data Bit 4: POF data valid Bit 5: POF is null Bit [7:6]: Reserved (0)

Where to Go Next

For detailed information on programming FPGAs, including compiling, downloading, and running FPGA VIs, refer to the *LabVIEW FPGA Module Help*. Access the help on your development machine at **Start** »**National Instruments** or search for the help by name at *ni.com/manuals*.

NI Services

Visit *ni.com/support* to find support resources including documentation, downloads, and troubleshooting and application development self-help such as tutorials and examples.

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