SPECIFICATIONS

PXIe-5172

PXIe, 100 MHz, 4- or 8-channel, 14-bit, Kintex-7 325T or 410T FPGA Reconfigurable PXI Oscilloscope

These specifications apply to the PXIe-5172 with 4 channels and the PXIe-5172 with 8 channels.

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Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty. Warranted specifications account for measurement uncertainties, temperature drift, and aging. Warranted specifications are ensured by design or verified during production and calibration.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.
- *Measured* specifications describe the measured performance of a representative model.

Specifications are *Nominal* unless otherwise noted.

Conditions

Specifications are valid under the following conditions unless otherwise noted.

- All vertical ranges
- All bandwidths and bandwidth limiting filters
- Sample rate set to 250 MS/s

- Onboard sample clock locked to onboard reference clock
- PXIe-5172 module warmed up for 15 minutes at ambient temperature.[1]
- Calibration IP used properly when using LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes (instrument design libraries) to create FPGA bitfiles. Refer to the *NI Reconfigurable Oscilloscopes Help* for more information about the calibration API.

Warranted specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 45 °C
- Chassis configured:[2]
  - PXI Express chassis fan speed set to HIGH
  - Foam fan filters removed if present
  - Empty slots contain PXI chassis slot blockers and filler panels
- External calibration cycle maintained
- External calibration performed at 23 °C ±3 °C

Typical specifications are valid under the following conditions unless otherwise noted.

- Ambient temperature range of 0 °C to 45 °C

Nominal and Measured specifications are valid under the following conditions unless otherwise noted.

- Room temperature, approximately 23 °C

Vertical

Analog Input

Number of channels	
PXIe-5172 (4 CH)	Four (simultaneously sampled)
PXIe-5172 (8 CH)	Eight (simultaneously sampled)
Input type	Referenced single-ended
Connectors	SMB, ground referenced

[1] Warm-up begins after the chassis and controller or PC is powered, the PXIe-5172 is recognized by the host, and the PXIe-5172 is configured using the instrument design libraries or NI-SCOPE. In some RIO applications, the power consumed by the PXIe-5172 can be significantly higher than the default image for the module. In these cases, you can improve performance by loading your image and configuring the device before warm-up time begins. Self-calibration is recommended following the specified warm-up time.

[2] For more information about cooling, refer to the *Maintain Forced-Air Cooling Note to Users* available at *ni.com/manuals*.

Impedance and Coupling

Input impedance	50 Ω ±1.5%, typical 1 MΩ ±0.5%, typical
Input capacitance (1 MΩ)	16 pF ±1.2 pF, typical
Input coupling	AC DC

Figure 1. 50 Ω Voltage Standing Wave Ratio (VSWR), Measured

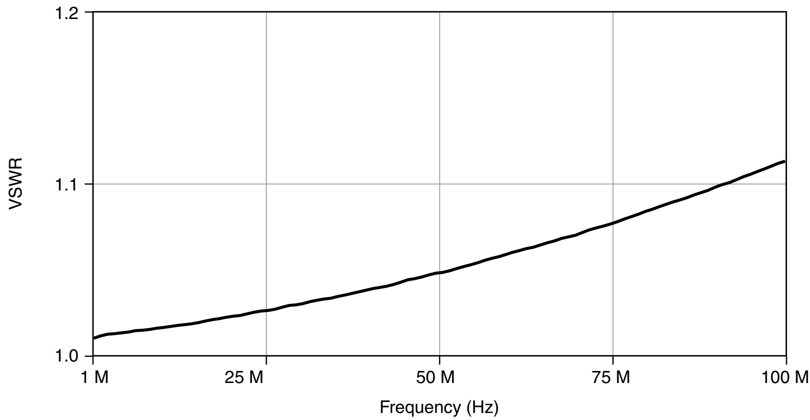
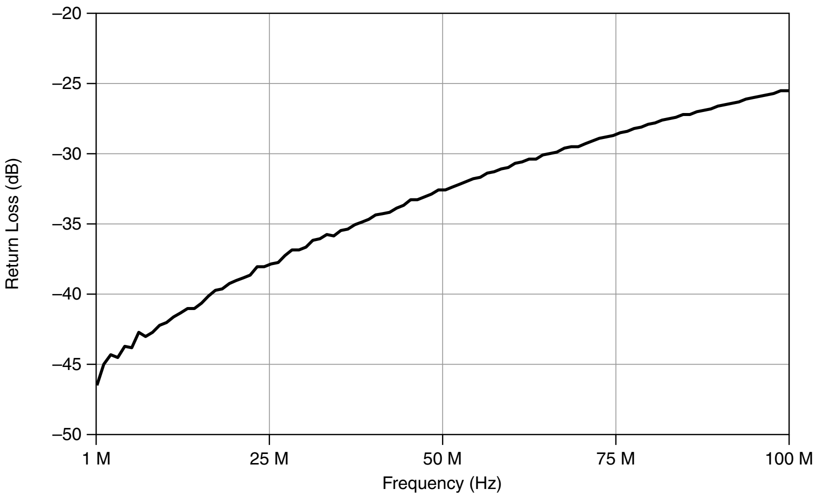


Figure 2. 50 Ω Input Return Loss, Measured



Voltage Levels

Table 1. 50 Ω FS Input Range and Vertical Offset Range

Input Range ($V_{pk\text{-}pk}$)	Vertical Offset Range (V)
0.2 V	±0.5
0.7 V	±0.5
1.4 V	±0.5
5 V	±2.5
10 V[3]	0

Table 2. 1 MΩ FS Input Range and Vertical Offset Range

Input Range ($V_{pk\text{-}pk}$)	Vertical Offset Range (V)
0.2 V	±0.5
0.7 V	±0.5
1.4 V	±0.5
5 V	±4.5
10 V	±4.5
40 V	±20
80 V	0

Maximum input overload	
50 Ω	7 V RMS with |Peaks| ≤10 V
1 MΩ	|Peaks| ≤42 V

Notice Signals exceeding the maximum input overload may cause damage to the device.

[3] Derated to 5 $V_{pk\text{-}pk}$ for periodic waveforms with frequencies below 100 kHz.

Accuracy

Resolution	14 bits
DC accuracy[4]	
50 Ω	±[(0.45% × |*Reading* - *Vertical Offset*|) + (0.4% × |*Vertical Offset*|) + (0.05% of FS) + 0.4 mV], warranted
1 MΩ, 40 V_{pk-pk} range	±[(0.45% × |*Reading* - *Vertical Offset*|) + (0.5% × |*Vertical Offset*|) + (0.05% of FS) + 0.4 mV], warranted
1 MΩ, all other ranges	±[(0.45% × |*Reading* - *Vertical Offset*|) + (0.4% × |*Vertical Offset*|) + (0.05% of FS) + 0.4 mV], warranted
DC drift[5]	±[(0.010% × |*Reading* - *Vertical Offset*|) + (0.003% × |*Vertical Offset*|) + (0.006% of FS)] per °C
AC amplitude accuracy[4]	
50 Ω	±0.15 dB at 50 kHz, warranted
1 MΩ, 40 V_{pk-pk} and 80 V_{pk-pk} ranges	±0.25 dB at 50 kHz, warranted
1 MΩ, all other ranges	±0.15 dB at 50 kHz, warranted
Conversion error rate[6]	
250 MS/sec	$<1 \times 10^{-10}$
200 MS/sec	$<1 \times 10^{-15}$
150 MS/sec	$<1 \times 10^{-20}$

4 Within ± 5 °C of self-calibration temperature. Accuracy is warranted only when using DC input coupling.

5 Used to calculate errors when onboard temperature changes more than ±5 °C from the self-calibration temperature.

6 A *conversion error* is defined as deviation greater than 0.6% of full scale.

Table 3. Crosstalk[7]

Frequency	Level		
	50 Ω	1 MΩ, 0.2 $V_{pk\text{-}pk}$ to 10 $V_{pk\text{-}pk}$ Range	1 MΩ, 40 $V_{pk\text{-}pk}$ Range
1 MHz	-75 dB	-75 dB	-65 dB
50 MHz	-75 dB	-75 dB	
100 MHz	-70 dB	-70 dB	

Notice This device may experience increased peak to peak noise when connected cables are routed in an environment with radiated or conducted electromagnetic interference. To limit the effects of this interference and to ensure that this device functions within specifications, take precautions when designing, selecting, and installing measurement probes and cables.

Bandwidth and Transient Response

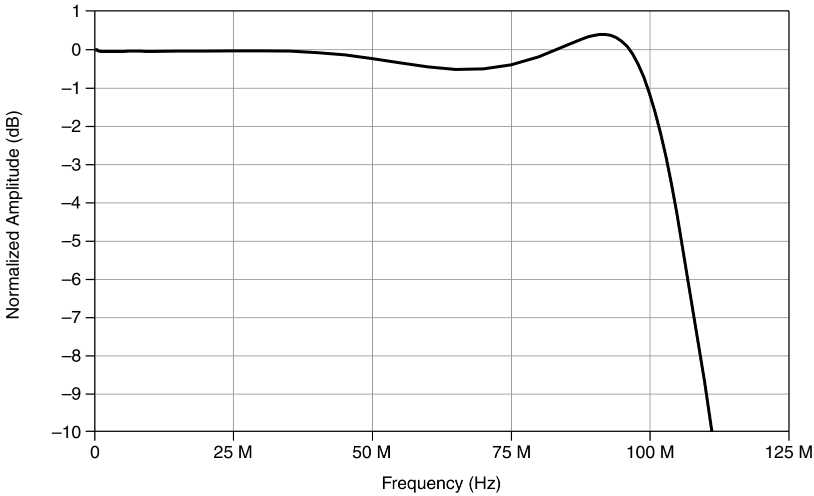
Table 4. Bandwidth (-3 dB), Warranted[8]

Input Impedance	Input Range ($V_{pk\text{-}pk}$)	Bandwidth
50 Ω	0.2 V	99 MHz
	All other input ranges	100 MHz
1 MΩ[9]	All input ranges	98 MHz

Bandwidth-limiting filters[8,10]	20 MHz noise filter
AC-coupling cutoff (-3 dB)[11]	16.50 Hz
Rise/fall time[12]	
50 Ω	5.15 ns
1 MΩ	5.25 ns

7 Measured on one channel with test signal applied to another channel, with the same range setting on both channels.
8 Normalized to 50 kHz.
9 Verified using a 50 Ω source and 50 Ω feedthrough terminator.
10 Only available using NI-SCOPE.
11 Verified using a 50 Ω source.
12 50% FS input pulse.

Figure 3. 50 Ω Full Bandwidth Frequency Response, 1.4 V_{pk-pk}, Measured



Spectral Characteristics[13]

Table 5. Spurious-Free Dynamic Range (SFDR), 50 Ω and 1 MΩ[14]

Input Range (V_{pk-pk})	Full Bandwidth, Input Frequency ≤30 MHz
0.2 V	-70 dBc
0.7 V	-78 dBc
1.4 V	-71 dBc
5 V	-80 dBc

Table 6. Total Harmonic Distortion (THD), 50 Ω and 1 MΩ[15]

Input Range (V_{pk-pk})	Full Bandwidth, Input Frequency ≤30 MHz
0.2 V	-74 dBc
0.7 V	-77 dBc

13 For 1 MΩ, verified using a 50 Ω source and 50 Ω feedthrough terminator.
14 -1 dBFS input signal corrected to FS. 358 Hz resolution bandwidth.
15 -1 dBFS input signal corrected to FS. Includes the 2nd through the 5th harmonics.

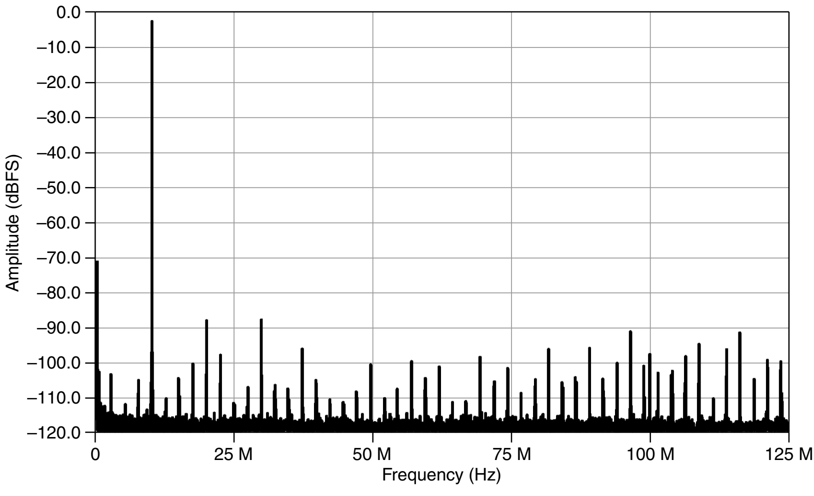
Table 6. Total Harmonic Distortion (THD), 50 Ω and 1 MΩ[15] (Continued)

Input Range (V_{pk-pk})	Full Bandwidth, Input Frequency ≤30 MHz
1.4 V	-70 dBc
5 V	-77 dBc

Table 7. Effective Number of Bits (ENOB), 50 Ω and 1 MΩ[14]

Input Range (V_{pk-pk})	20 MHz Filter Enabled, Input Frequency ≤10 MHz	Full Bandwidth, Input Frequency >10 MHz, ≤30 MHz
0.2 V	9.8	9.5
0.7 V	11.4	10.8
1.4 V	11.9	10.8
5 V	11.8	11.0

Figure 4. 50 Ω Single-Tone Spectrum, 1.4 V_{pk-pk} Input Range, Full Bandwidth, 9.9 MHz Input Tone at -1 dBFS, Measured



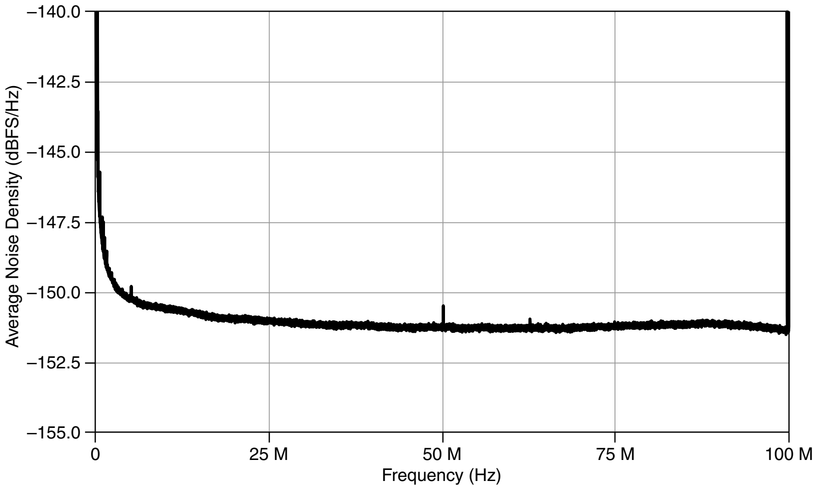
15 -1 dBFS input signal corrected to FS. Includes the 2nd through the 5th harmonics.

Noise[16]

Table 8. RMS Noise, 50 Ω and 1 MΩ, Warranted

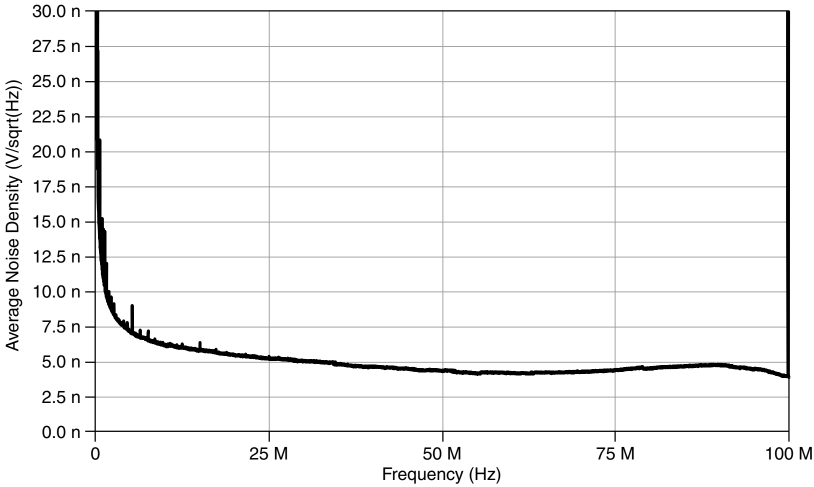
Input Range ($V_{pk\text{-}pk}$)	RMS Noise (% of Full Scale)
0.2 V	0.045
All other input ranges	0.018

Figure 5. 50 Ω Average Noise Density, 1.4 $V_{pk\text{-}pk}$ Range, Measured



[16] Verified using a 50 Ω terminator connected to input.

Figure 6. 50 Ω Average Noise Density, 0.2 $V_{pk\text{-}pk}$ Range, Measured



Skew

Channel-to-channel skew[17]	<120 ps

Horizontal

Sample Clock

Sources	
Internal	Onboard clock (internal VCXO)
External	AUX 0 CLK IN (front panel MHDMR connector) PXIe_DStarA (backplane connector)
Sample rate range, real-time[18]	3.815 kS/s to 250 MS/s
Sample clock jitter[19]	700 fs RMS

[17] For input frequencies <90 MHz.

[18] Divide by *n* decimation from 250 MS/s. For more information about the sample clock and decimation, refer to the *NI Reconfigurable Oscilloscopes Help* at ni.com/manuals.

[19] Integrated from 100 Hz to 10 MHz. Includes the effects of the converter aperture uncertainty and the clock circuitry jitter.

Timebase frequency	
Internal	250 MHz
External	150 MHz to 250 MHz
Timebase accuracy	
Phase-locked to onboard clock	±25 ppm, warranted
Phase-locked to external clock	Equal to the external clock accuracy
DC accuracy sampling drift, ±(% of |*Reading*|) per MHz from 250 MHz[20]	±0.0127
Duty cycle tolerance	45% to 55%

Phase-Locked Loop (PLL) Reference Clock

Sources	
Internal	None (internal VCXO) Onboard clock (internal VCXO) PXI_Clk10 (backplane connector)
External (10 MHz)[21]	AUX 0 CLK IN (front panel MHDMR connector)
Duty cycle tolerance	45% to 55%

External Sample Clock

Source	AUX 0 CLK IN (front panel MHDMR connector)
Impedance	50 Ω
Coupling	AC
Input voltage range	
As a 250 MHz sine wave	1 dBm through 18 dBm
As a fast slew rate input (square wave, $V_{pk\text{-}pk}$)	0.4 V to 5 V
Maximum input overload	
As a 250 MHz sine wave	20 dBm
As a fast slew rate input (square wave, $V_{pk\text{-}pk}$)	6 V

20 Used to calculate additional DC accuracy error when using an external sample clock that is less than 250 MHz. To calculate the additional error, take the difference of the external sample clock rate from 250 MHz, divide by 1,000,000, and multiply by the DC accuracy sampling drift.

21 The PLL reference clock must be accurate to ±25 ppm.

External Reference Clock In

Source	AUX 0 CLK IN (front panel MHDMR connector)
Impedance	50 Ω
Coupling	AC
Frequency[22]	10 MHz
Input voltage range	
As a 250 MHz sine wave	1 dBm through 18 dBm
As a fast slew rate input (square wave, $V_{pk\text{-}pk}$)	6 V
Duty cycle tolerance	45% to 55%

Reference Clock Out

Source	PXI_Clk10 (backplane connector)
Destination	AUX 0 CLK OUT
Output impedance	50 Ω
Logic type	3.3 V LVCMOS
Maximum current drive	±8 mA

PXIe_DStarA

Source	System timing slot
Destinations	Onboard clock (internal VCXO) FPGA

PXI_Clk10

Source	PXI backplane
Destination	Reference clock

PXI_Clk100

Source	PXI backplane
Destination	FPGA

[22] The PLL reference clock must be accurate to ±25 ppm.

Trigger[23]

Supported triggers	Reference (stop) trigger Reference (arm) trigger Start trigger Advance trigger
Trigger types	Edge Hysteresis Window Digital Immediate Software
Dead time	*Sample clock period* × 10
Holdoff	From *Dead time* to [(2^{64} - 1) × *Sample clock period*]
Delay	From 0 to [(2^{51} - 1) × *Sample clock period*]

Analog Trigger

Sources	
PXIe-5172 (4 CH)	CH <0..3>
PXIe-5172 (8 CH)	CH <0..7>

Table 9. Analog Trigger Time Resolution and Rearm Time

Interpolator Status	Time Resolution	Rearm Time
Enabled	*Sample clock period* / 1024	*Sample clock period* × 124
Disabled	Sample clock period	*Sample clock period* × 84

Trigger accuracy[24]	
Input range (V_{pk-pk}): 0.2 V	0.75% of FS
Input range (V_{pk-pk}): 0.7 V, 1.4 V, 5 V	0.5% of FS

23 Refer to the *NI Reconfigurable Oscilloscopes Help* for information on supported data triggers. Specifications apply when Data Trigger IP is used properly when using instrument design libraries to create FPGA bitfiles.

24 For input frequencies <90 MHz.

Trigger jitter[24]	15 ps RMS
Minimum threshold duration[25]	Sample clock period

Digital Trigger

Sources	AUX 0 PFI <0..7> PXI_Trig <0..6>
Time resolution	*Sample clock period* × 2
Rearm time	*Sample clock period* × 84

Software Trigger

Destinations	Reference (stop) trigger Reference (arm) trigger Start trigger Advance trigger
Time resolution	*Sample clock period* × 2
Rearm time	*Sample clock period* × 84

Programmable Function Interface

Connector	AUX 0 PFI <0..7> (front panel MHDMR connector)
Direction	Bidirectional per channel
Direction control latency	125 ns
As an input (trigger)	
Destinations	FPGA diagram Start trigger (acquisition arm) Reference (stop) trigger Arm Reference trigger Advance trigger
Input impedance	49.9 kΩ
V_{IH}	2 V
V_{IL}	0.8 V
Maximum input overload	0 V to 3.3 V (5 V tolerant)
Minimum pulse width	10 ns

[25] Data must exceed each corresponding trigger threshold for at least the minimum duration to ensure analog triggering.

As an output (event)	
Sources	FPGA diagram Ready for Start Start trigger (acquisition arm) Ready for Reference Reference (stop) trigger End of Record Ready for Advance Advance trigger Done (End of Acquisition)
Output impedance	50 Ω
Logic type	3.3 V CMOS
Maximum current drive	12 mA
Minimum pulse width	10 ns

Power Output (+3.3 V)

Connector	AUX 0 +3.3 V (front panel MHDMR connector)
Voltage output	3.3 V ±10%
Maximum current drive	200 mA
Output impedance	<1 Ω

Waveform

Onboard memory size[26]	
PXIe-5172 (4 CH)	0.75 GB
PXIe-5172 (8 CH)	1.5 GB
Minimum record length	1 sample
Number of pretrigger samples	Zero up to (*Record length* - 1)
Number of posttrigger samples	Zero up to *Record length*
Maximum number of records in onboard memory	*Total onboard memory* / 48 × *Number of channels*, where *number of channels* is the number of channels enabled rounded up to the nearest power of two

[26] Onboard memory is shared among all enabled channels.

Figure 7. Allocated Onboard Memory Per Record

$$\text{Roundup}\left(\text{Roundup}\left(\frac{\mathit{Coerced\ number\ of\ samples} + \mathit{Number\ of\ samples\ per\ sample\ word}}{\mathit{Number\ of\ samples\ per\ memory\ word}}\right) \times \mathit{Number\ of\ samples\ per\ memory\ word} + 3 \times \mathit{Number\ of\ samples\ per\ memory\ word}\right) \times \mathit{Bytes\ per\ sample} \times \mathit{Number\ of\ channels}$$

where

Number of samples per sample word = 16 samples / *number of channels*

Number of samples per memory word = 48 samples / *number of channels*

Coerced number of samples is the number of pretrigger samples rounded up to the next multiple of *Number of samples per sample word* + the number of posttrigger samples rounded up to the next multiple of *number of samples per sample word*

Number of channels is the number of channels enabled rounded up to the nearest power of two

Memory Sanitization

For information about memory sanitization, refer to the letter of volatility for your device, which is available at *ni.com/manuals*.

FPGA

FPGA support

PXIe-5172 (4 CH)	Xilinx Kintex-7 XC7K325T FPGA
PXIe-5172 (8 CH)	Xilinx Kintex-7 XC7K325T FPGA Xilinx Kintex-7 XC7K410T FPGA

Table 10. FPGA Resources

Resource Type	Xilinx Kintex-7 XC7K325T	Xilinx Kintex-7 XC7K410T
Slice registers	407,600	508,400
Slice look-up tables (LUT)	203,800	254,200
DSPs	840	1,540
18 Kb block RAMs	890	1,590

Note Some of these FPGA resources are consumed by the logic necessary to operate the device and integrate with software and are thus out of the control of users.

Calibration

External Calibration

External calibration yields the following benefits:

- Corrects for gain and offset errors of the onboard references used in self-calibration.
- Adjusts timebase accuracy.
- Compensates the 1 MΩ ranges.

All calibration constants are stored in nonvolatile memory.

Self-Calibration

Self-calibration is done on software command. The calibration corrects for the following aspects:

- Gain
- Offset
- Intermodule synchronization errors

Refer to the *NI High-Speed Digitizers Help* for information about when to self-calibrate the device.

Calibration Specifications

Interval for external calibration	2 years
Warm-up time[27]	15 minutes

Software

Driver Software

This device was first supported in NI-SCOPE 17.1 and LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes 17.1. LabVIEW Instrument Design Libraries for Reconfigurable Oscilloscopes is an IVI-compliant driver that allows you to configure, control,

[27] Warm-up begins after the chassis and controller or PC is powered, the PXIe-5172 is recognized by the host, and the PXIe-5172 is configured using the instrument design libraries or NI-SCOPE. In some RIO applications, the power consumed by the PXIe-5172 can be significantly higher than the default image for the module. In these cases, you can improve performance by loading your image and configuring the device before warm-up time begins. Self-calibration is recommended following the specified warm-up time.

and calibrate the device. NI-SCOPE provides application programming interfaces for many development environments.

Related Information

For more information about available software options, refer to the PXIe-5172 Getting Started Guide.

Application Software

NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments:

- LabVIEW
- LabWindows™/CVI™
- Measurement Studio
- Microsoft Visual C/C++
- .NET (C# and VB.NET)

Interactive Soft Front Panel and Configuration

When you install NI-SCOPE on a 64-bit system, you can monitor, control, and record measurements from the PXIe-5172 using InstrumentStudio.

InstrumentStudio is a software-based front panel application that allows you to perform interactive measurements on several different device types in a single program.

Note InstrumentStudio is supported only on 64-bit systems. If you are using a 32-bit system, use the NI-SCOPE–specific soft front panel instead of InstrumentStudio.

Interactive control of the PXIe-5172 was first available via InstrumentStudio in NI-SCOPE 18.1 and via the NI-SCOPE SFP in NI-SCOPE 17.1. InstrumentStudio and the NI-SCOPE SFP are included on the NI-SCOPE media.

NI Measurement & Automation Explorer (MAX) also provides interactive configuration and test tools for the PXIe-5172. MAX is included on the driver media.

TClk Specifications

You can use the NI TClk synchronization method and the NI-TClk driver to align the Sample clocks on any number of supported devices, in one or more chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help*, which is located within the *NI High-Speed Digitizers Help*. For other configurations, including multichassis systems, contact NI Technical Support at *ni.com/support*.

Intermodule Synchronization Using NI-TClk for Identical Modules

Synchronization specifications are valid under the following conditions:

- All modules are installed in one PXI Express chassis.
- The NI-TClk driver is used to align the Sample clocks of each module.
- All parameters are set to identical values for each SMC-based module.
- Modules are synchronized without using an external Sample clock.
- Self-calibration is completed.

Note Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

Skew[28]	300 ps
Skew after manual adjustment	≤10 ps
Sample clock delay/adjustment resolution	3.5 ps

Power

Note Power consumed depends on the FPGA image and driver software used. Specifications for instrument design libraries reflect the performance of a device using the FPGA image from the Multirecord Acquisition sample project. Maximum power consumption occurs at the highest operating temperature.

PXIe-5172 (4 CH) power consumption	
+3.3 V DC	6.5 W, typical
+12 V DC	13.75 W, typical
Total power	20.25 W, typical
PXIe-5172 (8 CH) power consumption	
+3.3 V DC	8.5 W, typical
+12 V DC	18 W, typical
Total power	26.5 W, typical
Total maximum power allowed	38.25 W

28 Caused by clock and analog path delay differences. No manual adjustment performed. Tested with a PXIe-1082 chassis with a maximum slot-to-slot skew of 100 ps. Valid within ±1 °C of self-calibration.

Physical

Dimensions	3U, one-slot, PXI Express Gen 2 x8 Module 18.5 cm × 2.0 cm × 13.0 cm (7.3 in × 0.8 in × 5.1 in)
Weight	
PXIe-5172 (4 CH)	449 g (15.8 oz)
PXIe-5172 (8 CH)	461 g (16.3 oz)

Environment

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 °C to 45 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 4 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Storage Environment

Ambient temperature range	-40 °C to 71 °C (Tested in accordance with IEC 60068-2-1 and IEC 60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC 60068-2-56.)

Shock and Vibration

Operating shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC 60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

Random vibration

Operating	5 Hz to 500 Hz, 0.3 g_{rms} (Tested in accordance with IEC 60068-2-64.)
Nonoperating	5 Hz to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC 60068-2-64. Test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Compliance and Certifications

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the *Product Certifications and Declarations* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- EN 55022 (CISPR 22): Class A emissions
- EN 55024 (CISPR 24): Immunity
- AS/NZS CISPR 11: Group 1, Class A emissions
- AS/NZS CISPR 22: Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations, certifications, and additional information, refer to the *Product Certifications and Declarations* section.

CE Compliance

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit *ni.com/product-certifications*, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Commitment to the Environment* web page at *ni.com/environment*. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit *ni.com/environment/weee*.

电子信息产品污染控制管理办法（中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

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