

# NI PXIe/PCIe-6536/6537 Specifications

## 25/50 MHz Digital I/O Device

This document provides the specifications for the NI PXIe/PCIe-6536/6537 (NI 6536/6537).

Typical values are representative of an average unit operating at room temperature. Specifications are subject to change without notice. For the most recent NI 6536/6537 specifications, visit [ni.com/manuals](http://ni.com/manuals).

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# Channel Specifications

Specification	Value		Comments
Number of data channels	32		—
Direction control of data channels	Per channel		—
Number of Programmable Function Interface (PFI) channels	6		Refer to the <a href="#">Waveform Specifications</a> section for more information about the PFI channels.
Direction control of PFI channels	Per channel		—
Number of RTSI/PXI trigger channels	<b>PXI Express</b>	<b>PCI Express</b>	The NI PXIe-6536/6537 does not support PXI_TRIG 7 as an input trigger.
	10 (PXI_TRIG<0..7>, PXIe_DSTARB, PXIe_DSTARC)	8 (RTSI <0..7>)	
Direction control of RTSI/PXI trigger channels	RTSI<0..7>/PXI_TRIG<0..7>: Bidirectional; per channel  PXIe_DSTARB: Unidirectional input (PXI Express only)  PXIe_DSTARC: Unidirectional output (PXI Express only)		
Number of Sample clock terminals	3 bidirectional clock terminals (PFI 4, PFI 5, RTSI 7)  1 exported clock terminal (PXIe_DSTARC) (PXI Express only)  2 clock source terminals (PXIe_DSTARA, PXI_STAR) (PXI Express only)		Refer to <a href="#">Timing Specifications</a> for more information about clock sources.

## Generation Channels (Data and PFI <0..5> Channels)

Specification	Value				Comments	
Generation voltage families	2.5V, 3.3V (5V TTL compatible)				—	
Generation signal type	Single-ended				—	
Generation voltage levels	<b>Low Voltage Levels</b>		<b>High Voltage Levels</b>		Into 1 M $\Omega$	
	<b>Typical</b>	<b>Maximum</b>	<b>Minimum</b>	<b>Typical</b>		
	2.5 V	0.0 V	0.1 V	2.4 V		2.5 V
	3.3 V	0.0 V	0.1 V	3.2 V		3.3 V
	5.0 V	0.0 V	0.1 V	3.2 V		3.3 V
Output impedance	50 $\Omega$ nominal				—	
Maximum DC drive strength	$\pm 16$ mA at 2.5 V $\pm 32$ mA at 3.3 V				—	
Data channel driver enable/disable control	Per channel				Software-selectable.	
Channel power-up state	Software programmable (Tristate, 0, or 1 at 2.5 V or 3.3 V)				Channel data is typically valid 750 ms after the power up state is set.	
Output protection	The device can indefinitely sustain a short to any voltage between 0 and 5 V.				—	

## Acquisition Channels (Data and PFI <0..5> Channels)

Specification	Value		Comments
Acquisition voltage families	2.5V, 3.3V (5V TTL compatible)		—
Acquisition voltage levels	<b>Low Voltage Thresholds</b>	<b>High Voltage Thresholds</b>	—
	<b>Maximum</b>	<b>Minimum</b>	
2.5 V	0.75 V	1.75 V	
3.3 V	1.0 V	2.3 V	
5.0 V	1.0 V	2.3 V	
Input impedance	High-impedance (50 kΩ to ground)		—
Input protection	-1 to 6 V		Diode clamps in the design may provide additional protection outside this range.

# Timing Specifications

## Sample Clock

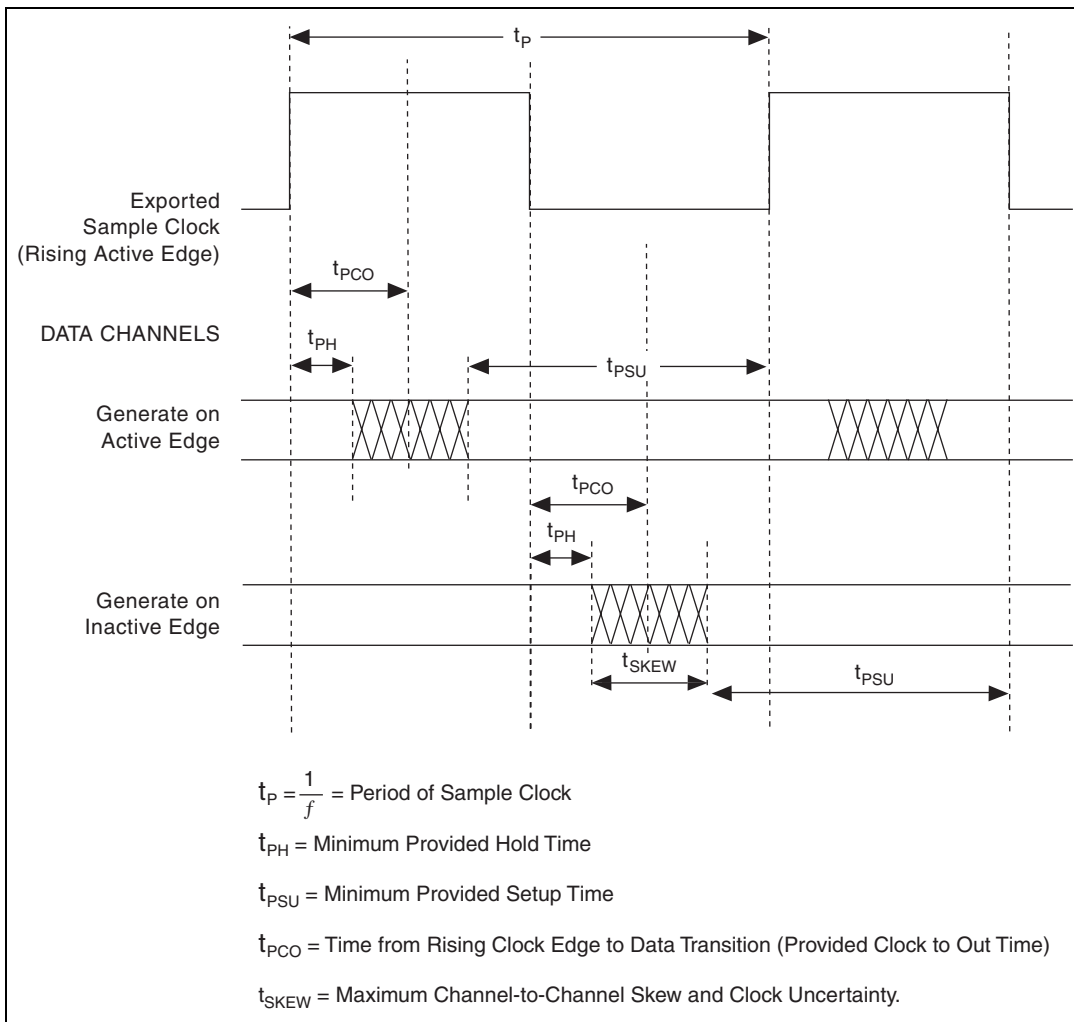
Specification	Value		Comments
Sample clock sources	<ol style="list-style-type: none"> <li>1. On Board Clock (Sample Clock Timebase with divider)</li> <li>2. PFI &lt;4..5&gt;</li> <li>3. PXI_TRIG 7 (PXI backplane—PXI Express only) RTSI 7 (RTSI bus—PCI Express only)</li> <li>4. PXI_STAR (PXI backplane—PXI Express only)</li> <li>5. PXIe_DSTARA (PXI backplane—PXI Express only)</li> </ol>		Refer to the Clocking diagram in the <i>NI 6536/6537 Help</i> for an illustration of the various clock and timebase sources.
Sample clock timebase sources	<ol style="list-style-type: none"> <li>1. 200 MHz Timebase (internal oscillator)</li> <li>2. PFI &lt;0..5&gt;</li> <li>3. PXI_TRIG&lt;0..6&gt; (PXI backplane—PXI Express only) RTSI &lt;0..7&gt; (RTSI bus—PCI Express only)</li> <li>4. PXIe_DSTARB (PXI backplane—PXI Express only)</li> </ol>		
On Board Clock frequency range	NI 6536: 48 Hz to 25 MHz Configurable to 200 MHz/N; $8 \leq N \leq 4,194,307$  NI 6537: 48 Hz to 50 MHz Configurable to 200 MHz/N; $4 \leq N \leq 4,194,307$		—
Imported Sample clock frequency range	<b>PFI &lt;4..5&gt;</b> <b>PXIe_DSTARA (PXIe Only)</b>	<b>PXI_TRIG 7 (PXIe Only)</b> <b>RTSI 7 (PCIe Only)</b>	—
	NI 6536: 0 Hz to 25 MHz NI 6537: 0 Hz to 50 MHz	0 Hz to 25 MHz	
Minimum detectable Sample clock pulse width	<b>PFI &lt;4..5&gt;</b> <b>PXIe_DSTARA (PXIe Only)</b>	<b>PXI_TRIG 7 (PXIe Only)</b> <b>RTSI 7 (PCIe Only)</b>	Positive and negative pulse width at voltage thresholds.
	8 ns	15 ns	
Imported timebase clock frequency range	<b>PFI &lt;0..5&gt;</b> <b>PXIe_DSTARB (PXIe Only)</b>	<b>PXI_TRIG 7 (PXIe Only)</b> <b>RTSI 7 (PCIe Only)</b>	—
	NI 6536: 0 Hz to 25 MHz NI 6537: 0 Hz to 50 MHz	0 Hz to 25 MHz	

Specification	Value		Comments
Minimum detectable imported timebase clock pulse width	<b>PFI &lt;4..5&gt; PXIe_DSTARB (PXIe Only)</b>	<b>PXI_TRIG 7 (PXIe Only) RTSI 7 (PCIe Only)</b>	Positive and negative pulse width at voltage thresholds.
	6.5 ns	15 ns	
Exported Sample clock destinations	<b>Generation</b>	<b>Acquisition</b>	—
	1. PFI 4 2. RTSI 7 (PCI Express only) PXI_TRIG7 (PXI Express only) 3. PXIe_DSTARC (PXI Express only)	PFI 5	
Exported Sample clock duty cycle	Internal Sample clock or divided-down timebase: 33–67% Imported Sample clock: Limited by input duty cycle		Typical.

## Pattern Generation Timing (Data and PFI 5 Channels)

Specification	Value		Comments
Maximum data channel toggle rate	NI 6536: 12.5 MHz NI 6537: 25 MHz		—
Data position modes	<b>Data Channels</b>	<b>PFI Channels</b>	Relative to Sample clock; Active edge may be rising or falling.
	Active edge, Inactive edge	Active edge	
Exported Sample Clock Offset ( $t_{PCO}$ )	3.1 ns		Typical.

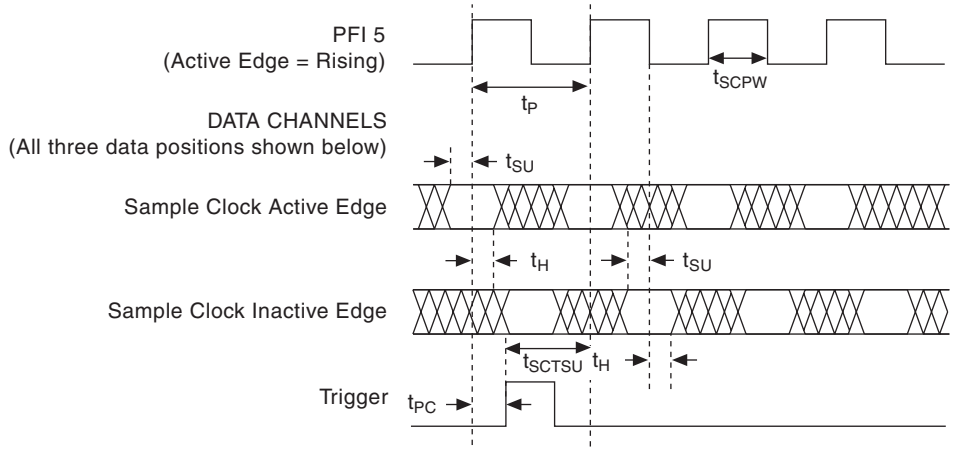
Specification	Value		Comments
	PXI Express	PCI Express	
Minimum provided hold time with respect to PFI 4 ( $t_{PH}$ )	750 ps	1.1 ns	$t_p$ is the Sample clock interval; Values assume the sample is generated and acquired on the same clock edge. Includes maximum channel-to-channel skew. Valid for all data and events.
Minimum provided setup time with respect to PFI 4 ( $t_{PSU}$ )	Sample clock interval ( $t_p$ ) – 5.35 ns	Sample clock interval ( $t_p$ ) – 5 ns	



**Figure 1.** Provided Setup and Hold Times

## Pattern Acquisition Timing (Data and PFI 5 Channels)

Specification	Value		Comments
Setup time with respect to PFI 5 ( $t_{SU}$ )	<b>PXI Express</b>	<b>PCI Express</b>	Maximum required; includes maximum data channel-to-channel skew; valid for data and all triggers except the Start trigger when using the Sample Clock sample timing type.
	2.8 ns	2.0 ns	
Hold time with respect to PFI5 ( $t_H$ )	<b>PXI Express</b>	<b>PCI Express</b>	Maximum required; Sample Clock sample timing type only.
	1.5 ns	2.0 ns	
Setup time of triggers with respect to PFI 5 ( $t_{SCTSU}$ )	15 ns		Maximum required; Sample Clock sample timing type only.
Trigger delay from PFI 5 to trigger edge ( $t_{PC}$ )	2 ns		



$t_{SU}$  = Setup Time with Respect to PFI 5

$t_H$  = Hold Time with Respect to PFI 5

$t_p = \frac{1}{f} = \text{Sample Clock Period}$

$t_{SCPW}$  = Minimum Detectable Sample Clock Pulse Width

$t_{PC}$  = Trigger Delay from PFI 5 to Trigger Edge\*

$t_{SCTS_U}$  = Setup Time of Trigger with Respect to PFI 5\*

\*Sample Clock Sample Timing Type only.

**Figure 2.** Acquisition Timing Diagram Using PFI 5 as the Sample Clock

## Handshaking

Specification	Value	Comments
Asynchronous handshaking modes	Handshake (8255) sample timing type	8255 emulation equivalent.
Synchronous handshaking modes	<ol style="list-style-type: none"> <li>1. Burst sample timing type</li> <li>2. Pipelined Sample Clock sample timing type</li> </ol>	—
Control line polarity	<ol style="list-style-type: none"> <li>1. Active high</li> <li>2. Active low</li> </ol>	—
Program-mable delay resolution for Handshake sample timing type	20 ns	—

## Change Detection

Specification	Value	Comments
Change detection resolution	Sample clock period	—
Sources	P0.<0..7>, P1.<0..7>, P2.<0..7>, P3.<0..7>	Per data channel selectable.
Valid sample position	<ol style="list-style-type: none"> <li>1. Active edge</li> <li>2. Inactive edge</li> </ol>	Per data channel selectable.
Valid changes	<ol style="list-style-type: none"> <li>1. Don't care</li> <li>2. Rising edge</li> <li>3. Falling edge</li> <li>4. Rising or falling edge</li> </ol>	Per data channel selectable.

# Waveform Specifications

## Memory

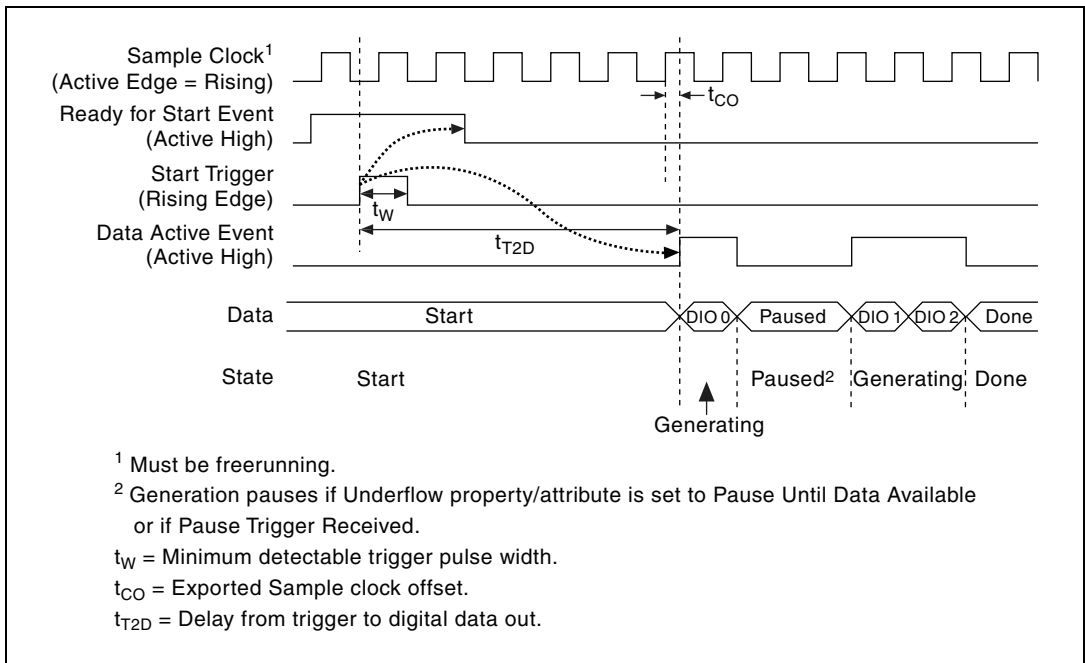
Specification	Value	Comments
Onboard memory size	2,048 samples (S)	FIFO based.
Transfer type	1. DMA 2. Programmed I/O (On Demand sample timing type only)	—
Generation waveform quantum	Waveform size must be an integer multiple of 1 S.	—
Acquisition minimum buffer size	2 S	—

## Triggers

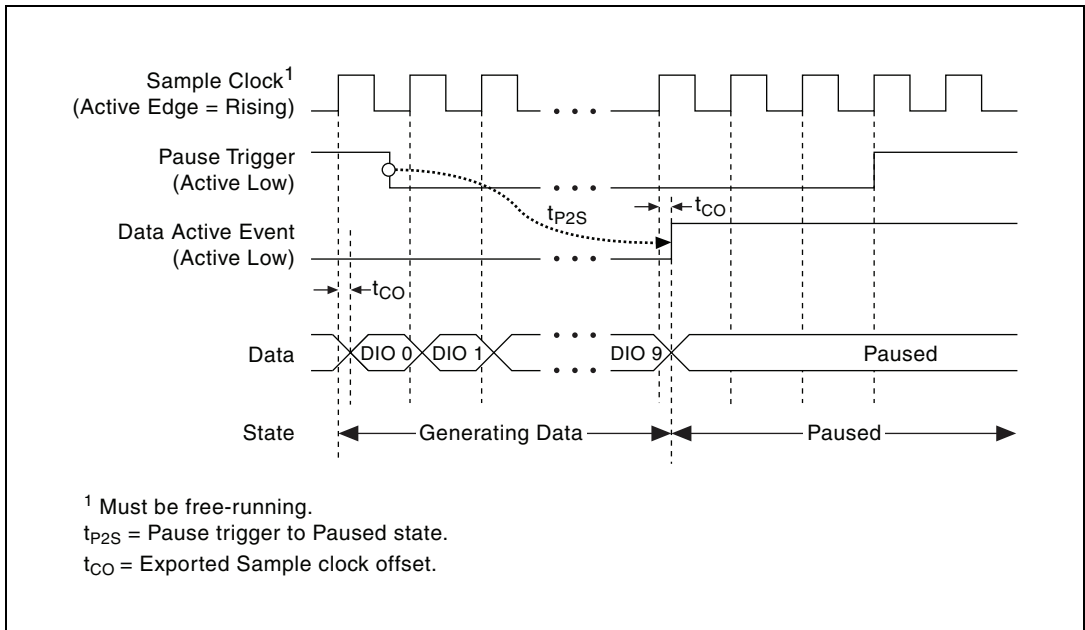
Specification	Value			Comments
Supported triggers (by sample timing type)	<b>Sample Timing Type</b>	<b>Acquisition</b>	<b>Generation</b>	Generation operations do not support pattern match triggers.
	<b>Sample Clock</b>	Start, Reference	Start	
	<b>Pipelined Sample Clock</b>	Pause, Start, Reference	Pause, Start	
	<b>Burst Handshake</b>	Pause (not including the pattern match type trigger)	Pause	
	<b>Handshake</b>	Handshake	Handshake	
	<b>Change Detection</b>	Start	N/A	

Specification	Value		Comments
Sources	<ol style="list-style-type: none"> <li>1. PFI &lt;0..5&gt; (DDC connector)</li> <li>2. PXI_TRIG&lt;0..6&gt; (PXI backplane—PXI Express only) RTSI &lt;0..7&gt; (RTSI bus—PCI Express only)</li> <li>3. PXIe_DSTARB (PXI backplane—PXI Express only)</li> <li>4. Pattern match (Acquisition sessions only)</li> <li>5. Disabled (Do not wait for a trigger)</li> </ol>		—
Trigger detection	<ol style="list-style-type: none"> <li>1. Start Trigger (Edge detection: rising or falling; Pattern match: match or does not match)</li> <li>2. Pause Trigger (Level detection: high or low; Pattern match: match or does not match)</li> <li>3. Reference Trigger (Edge detection: rising or falling; Pattern match: match or does not match)</li> <li>4. Handshaking Trigger (Interlocked: high or low)</li> </ol>		—
Destinations	<ol style="list-style-type: none"> <li>1. PFI &lt;0..5&gt; (DDC Connector)</li> <li>2. PXI_TRIG&lt;0..7&gt; (PXI backplane—PXIe only) RTSI &lt;0..7&gt; (RTSI bus—PCIe only)</li> <li>3. PXIe_DSTARC (PXI backplane—PXI Express only)</li> </ol>		—
Delay from Pause trigger to Paused state ( $t_{P2S}$ )	Generation		Acquisition
	Minimum	Maximum	
	6 sample clock cycles + 6.7 ns	<b>PCIe:</b> 7 sample clock cycles + 15.4 ns  <b>PXIe:</b> 7 sample clock cycles + 17 ns	Synchronous to the data
Delay from trigger to digital data output ( $t_{T2D}$ )	Generation		Acquisition
	Minimum	Maximum	
	65 ns	1 sample clock cycle + 130 ns	N/A
			Guaranteed by design.

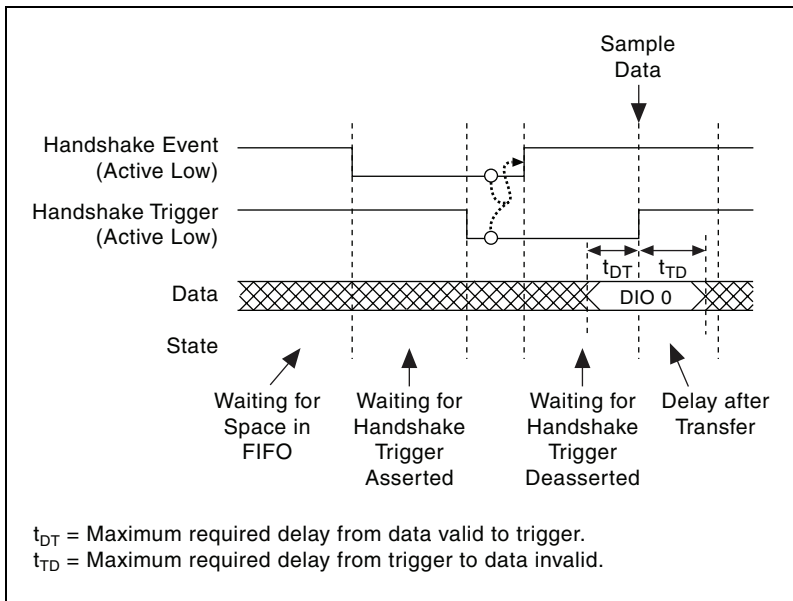
Specification	Value		Comments
Minimum detectable trigger pulse width ( $t_w$ )	<b>Sample Clock Timing Mode Triggers and Pipelined Mode Generation Start Trigger</b>	<b>Burst and Pipelined Mode Generation Pause Trigger</b>	Maximum required pulse width to guarantee sampling by an asynchronous clock; synchronous triggers have same setup and hold requirements as data.
	10 ns	Sample clock period + 4 ns	
Maximum required setup and hold of Sample Clock sample timing type triggers with respect to PFI 5	Refer to the <i>Pattern Acquisition Timing (Data and PFI 5 Channels)</i> section of this document.		—
Maximum required delay from data to Handshake trigger ( $t_{DT}$ )	5 ns		Maximum required time between data valid and the Handshake trigger; Handshake sample timing type only.
Maximum required delay from Handshake trigger to data ( $t_{TD}$ )	50 ns		Maximum required time between the Handshake Trigger and data invalid; Handshake sample timing type only.



**Figure 3.** Pipelined Generation Timing Diagram



**Figure 4.** Pipelined Generation Handshaking Timing Diagram



**Figure 5.** Handshake (8255) Acquisition Timing Diagram

## Events

Specification	Value			Comments
Supported events (by sample timing type)	<b>Sample Timing Type</b>	<b>Acquisition</b>	<b>Generation</b>	—
	<b>Sample Clock</b>	Ready for Start	Ready for Start, Data Active	
	<b>Pipelined Sample Clock</b>	Ready for Transfer, Ready for Start	Ready for Start, Data Active	
	<b>Burst Handshake</b>	Ready for Transfer	Ready for Transfer	
	<b>Handshake</b>	Handshake	Handshake	
	<b>Change Detection</b>	Change Detection, Ready for Start	N/A	

Specification	Value		Comments
Destinations	1. PFI <0..5> (DDC Connector) 2. PXI_TRIG<0..7> (PXI backplane—PXIe only) RTSI <0..7> (RTSI bus—PCIe only) 3. PXIe_DSTARC (PXI backplane—PXI Express only)		—
Pulse width for the exported Change Detection event	<b>Frequency ≤ 10 MHz</b>	<b>Frequency &gt; 10 MHz</b>	Software determined based on Sample clock frequency.
	50 ns	15 ns	
Delay from Change Detect to event	<b>Minimum</b>	<b>Maximum</b>	Delay from data at the DDC connector to the event generated on the DDC connector.
	90 ns	<b>PCIe:</b> 1 Sample clock cycle + 100 ns <b>PXIe:</b> 1 Sample clock cycle + 105 ns	

## Nonvolatile Storage

Specification	Value	Comments
Description	16 Mbit storage for firmware and power up states	—
Write Cycles	75,000 minimum	—

## Power

Specification	Value		Comments
	Typical	Maximum	
+3.3 VDC	700 mA	750 mA	All data channels loaded by 5 kΩ.
+12 VDC	250 mA	300 mA	
Total power	5.1 W	6.1 W	

## Physical Specifications

Specification	Value		Comments
Dimensions	PXI Express	PCI Express	
	21.4 cm × 2.0 cm × 13.1 cm (8.42 in. × 0.79 in. × 5.14 in.)	18.1 cm × 2.2 cm × 12.6 cm (7.13 in. × 0.85 in. × 4.93 in.)	—
Weight	144.58 g (5.1 oz)	107.7 g (3.8 oz)	—

## Software

Specification	Value	Comments
Driver software	NI-DAQmx driver software version 8.5 or later	—
Application software	<p>NI-DAQmx provides programming interfaces for the following application development environments:</p> <ul style="list-style-type: none"> <li>• National Instruments LabVIEW 7.1 or later</li> <li>• National Instruments LabWindows™/CVI™ 6.0 or later</li> <li>• Microsoft Visual Studio 6.0 or later for ANSI C</li> <li>• Microsoft Visual Studio 2003 for C++</li> </ul>	—
Test Panel	National Instruments Measurement and Automation Explorer (MAX) provides test panels with basic acquisition and generation functionality for the NI 6536/6537. MAX is included on the NI-DAQmx driver CD.	—

## Environment



**Note** The NI 6536/6537 is intended for indoor use only.

Specification	Value		Comments
Operating temperature	PXI Express	PCI Express	
	0 to +55 °C	0 to +45 °C	—
Storage temperature	–20 to 70 °C		—

Specification	Value	Comments
Operating relative humidity	10 to 90% relative humidity, noncondensing (Meets IEC 60068-2-56)	—
Storage relative humidity	5 to 95% relative humidity, noncondensing (Meets IEC 60068-2-56)	—
Operating shock	30 g, half-sine, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	PXIe only
Storage shock	50 g, half-size, 11 ms pulse (Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.)	PXIe only
Operating vibration	5 to 500 Hz, 0.31 g <sub>rms</sub> (Meets IEC 60068-2-64.)	PXIe only
Storage vibration	5 to 500 Hz, 2.46 g <sub>rms</sub> (Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class B.)	PXIe only
Altitude	0 to 2,000 m above sea level (at 25 °C ambient temperature)	—
Pollution Degree	II	—

## Safety, Electromagnetic Compatibility, and CE Compliance

Specification	Value	Comments
Safety	<p>This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:</p> <ul style="list-style-type: none"> <li>• IEC 61010-1, EN 61010-1</li> <li>• UL 61010-1, CSA 61010-1</li> </ul>	
<p><b>Note:</b> For UL and other safety certifications, refer to the product label or visit <a href="http://ni.com/certification">ni.com/certification</a>, search by model number or product line, and click the appropriate link in the Certification column.</p>		

Emissions	EN 55011 Class A at 10 m FCC Part 15A above 1 GHz	With use of SHC68-C68-D2 or SHC68-C68-D4 shielded cable.
Electro-magnetic Compatibility	<p>This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:</p> <ul style="list-style-type: none"> <li>• EN 61326 EMC requirements; Minimum Immunity</li> <li>• EN 55011 Emissions; Group 1, Class A</li> <li>• CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A</li> </ul> <p><b>Note:</b> For EMC compliance, device <i>must</i> be operated with shielded cabling. In addition, filler panels must be installed.</p>	—
This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:		
CE Compliance	<ul style="list-style-type: none"> <li>• 73/23/EEC; Low-Voltage Directive (safety)</li> <li>• 89/336/EEC; Electromagnetic Compatibility Directive (EMC)</li> </ul>	—
<b>Note:</b> Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit <a href="http://ni.com/certification">ni.com/certification</a> , search by model number or product line, and click the appropriate link in the Certification column.		
Waste Electrical and Electronic Equipment (WEEE)	<b>EU Customers:</b> At the end of their life cycle, all products <i>must</i> be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit <a href="http://ni.com/environment/weee.htm">ni.com/environment/weee.htm</a> .	

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