

3.5 Ensuring Compliance for Next-Generation Serial Buses

Evaluating Platforms for Performance and Reusability

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Tektronix is a member of a number of working groups within standards organizations and trade associations

Tektronix participates in industry “Plugfests” – for example, PCI-Express

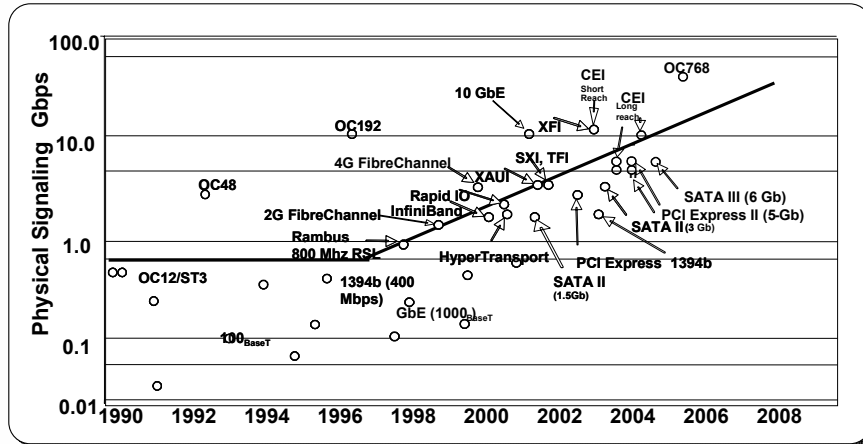
Tektronix role in development, evolution of serial data standards

We contribute test methods information exchange

Ensure practicality and feasibility in the specifications

Tek has a strong history in Serial Data standards, providing the Special Interest Groups (SIG) with guidance and direction on proper testing approaches. Participation in the plugfests with equipment and consultation on how to get equipment compliant.

Customer Needs – Increasing Signal Speeds

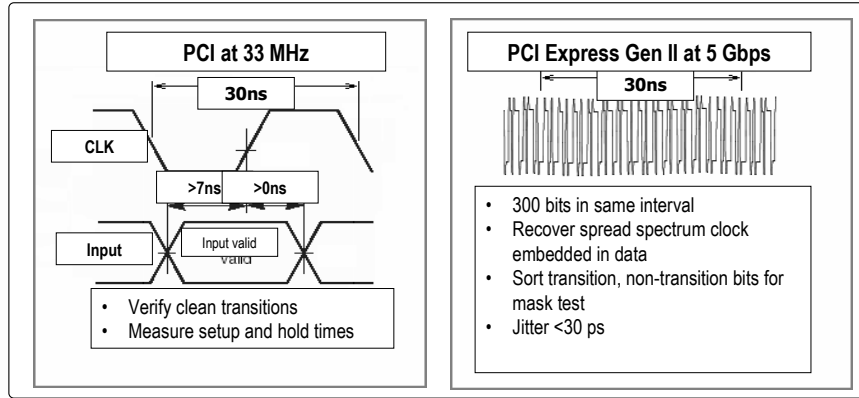


Testing and signal integrity challenges are growing as chips and boards increase in operating speeds and densities

A consistent trend is growth in speed and scalability in Serial data Standards. This graph shows some of the new standards being proposed and/or adopted and their impact on signal speeds. This adds significant challenges to testing and signal integrity environments.

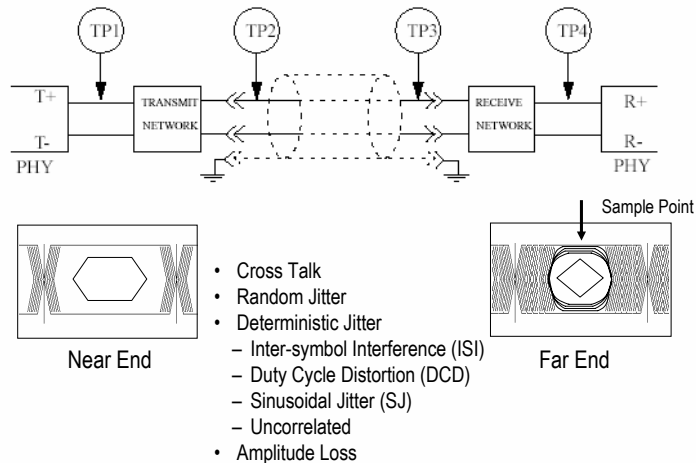
Customer Needs – Increasing Complexity

- Compare PCI, PCI Express activity over the same time interval



- Traditional voltage versus time display is insufficient for insight into signaling activity

What are we trying to determine here?



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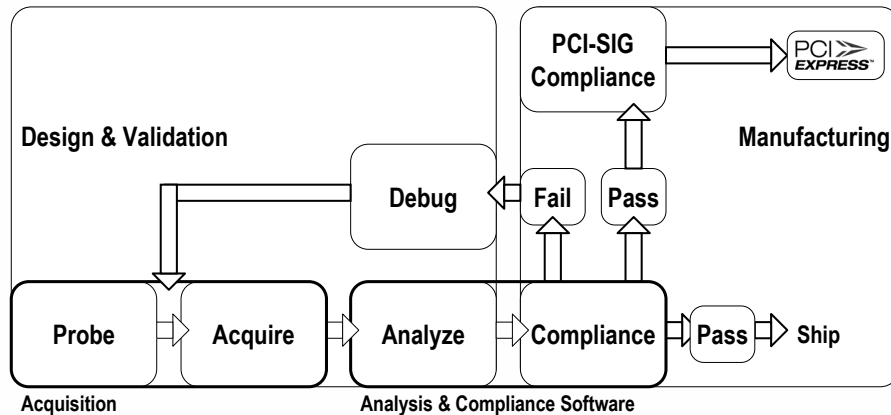
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So what is the objective here? Well, in order to design a compliant device, we need to design a transmitter that will present an Open Eye at the receiver, so when the clock is recovered from the data, and the receiver clocks in the data at the Sample Point, that it sees the one or zero that was transmitter. We need to send 1012 bits reliably as defined by the standard's Bit Error Ratio specification. This must be true with a worst case transmission channel.

The things standing in our way of achieving this objective are cross talk, random jitter, deterministic jitter, and amplitude loss.

The concept of serial data transmission is simple, but when transmitting at frequencies of 2.5 GHz, this sometimes becomes a major challenge.

Systematic Approach to Compliance/Analysis

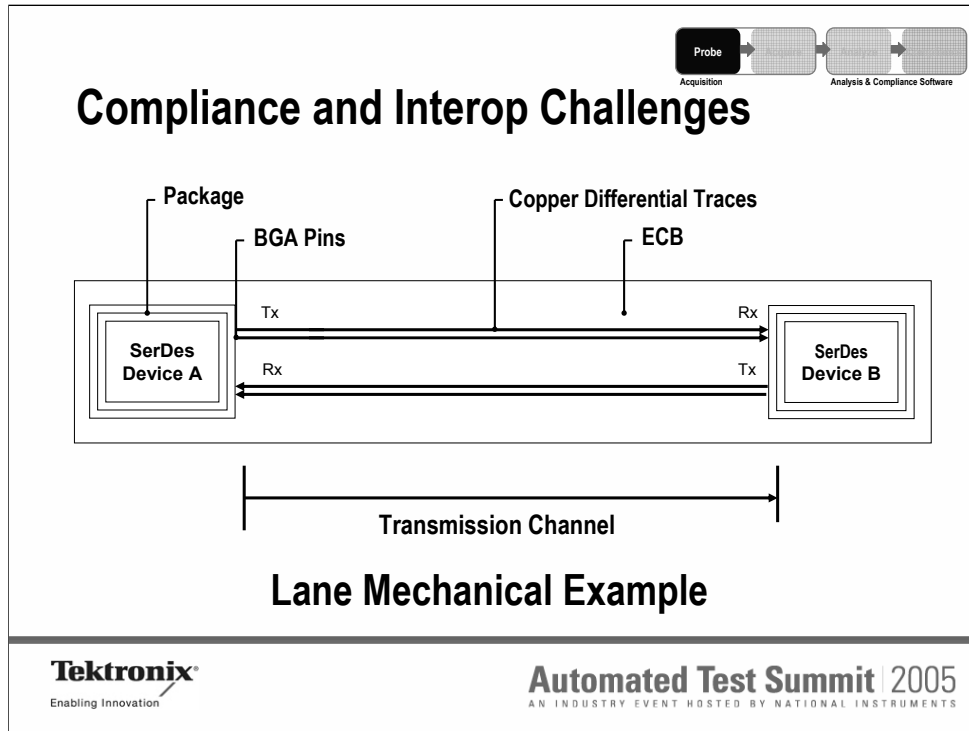


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Now that we understand some of the challenges, let's move on to the measurement solutions. First we must ask, what is the problem we are trying to solve? The ultimate goal is to ship parts or system components that are compliant with the specification. Compliance is a wonderful thing. When we have compliance, we can consider our design complete and ship our product to customers. We can also get our devices certified. Compliance tools are very valuable in the last stages of design to prove compliance to standards.

However, what happens if we fail the compliance test? We must have tools we can use to debug our design. This is where waveform data analysis tools become important. The focus of the latter part of this presentation will be in the Compliance and Analysis portion of the solution. But first we need to insure that we have good signal fidelity going into the analysis. Signal Fidelity is defined by how accurately we can get the signal into our acquisition memory, and is the combination of the quality of the probing solution and the acquisition system of the measurement instrument.

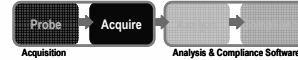


The first step to evaluating Signal Integrity is good probing. Every oscilloscope solution starts at the probe tip. Since there is such a wide range of probing choices, this is often the point at which the most errors are made when validating devices. Del Cecchi from IBM reminds us that “On a printed circuit board, there is no such thing as a differential signal, just two single ended signals being transmitted in a differential mode”. This emphasizes the need to not only consider differential mode effects on the signal, but also common mode effects that can lead to signal integrity analysis issues.

This brings us to looking at an example application, here is a chip-chip link transmitted across a length of circuit board. In this configuration, we will probe as closely as possible to the receiver pins in order to get good signal integrity. There are two possible probing configurations we can use. But how do we probe it—single-ended, differentially?

Real-time Oscilloscope

- System Analog BW > 1.8 x Bit Rate
- System (with probe) Rise time Specs
 - PCI Express Gen 1 Spec 50ps *(20%-80%) minimum
 - PCI Express Gen 2 Spec 30ps *(20%-80%) minimum
 - 6 GHz SE (P7260) – *45ps
 - 12.5 GHz Diff (P7313) – * <25ps
 - 8 GHz Diff (P7380SMA) – * <35ps
- Sample Rate satisfies Nyquist
 - >2X Instrument Bandwidth
 - >3X Interpolation
- Record Length
 - Dependent on analysis method



TDS6000C

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First we consider analog bandwidth. The Fibre Channel specifications FC-PI states that for accurate rise time measurements, an oscilloscope should have a bandwidth of 1.8 times the bit rate (or baud rate). A 2.5 GS/s, an NRZ signal has a 1.25 GHz fundamental. The 1.8 factor provides adequate bandwidth to capture the first and third harmonic. TDS 4 and 6 GHz models provide a good solution for signals ranging from 1–3Gb/s.

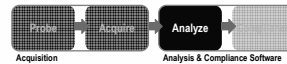
What is more important than bandwidth is the rise time specification, especially since test equipment vendors sometimes specify rise time differently. Tektronix specifies its probe rise time (10–90% guaranteed). This guaranteed specification converted to 20–80% is <25–65ps depending on the probe configuration with the scope being used. The 6 and 8 GHz Bullets assume either the 6804B or 6124C/6154C scopes. The 12.5 GHz bullet assumes it is paired with the 6154C. For PCI Express, Gen 2, the minimum Rise time is 30ps at transmitter pins, maximum is 60ps. This is right in the sweet spot of accurate rise time measurements with P7313 and TDS6154C. As we can make accurate rise times with 5% accuracy on 30ps transition times.

An important thing to keep in mind is that the minimum specification (at the IC pins) is on the same order as the probe. Therefore, there will always be rise time error in the measurement. Typically as the signal travels across some length of circuit board to a connector, the rise times are between 100–150ps, making this measurement error less, but still present. Faster instruments, such as sampling oscilloscopes are available for making more accurate rise time measurements.

However, because of the data analysis advantage on real-time data, the real time scope has become the workhorse for validation and compliance.

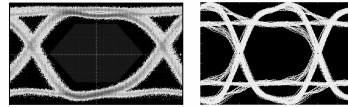
The required sample rate is dependent on the rise time and bandwidth of the signal under test. Nyquist states that if your sample rate exceeds your bandwidth by greater than 2X, then the analog signal can be accurately reconstructed using $\text{Sin}(x)/x$ interpolation. All Tektronix real time oscilloscopes meet this standard. The required interpolation factor for accurate measurements depends on the measurement. However, a good rule of thumb is 3X interpolation or three interpolated points between each real sample point.

Finally, record length need is dependent on the data analysis method used, primarily in the area of jitter measurements. The analysis method used for PCI Express does not require long record length while the analysis method for Jitter defined by the MJSQ for total jitter at a specified BER does require longer records, if a long data pattern such as Compliant Jitter Pattern (CJTPAT) is used.



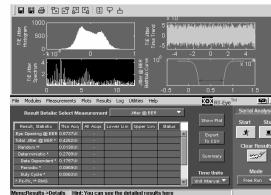
Serial Data Analysis

- Clock to Data Recovery (CDR), Eye Diagram Mask Testing
 - Hardware CDR (PLL)
 - Software CDR (PLL + Others)



- Measurements

Timing		Amplitude		Jitter
Eye Width/ Eye Height	Unit Interval	Differential Voltage	CM Voltage	Jitter @ BER
Rise Time	Bit Rate	High Amplitude	AC CM Voltage	TIE Jitter
Fall Time	Differential Skew	Low Amplitude	De- Emphasis	

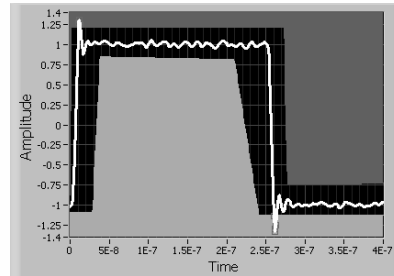


- Plotting

- Jitter: Trend, Spectrum, Histogram, Bathtub Curve

Custom Serial Data Analysis in LabVIEW

- Limit/Mask Testing
- Timing/Transition Measurement
 - Frequency, period, pulse duration, duty cycle, preshoot, overshoot, slew rate
- Develop custom serial data with software-defined hardware
 - LabVIEW FPGA module
 - Advanced timing/triggering



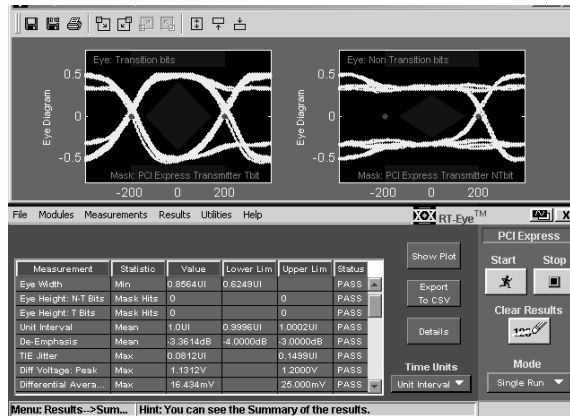
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As an alternative to turn-key systems, you can perform many common digital measurements in LabVIEW. Using standard connectivity methods like GPIB or serial, they can acquire these waveforms from a Tektronix scope. Then, you can take advantage of Express VIs to implement limit/mask testing as well as timing and transition measurements on signals of any frequency or shape. This allows the user to work with custom digital signals or serial data protocols not testable through a turn-key solution. With the LabVIEW FPGA module, you can make use of advanced timing and triggering to prototype down to the physical layer.

Compliance Test – Simple Approval ID

Example: PCI Express Compliance Test on a Tektronix Scope



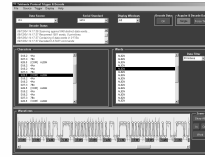
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Here we see the result of a PCI Express transmitter Compliance test. All the tests are completely automated and a Pass/Fail indication is given in the status column of the software. It's almost as simple as a rubber stamp.

Debug

- Protocol Trigger – Decode
 - Trigger on Protocol word
- Jitter Trend (view jitter waveform)
 - Correlate jitter waveform with waveform.
- Transients and noise captured
- Complex triggering
- Acquisition Modes (FastAcq and WfmDb)
- More integrated debug
 - Integrated LA and Oscilloscope Solution
 - Multi-Channel View
 - Signal Sources for traffic generation
 - Golden Stimulus



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The final step of our design and validation process is one that it is often nice to avoid. However, if your design is not compliant, there are several steps that can be taken to debug your device using not only the features of the RT-Eye analysis software, but additional features of the instrument and even the use of other instruments such as Logic Analyzers and Signal sources.

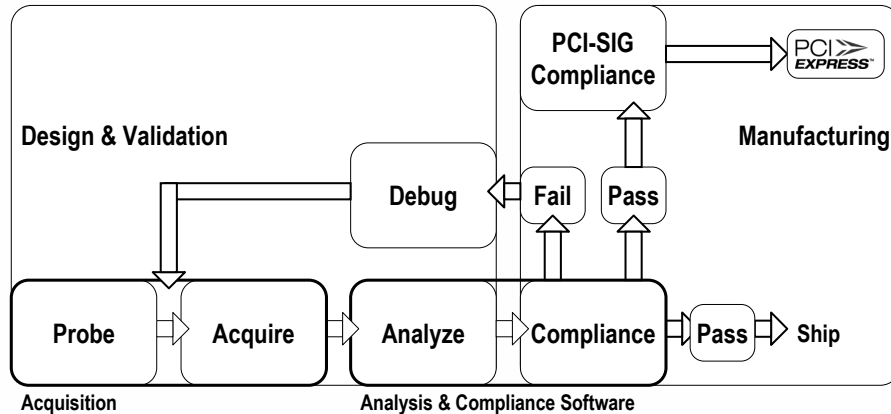
One powerful debug attribute of a real time oscilloscope is that the acquisition is continuous data of the actual waveform. This allows you to see signal behavior not obvious on Equivalent Time devices such as sampling oscilloscopes and time interval analyzers.

As seen earlier, different views of jitter (histogram, trend, spectrum) can lead you to diagnosing sources of jitter in your system such as cross talk or power supply coupling.

Other powerful debug features include the ability to view transients and noise. You can use complex triggers to isolate error conditions and different Acquisition modes such as Fast Acquisition and Waveform Database to view random events that cause system problems.

The oscilloscope can also be cross triggered with a Logic Analyzer or used in conjunction with a Digital Timing Generator for jitter stress testing.

Compliance and Analysis – Summary



www.tektronix.com/serial_data for more information

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We have now completed our tour through the steps to compliant devices in the Serial Data domain. Thank you for your participation. We hope this presentation has been helpful in understanding the measurement challenges and some recommended solutions for the validation, compliance testing, and debug of your devices. Proper understanding of these issues and proper use of the tools can save you many headaches and hopefully time to market. If you'd like more information and tips on how to get the proper measurement suite for your serial design, visit www.tektronix.com/serial_data and select from many emerging serial standards.