Manufacturer: NI

Board Assembly Part Numbers (Refer to Procedure 1 for identification procedure)**:**

Part Number and Revision	Description
134575A-01L or later	**STS-MMWAVE-02**

Volatile and Non-Volatile Memory of Component Models

Volatile Memory

Target Data	*Type*	*Size*	*Battery Backup*	*User[1] Accessible*	*System Accessible*	*Sanitization Procedure*
None						

Non-Volatile Memory (*incl. Media Storage*)

Target Data	*Type*	*Size*	*Battery Backup*	*User Accessible*	*System Accessible*	*Sanitization Procedure*
Board identification, reserved and user memory space (“IDPROM”) x4 (4 IDPROMs per CCLB)	EEPROM	4kB x 8 (32 Kbit) (x4)	No	Yes	Yes	Procedure 2

[1] Refer to *Terms and Definitions* section for clarification of *User* and *System Accessible*

Procedures

Procedure 1 – Board Assembly Part Number identification:
To determine the Board Assembly Part Number and Revision, find it with the serial number that is visible on the top cover of the board. Refer to Figure 1.

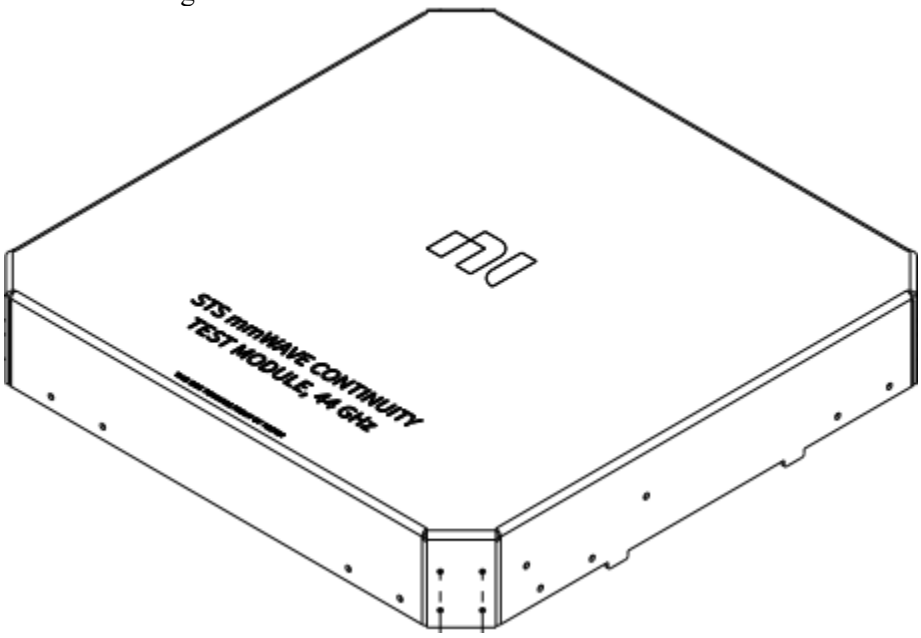

Figure 1 CCLB board (top view)

Procedure 2 – IDPROM:
All the memory on this device is user accessible through the Semiconductor Test System (STS) Maintenance Software (MSW) LabVIEW Applications Programming Interface (API). To install LabVIEW and the STS MSW API, download and install the latest version of the NI Semiconductor Test System Development Software available at ni.com.
https://www.ni.com/en-us/support/downloads/software-products/download.semiconductor-test-system-development-software.html

WARNING: Changing any values in the memory could result in improper behavior of the system.

To **clear the IDPROM**, complete the following steps in LabVIEW (refer to Figure 2 for block diagram of the procedure):

1. Place the CCLB board on the STS blindmate.
2. Lock CCLB in place so that IDPROM pins come in contact with the spring-loaded P142 and P143 pogo block pins on the STS blindmate. Refer to Figures 3 and 4 in the Appendix.
3. Open an STS session using the "niSTS Initialize SVCFWD.vi".
4. Configure the I2C communication using the "niSTS configure I2C.vi" and setting it up as follows:
    a. Use drop down option "IDPROM I2C Configure"
    b. Wire in a constant into "I2C Protocol Configure" with the following:
        i. Set Address to 80 decimal (50 hex)
        ii. Set the Rate to 100 kHz
    c. Wire in a constant into "Write Options" with the following:
        i. Set the Page size to 32 bytes

ii. Set Write Delay Between Pages to 5 ms

5. Configure the I2C path using the “niSTS Write I2C.vi” and setting it up as follows:
    a. Use drop down option “IDPROM I2C Write – No Register (U8)”
    b. Wire into “Register Values” an array of size 1 with a U8 constant of 0
6. Configure the I2C communication using the “niSTS configure I2C.vi” and setting it up as follows:
    a. Use drop down option “IDPROM I2C Configure”
    b. Wire in a constant into “I2C Protocol Configure” with the following:
        i. Set Address to 80 decimal (50 hex)
        ii. Set the Rate to 100 kHz
    c. Wire in a constant into “Write Options” with the following:
        i. Set the Page size to 32 bytes
        ii. Set Write Delay Between Pages to 5 ms
7. write to the memory using the “niSTS Write I2C.vi” and setting it up as follows:
    a. Use drop down option “IDPROM I2C Write (U8 Data, U16 Address)”
    b. Wire into “Register Values” an array of size 4000 with U8 constants, these can all be set to 00 or FF
    c. Wire 0 into “Register Address”
    d. Wire 100000 into “ms timeout”
8. Close the STS session using the “niSTS Close.vi”
9. Save the VI and run it. This would clear IDPROM #1.
10. Unlock CCLB from the STS Blindmate and rotate CCLB clockwise one time to erase the next IDPROM (Note: only one IDPROM is mated with the STS blindmate when the CCLB is fully locked).
11. Lock CCLB in place and run the created VI to clear IDPROM#2.
12. Repeat the steps 10-11 rotating CCLB clockwise each time.

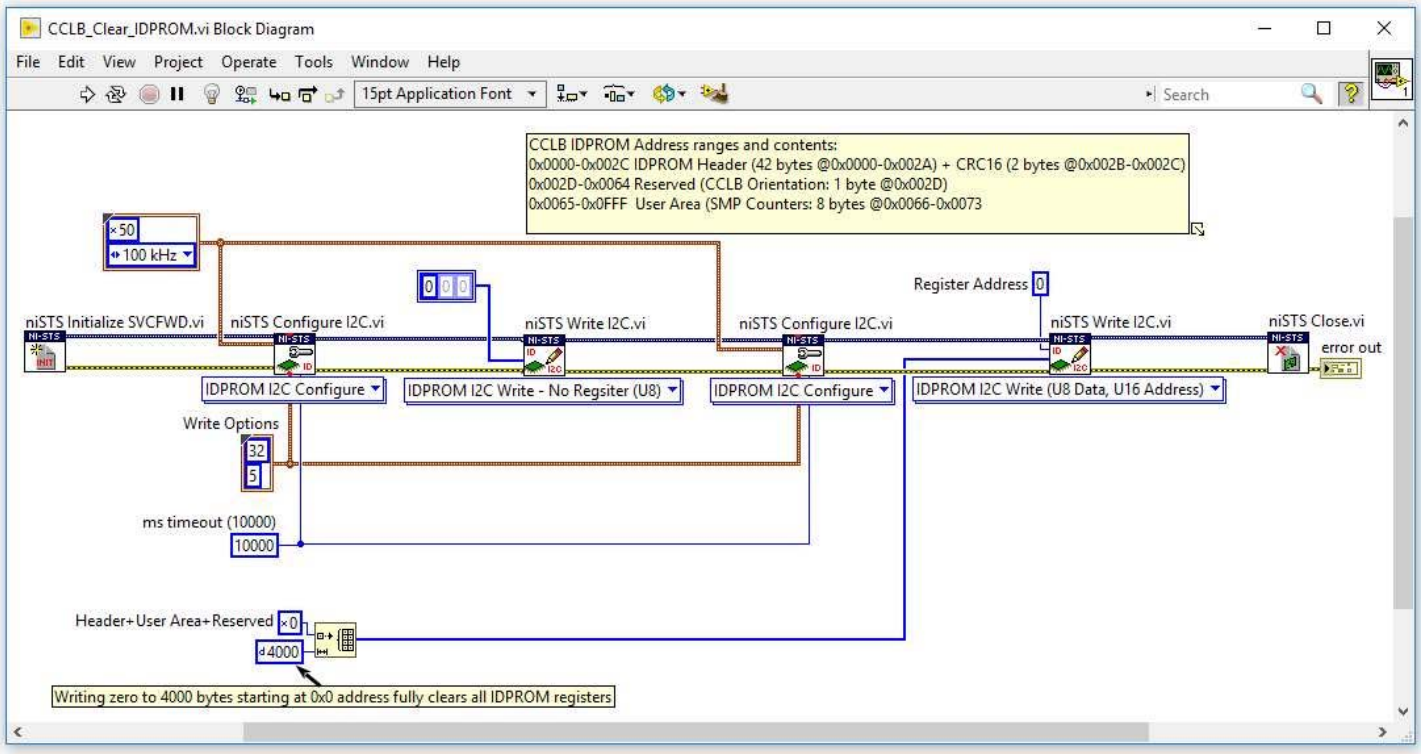

Figure 2 CCLB Clear IDPROM Procedure

To **verify the IDPROM** has been correctly cleared, complete the following steps in LabVIEW:

1. Place the CCLB board on the STS blindmate and lock it in place so that IDPROM pins come in contact with the spring-loaded P142 and P143 pogo block pins on the STS blindmate
2. Open an STS session using the "niSTS Initialize SVCFWD.vi".
3. Configure the I2C communication using the "niSTS configure I2C.vi" and setting it up as follows:
    a. Use drop down option "IDPROM I2C Configure"
    b. Wire in a constant into "I2C Protocol Configure" with the following:
        i. Set Address to 80 decimal (50 hex)
        ii. Set the Rate to 100 kHz
    c. Wire in a constant into "Write Options" with the following:
        i. Set the Page size to 32 bytes
        ii. Set Write Delay Between Pages to 5 ms
4. Configure the I2C path using the "niSTS Write I2C.vi" and setting it up as follows:
    a. Use drop down option "IDPROM I2C Write – No Register (U8)"
    b. Wire into "Register Values" an array of size 1 with a U8 constant of 0
5. Configure the I2C communication using the "niSTS configure I2C.vi" and setting it up as follows:
    a. Use drop down option "IDPROM I2C Configure"
    b. Wire in a constant into "I2C Protocol Configure" with the following:
        i. Set Address to 80 decimal (50 hex)
        ii. Set the Rate to 100 kHz
    c. Wire in a constant into "Write Options" with the following:
        i. Set the Page size to 32 bytes
        ii. Set Write Delay Between Pages to 5 ms
6. Read the memory using the "niSTS Read I2C.vi" and setting it up as follows:
    a. Use drop down option "IDPROM I2C Read (U8 Data, U16 Address)"
    b. Wire 0 into "Register Address"
    c. Wire 4000 into IDPROM # of Bytes
    d. Wire 100000 into "ms timeout"
7. Close the STS session using the "niSTS Close.vi"

Terms and Definitions

CCLB:
Continuity Checker Load Board

Cycle Power:
The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

Volatile Memory:
Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application specific data such as capture waveforms.

Non-Volatile Memory:
Power is not required to maintain the stored information. Device retains its contents when power is removed. This type of memory typically contains information necessary to boot, configure, or calibrate the product or may include device power up states.

User Accessible:
The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

System Accessible:
The component is read and/or write addressable from the host without the need to physically alter the product.

Clearing:
Per *NIST Special Publication 800-88 Revision 1*, "clearing" is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

Sanitization:
Per *NIST Special Publication 800-88 Revision 1*, "sanitization" is a process to render access to "Target Data" on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.

APPENDIX

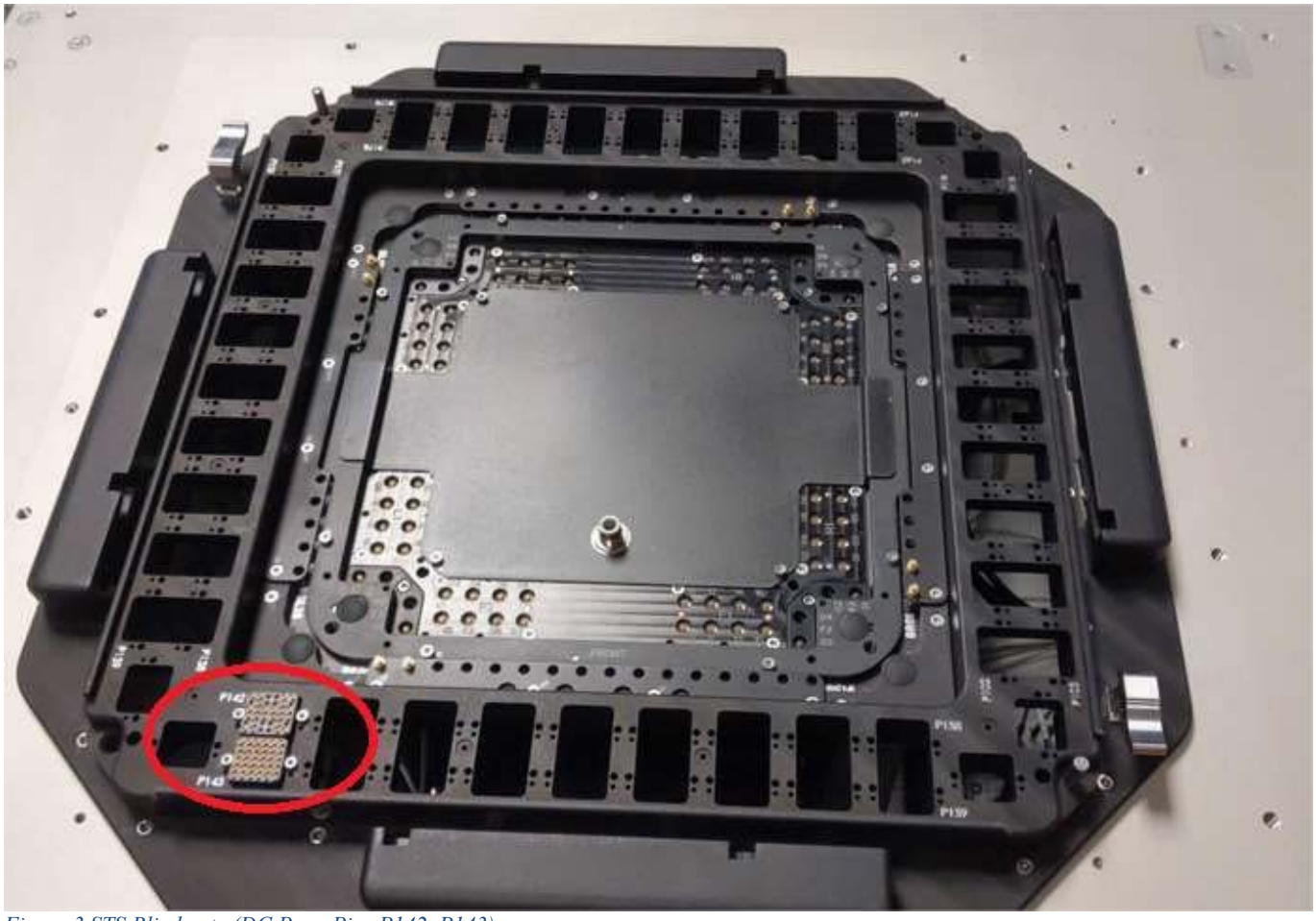

Figure 3 STS Blindmate (DC Pogo Pins P142, P143)

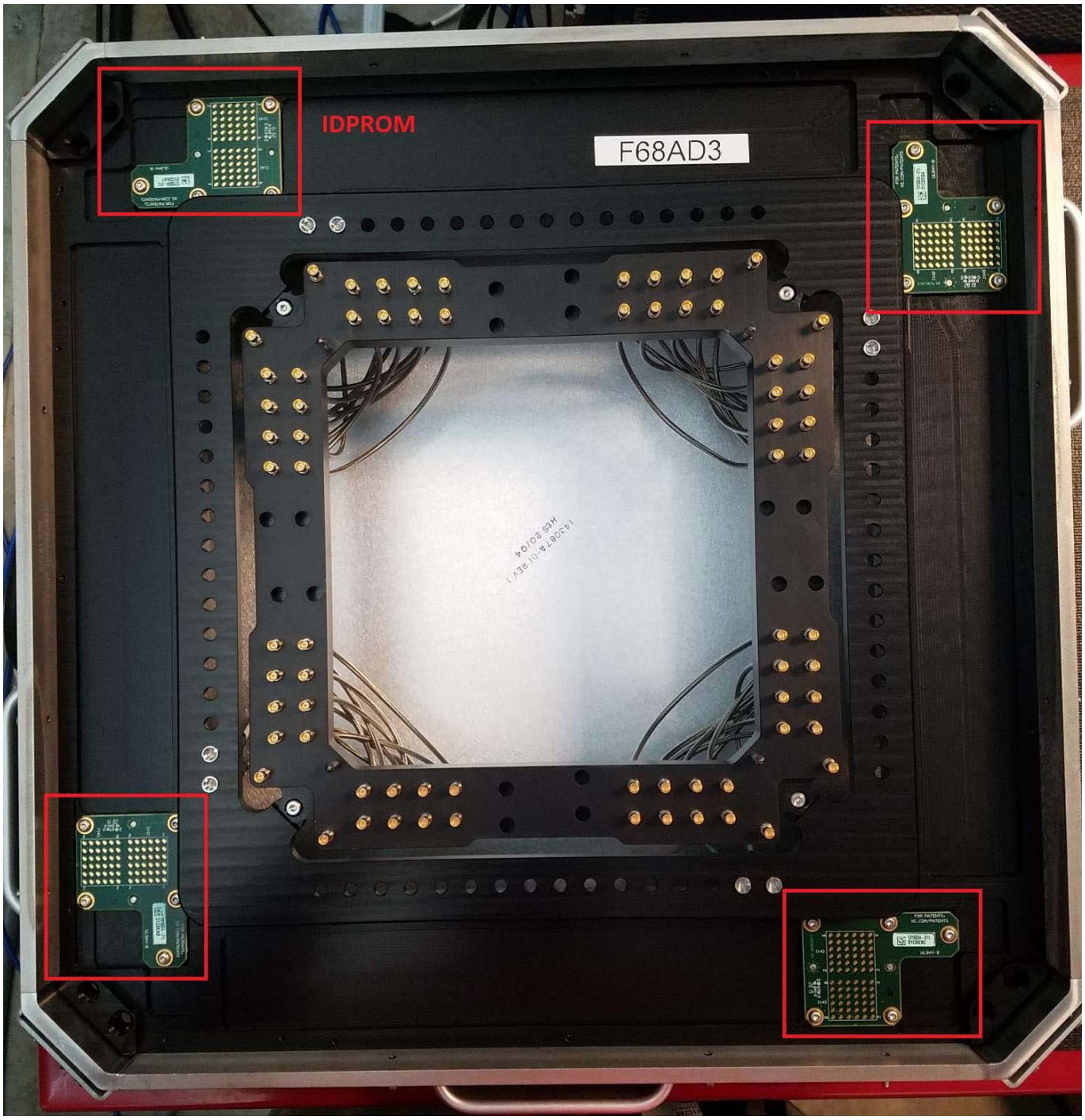

Figure 4 CCLB (bottom view) with 4 IDPROMs