Manufacturer: National Instruments

Board Assembly Part Numbers (Refer to Procedure 1 for identification procedure)**:**

Part Number and Revision	Description
131090B-43L or later	sbRIO-9609
131090B-03L or later	sbRIO-9608
131093A-01L or later	sbRIO-9603
148808B-22L or later	sbRIO-9628
131085B-43L or later	sbRIO-9629
148808B-12L or later	sbRIO-9638

Volatile Memory

Target Data	*Type*	*Size*	*Battery Backup*	*User[1] Accessible*	*System Accessible*	*Sanitization Procedure*
System memory	SDRAM	1 GB (9603/08/28) 2 GB (9609/29/38)	No	Yes	Yes	Cycle Power
LabVIEW and user data	FPGA	Xilinx XC7A75T (9603) XC7A100T (9628/38) XC7A200T (9608/09/29)	No	Yes	Yes	Cycle Power
CPLD memory	CPLD	Lattice LCMXO3-4300E (9603/08/09) LCMXO3-6900E (9628/29/38)	No	No	Yes	Cycle Power
Real-time clock	SoC RTC	242 Bytes	Yes	Yes	Yes	Procedure 2
ASIC firmware	RAM	8 MB	No	No	Yes	Cycle Power

Non-Volatile Memory (*incl. Media Storage*)

Target Data	*Type*	*Size*	*Battery Backup*	*User Accessible*	*System Accessible*	*Sanitization Procedure*
Primary storage	Disk-on-Chip	4 GB	No			
• Safe mode				No	Yes	None
• Operating system				No	Yes	Procedure 3
• User data				Yes	Yes	Procedure 3
FPGA storage	Flash	4MB (9603/28/38) 16 MB (9608/09/29)	No			
• FPGA firmware				No	Yes	None
• User FPGA VI bitstream				Yes	Yes	Procedure 4
General logic	CPLD	Lattice LCMXO3-4300E (9603/08/09) LCMXO36900E (9628/29/38)	No	No	Yes	None

[1] Refer to *Terms and Definitions* section for clarification of *User* and *System Accessible*

ASIC firmware	Flash	1 MB	No	No	Yes	None
Ethernet firmware	NVM	512 kB	No	No	Yes	None
USB Firmware	Flash	1 MB	No	No	Yes	None
DDR SPD EEPROM	EEPROM	256 Bytes	No	No	Yes	None
BIOS firmware	Flash	8 MB	No	No	Yes	None
Onboard analog input configuration	EEPROM	1 KB (9628/29/38) None (9603/08/09)	No			
• Calibration metadata				Yes No	Yes Yes	Procedure 5 None
• Calibration data[2]				No	Yes	None
Device information						
Onboard analog output configuration	EEPROM	1 KB (9628/29/38) None (9603/08/09)	No			
• Calibration metadata				Yes No	Yes Yes	Procedure 5 None
• Calibration data[2]				No	Yes	None
Device information						

[2] Calibration constants that are stored in device EEPROMs include information for the device's full operating range. Calibration constants do not maintain any unique data for specific configurations at which the device is used unless otherwise specified.

Procedures

Procedure 1 – Board Assembly Part Number identification:
To determine the Board Assembly Part Number and Revision, check the sticker on the top of the Ethernet connector. The Assembly Part Number should be formatted as 131090a-43L, where 'a' is the letter revision of the assembly (e.g. A, B, C…).

Procedure 2 – SoC RTC RAM (Real-Time Clock Data):
The battery-backed Real-Time Clock data can be cleared from the SoC RTC RAM by removing the battery from the BTH1 battery holder, and removing any voltage present on the VBAT pin through the RMC connector.
To clear the Real-Time Clock data, perform the following steps:

1. Disconnect power from the cRIO controller.
2. Locate the BTH1 battery holder on the opposite end but same side of the board as the power connector.
3. Remove the battery.
4. With the battery removed, remove any voltage present on the VBAT pin of the RMC connector for more than 1 second.

Procedure 3 – Primary Storage Disk-on-Chip (OS and User Data):
The Primary Storage DoC can be reformatted to clear the OS and User Data areas. The format operation is a "quick format" that re-initializes the file table, thereby making the existing files inaccessible. Format the drive for this NI Linux Real-Time target by performing one of the following steps:

1. Right-click the controller in MAX and click on "Format Drive".
2. Issue the nisystemformat command via a serial console local connection or SSH remote connection. Visit ni.com/info and enter the info code *format* for details.
3. Write a LabVIEW program that invokes the Format VI of the System Configuration API for the controller

Procedure 4 – FPGA Storage Flash (User FPGA Bitstream):
The User FPGA Bitstream in the FPGA Storage Flash can be cleared using NI-RIO Device Setup. To clear the bitstream from the flash, perform the following steps:

1. Add the cRIO target to your LabVIEW project by right-clicking on the project and selecting "New » Targets and Devices" and selecting your cRIO.
2. Right-click on the FPGA project item and select RIO Device Setup.
3. In the *Advanced* section, select *Erase Bitfile on Flash*.

Procedure 5 – Onboard Analog Input and Analog Output Configuration Calibration Data:
The user-accessible areas of the Device Configuration EEPROM are exposed through a calibration Applications Programming Interface (API) in LabVIEW. Go to www.ni.com/info and enter info code DAQmxLOV for instructions on how to change the calibration password and clear the user-accessible information.

Terms and Definitions

Cycle Power:
The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

Volatile Memory:
Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application specific data such as capture waveforms.

Non-Volatile Memory:
Power is not required to maintain the stored information. Device retains its contents when power is removed. This type of memory typically contains information necessary to boot, configure, or calibrate the product or may include device power up states.

User Accessible:
The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

System Accessible:
The component is read and/or write addressable from the host without the need to physically alter the product.

Clearing:
Per *NIST Special Publication 800-88 Revision 1*, "clearing" is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

Sanitization:
Per *NIST Special Publication 800-88 Revision 1*, "sanitization" is a process to render access to "Target Data" on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.