**Manufacturer:** National Instruments

**Board Assembly Part Numbers** (Refer to Procedure 1 for identification procedure)**:**

| Part Number and Revision | Description |
|---|---|
| **145051A-11L or later** | **cRIO-9048 (TPM)** |

## Volatile Memory

| *Target Data* | *Type* | *Size* | *Battery Backup* | *User[1] Accessible* | *System Accessible* | *Sanitization Procedure* |
|---|---|---|---|---|---|---|
| System memory | DDR3-SDRAM | 2 GB | No | Yes | Yes | Cycle Power |
| LabVIEW and user data | FPGA | Xilinx XC7K160T | No | Yes | Yes | Cycle Power |
| CPLD memory | CPLD | Lattice LCMXO2-4000 | No | No | Yes | Cycle Power |
| Real-time clock | SoC RTC RAM | 242 B | Yes | Yes | Yes | Procedure 2 |

## Non-Volatile Memory (*incl. Media Storage*)

| *Target Data* | *Type* | *Size* | *Battery Backup* | *User Accessible* | *System Accessible* | *Sanitization Procedure* |
|---|---|---|---|---|---|---|
| Primary storage | Disk-on-chip | 8 GB | No | | | |
| • Safe mode | | | | No | Yes | None |
| • Operating system | | | | No | Yes | Procedure 3 |
| • User data | | | | Yes | Yes | Procedure 3 |
| FPGA storage | On-chip | 4 MB | No | | | |
| • FPGA Firmware | | | | No | Yes | None |
| • User FPGA VI Bitstream | | | | Yes | Yes | Procedure 4 |
| General logic | CPLD | Lattice LCMXO2-4000 | No | No | Yes | None |
| Ethernet firmware | NVM | 1 MB | No | No | Yes | None |
| USB firmware | FLASH | 1 MB | No | No | Yes | None |
| DDR SPD EEPROM | EEPROM | 250 B | No | No | Yes | None |
| BIOS firmware | FLASH | 16 MB | No | No | Yes | None |
| TPM firmware | FLASH | 2 kB | No | No | Yes | None |
| TPM storage | FLASH | 32 kB | No | Yes | Yes | Procedure 5 |

[1] Refer to *Terms and Definitions* section for clarification of *User* and *System Accessible*

## Procedures

**Procedure 1 – Board Assembly Part Number identification:**
To determine the Board Assembly Part Number and Revision, refer to the label applied to the surface of your product. The Assembly Part Number should be formatted as "P/N: 145051a-11L", where "a" is the letter of the revision of the assembly (e.g., A, B, C…).

**Procedure 2 - System-on-Chip RTC RAM (Real-Time Clock Data):**
To clear the battery-backed System-on-Chip RTC RAM Real-Time Clock Data, complete the following steps:

1. Disconnect power from the cRIO controller.
2. Locate the CMOS reset button in the center of the cRIO backplane.
3. Press the CMOS reset button and hold it for 1 second.

**Procedure 3 - Primary Storage Disk-on-Chip (OS and User Data):**
The Primary Storage Disk-on-Chip can be reformatted to clear the OS and User Data areas. The format operation is a "quick format" that re-initializes the file table, thereby making the existing files inaccessible. Format the drive for the NI Linux Real-Time target by performing one of the following steps:

1. Right-click on the controller in NI-MAX and select "Format Drive".
2. Issue the nisystemformat command via a serial console local connection or SSH remote connection. Visit ni.com/info and enter the info code *format* for details.

**Procedure 4 – FPGA Storage Flash (User FPGA and Bitstream):**
The User FPGA Bitstream in the FPGA Storage Flash can be cleared using NI-RIO Device Setup. To clear the bitstream from the flash, perform the following steps:

1. Add the cRIO target to your LabVIEW project by right-clicking on the project and selected New » Targets and Devices and selecting your cRIO.
2. Right-click on the FPGA project item and select RIO Device Setup.
3. In the *Advanced* section, select *Erase Bitfile on Flash.*

**Procedure 5 – TPM Storage Flash:**
The user-accessible areas of the TPM Storage Flash may be cleared by completing the following steps:

1. While booting up the device, press "Delete" to enter the BIOS menu.
2. Navigate to the *Advanced* tab and select *Trusted Computing*.
3. Navigate to *Pending Operation* and select *TPM Clear*.
4. Return to the main BIOS menu and select *Save changes and exit*.
5. Restart the device for the changes to take effect.

## Terms and Definitions

**Cycle Power:**
The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

**Volatile Memory:**
Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application specific data such as capture waveforms.

**Non-Volatile Memory:**
Power is not required to maintain the stored information. Device retains its contents when power is removed. This type of memory typically contains information necessary to boot, configure, or calibrate the product or may include device power up states.

**User Accessible:**
The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

**System Accessible:**
The component is read and/or write addressable from the host without the need to physically alter the product.

**Clearing:**
Per *NIST Special Publication 800-88 Revision 1*, "clearing" is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

**Sanitization:**
Per *NIST Special Publication 800-88 Revision 1*, "sanitization" is a process to render access to "Target Data" on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.