Manufacturer: National Instruments

Board Assembly Part Numbers (PXI-5620 DIGITIZERS)

Part Number and Revision	Description
185701C-01 to 185701H-01	**PXI-5620 IF DIGITIZER, 16MS**
185701F-21	**PXI-5620 IF DIGITIZER, 16MS**
185701C-02 to 185701H-02	**PXI-5620 IF DIGITIZER, 32MS**
185701F-22	**PXI-5620 IF DIGITIZER, 32MS**

Volatile Memory

Target Data	*Type*	*Size*	*Battery Backup*	*User[1] Accessible*	*System Accessible*	*Sanitization Procedure*
Waveform Data	SDRAM	32 MB (-01/-21) 64 MB (-02/-22)	No	Yes	Yes	Cycle Power
DMA Scratch RAM	SRAM	32 KB	No	No	Yes	Cycle Power
Data Path FPGA	FPGA Block RAM	5 KB	No	No	Yes	Cycle Power
Data Path FPGA	LUTRAM	4.8 KB	No	No	Yes	Cycle Power
DRAM Control FPGA 1	FPGA Block RAM	4 KB	No	No	Yes	Cycle Power
DRAM Control FPGA 1	LUTRAM	3 KB	No	No	No	Cycle Power
DRAM Control FPGA 2	FPGA Block RAM	4 KB	No	No	Yes	Cycle Power
DRAM Control FPGA 2	LUTRAM	3 KB	No	No	No	Cycle Power

Non-Volatile Memory (*incl. Media Storage*)

Target Data	*Type*	*Size*	*Battery Backup*	*User Accessible*	*System Accessible*	*Sanitization Procedure*
Device calibration	EEPROM	4 KB	No			
• Calibration data[2]				Yes	Yes	Procedure 2
• Calibration metadata				Yes	Yes	Procedure 3
FPGA and PCI PHY configuration	EEPROM	8 KB	No	No	Yes	None
Board Control PLD	On-Chip	XC95288XL	No	No	No	None
FPGA Programming ROM	EEPROM	128 KB	No	No	No	None

[1] Refer to *Terms and Definitions* section for clarification of *User* and *System Accessible*
[2] Calibration constants that are stored on the device include information for the device's full operating range. Any implications resulting from partial self-calibration can be eliminated by running the full self-calibration procedure.

Board Assembly Part Numbers ((PXI-5620 IF DIGITIZERS)):

Part Number and Revision	Description
185701J-01L or later	**PXI-5620 IF DIGITIZER, 16MS**
185701J-02L or later	**PXI-5620 IF DIGITIZER, 32MS**

Volatile Memory

Target Data	*Type*	*Size*	*Battery Backup*	*User[1] Accessible*	*System Accessible*	*Sanitization Procedure*
Waveform Data	SDRAM	32 MB (-01) 64 MB (-02)	No	Yes	Yes	Cycle Power
DMA Scratch RAM	SRAM	32 KB	No	No	Yes	Cycle Power
Data Path FPGA	FPGA Block RAM	5 KB	No	No	Yes	Cycle Power
Data Path FPGA	LUTRAM	4.8 KB	No	No	Yes	Cycle Power
DRAM Control FPGA 1	FPGA Block RAM	5 KB	No	No	Yes	Cycle Power
DRAM Control FPGA 1	LUTRAM	4.8 KB	No	No	No	Cycle Power
DRAM Control FPGA 2	FPGA Block RAM	5 KB	No	No	Yes	Cycle Power
DRAM Control FPGA 2	LUTRAM	4.8 KB	No	No	No	Cycle Power

Non-Volatile Memory (*incl. Media Storage*)

Target Data	*Type*	*Size*	*Battery Backup*	*User Accessible*	*System Accessible*	*Sanitization Procedure*
Device calibration	EEPROM	4 KB	No			
• Calibration data[2]				Yes	Yes	Procedure 2
• Calibration metadata				Yes	Yes	Procedure 3
FPGA and PCI PHY configuration	EEPROM	8 KB	No	No	Yes	None
Board Control PLD	On-Chip	XC95288XL	No	No	No	None
FPGA Programming ROM	EEPROM	128 KB	No	No	No	None

[1] Refer to *Terms and Definitions* section for clarification of *User* and *System Accessible*
[2] Calibration constants that are stored on the device include information for the device's full operating range. Any implications resulting from partial self-calibration can be eliminated by running the full self-calibration procedure.

Procedures

Procedure 1 – Board Assembly Part Number Identification:
To determine the Board Assembly Part Number and Revision, refer to the label applied to the surface of your product. The Assembly Part Number should be formatted as "185701#-xx" or "185701#-xxL" where "#" is the letter module revision and "xx" is a two-digit numeric specifying variant information. Any part number shown in the Board Assembly Part Numbers tables are applicable to this document.

Procedure 2 - Device Calibration EEPROM (Calibration Data):
The user-accessible areas of the Calibration EEPROM are exposed through the NI-SCOPE Applications Programming Interface (API). User-accessible fields can be fetched or stored using this API which makes it convenient to store device calibration to a file for later restoration. Full external calibration can be run using *Calibration Executive for Traditional DAQ Version 3.5.2* which also requires additional equipment. This API allows the user to perform the following calibrations, which re-write the stored calibration constants:

a. VCXO Tuning Serial DAC
b. DDC Frequency Response
c. DDC ADC Voltage Gain and Offset

There are two options for clearing the calibration data. Either backup known-good values prior to use and restore the known-good values after use (Option 1), or overwrite the values with zeros (which requires a full external calibration to restore the device to operation – Option 2). In an empty VI in LabVIEW, complete the steps that apply to the desired option:

1. Open an NI-SCOPE calibration session using the niScope Cal Start VI. The "password" input must be configured to match the existing password value stored in the EEPROM.
2. (Option 1) To backup calibration data for later restoration:
    a. VCXO Tuning Serial DAC calibration data: use the niScope Cal Get Serial Dac Eeprom VI to fetch the DAC voltage and store to file.
    b. DDC Frequency Response calibration data: use the niScope Cal Get FR Eeprom VI to fetch the calibration data array and store to file.
    c. DDC ADC Voltage Gain and Offset calibration data: use the niScope Cal Get Adc Voltage Eeprom VI to fetch offset and gain information and store to file.
3. (Option 1) To restore calibration data from backup:
    a. VCXO Tuning Serial DAC calibration data: use the niScope Cal Set Serial Dac Eeprom VI and wire the "dacCalVolts" input of the VI to the data to restore.
    b. DDC Frequency Response calibration data: use the niScope Cal Set FR Eeprom and wire the "Polynomial Fit Coefficients" input of the VI to the data to restore.
    c. DDC ADC Voltage Gain and Offset calibration data: use the niScope Cal Set Adc Voltage Eeprom VI and wire the "adcVoltageGain" and "adcVoltageOffset" inputs of the VI to the data to restore.
4. (Option 2) To overwrite calibration data with zeros:
    a. VCXO Tuning Serial DAC calibration data: use the niScope Cal Set Serial Dac Eeprom VI and wire the "dacCalVolts" input of the VI to a zero constant.
    b. DDC Frequency Response calibration data: use the niScope Cal Set FR Eeprom and wire the "Polynomial Fit Coefficients" input of the VI to a 16-element array of zeros.
    c. DDC ADC Voltage Gain and Offset calibration data: use the niScope Cal Set Adc Voltage Eeprom VI and wire the "adcVoltageGain" and "adcVoltageOffset" inputs of the VI to a zero constant.
5. Close the NI-SCOPE session using the niScope Cal End VI. The "action" input should be configured to "Abort Calibration" as the calibration EEPROM data is committed in the previous steps.

Procedure 3 - Device Calibration EEPROM (Calibration Metadata):
The user-accessible areas of the Calibration EEPROM are exposed through the NI-SCOPE Applications Programming Interface (API). To clear the calibration metadata, complete the following steps in an empty VI and run in LabVIEW:

1. Open an NI-SCOPE calibration session using the niScope Cal Start VI. The “password” input must be configured to match the existing password value stored in EEPROM.
2. To clear the calibration password:
    a. Specify the current password in the “old password” input of the niScope Cal Change Password VI. Note that the default factory password is “NI” (excluding quotes).
    b. Wire the string “NI” (excluding quotes) to the “new password” input of the niScope Cal Change Password VI. This resets the password to the default factory password.
3. To clear the user-defined information:
    a. Wire the “miscellaneous information” input of the niScope Cal Store Misc Info VI to an Empty String constant. For PXI-5620 and PXI-5621 devices, the user input string is appended with empty characters such that the entire memory space dedicated to the user-defined information is overwritten.
4. Close the NI-SCOPE session using the niScope Cal End VI. The “action” input must be configured to “Store Calibration” for the user-defined information field in EEPROM to be cleared.

Terms and Definitions

Cycle Power:
The process of completely removing power from the device and its components and allowing for adequate discharge. This process includes a complete shutdown of the PC and/or chassis containing the device; a reboot is not sufficient for the completion of this process.

Volatile Memory:
Requires power to maintain the stored information. When power is removed from this memory, its contents are lost. This type of memory typically contains application specific data such as capture waveforms.

Non-Volatile Memory:
Power is not required to maintain the stored information. Device retains its contents when power is removed. This type of memory typically contains information necessary to boot, configure, or calibrate the product or may include device power up states.

User Accessible:
The component is read and/or write addressable such that a user can store arbitrary information to the component from the host using a publicly distributed NI tool, such as a Driver API, the System Configuration API, or MAX.

System Accessible:
The component is read and/or write addressable from the host without the need to physically alter the product.

Clearing:
Per *NIST Special Publication 800-88 Revision 1*, "clearing" is a logical technique to sanitize data in all User Accessible storage locations for protection against simple non-invasive data recovery techniques using the same interface available to the user; typically applied through the standard read and write commands to the storage device.

Sanitization:
Per *NIST Special Publication 800-88 Revision 1*, "sanitization" is a process to render access to "Target Data" on the media infeasible for a given level of effort. In this document, clearing is the degree of sanitization described.