PXIe-3352
Rubidium/GPS Frequency Standard
User Manual

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FOR YOUR SAFETY

Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an autotransformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.

Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.
2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until performance is checked by qualified personnel.

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DOCUMENT CHANGE HISTORY

Revision	Date	Description of Change
A	4/20/2017	Initial Astronics Test Systems release
B	5/16/2017	ECN08282. Revised to correct Ext PWR connector size. Added theory of operation/functional description to Chapter 1.

Chapter 1
Overview and Features

The PXIe-3352 (Figure 1-1) is a Rubidium/GPS module for use in PXI hybrid and PXI Express slots in a PXI mainframe. It provides a basic accuracy of $5e^{-11}$ in free-run mode, but, given an external GPS antenna (not included) and a view of the sky, can be disciplined to GPS satellites for improved timing accuracy.

The PXIe-3352 can be used in a wide variety of applications where a precision oscillator source is required. In addition, the onboard global position unit(GPS) can be used to train and discipline the precision oscillator source.

Figure 1-1, PXIe-3352

Functional Description

PXIe-3552 contains a rubidium-based oscillator and GPS timing module. Although calibrated before the shipping from the factory, the rubidium-based oscillator can be disciplined and calibrated by the GPS module when needed. All controls are via the PXIe bus in a PXIe compatible mainframe.

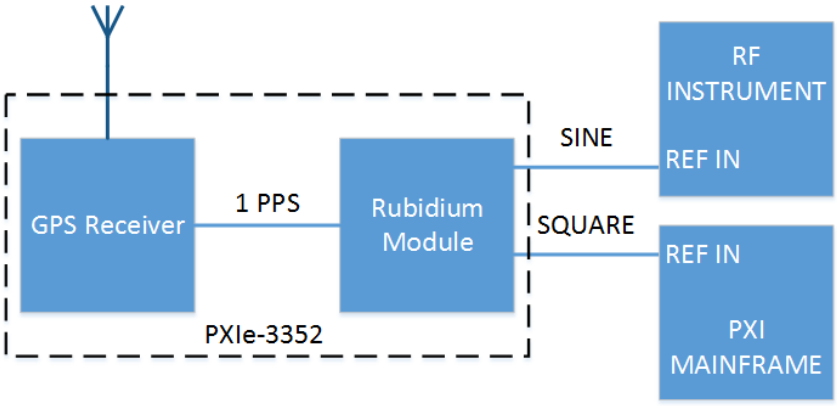

Figure 1-2, PXIe-3352 System Configuration Example

The PXIe-3352 card comprises three functional systems as follows:

- The Rubidium Block
- The GPS Block
- The Digital Controller

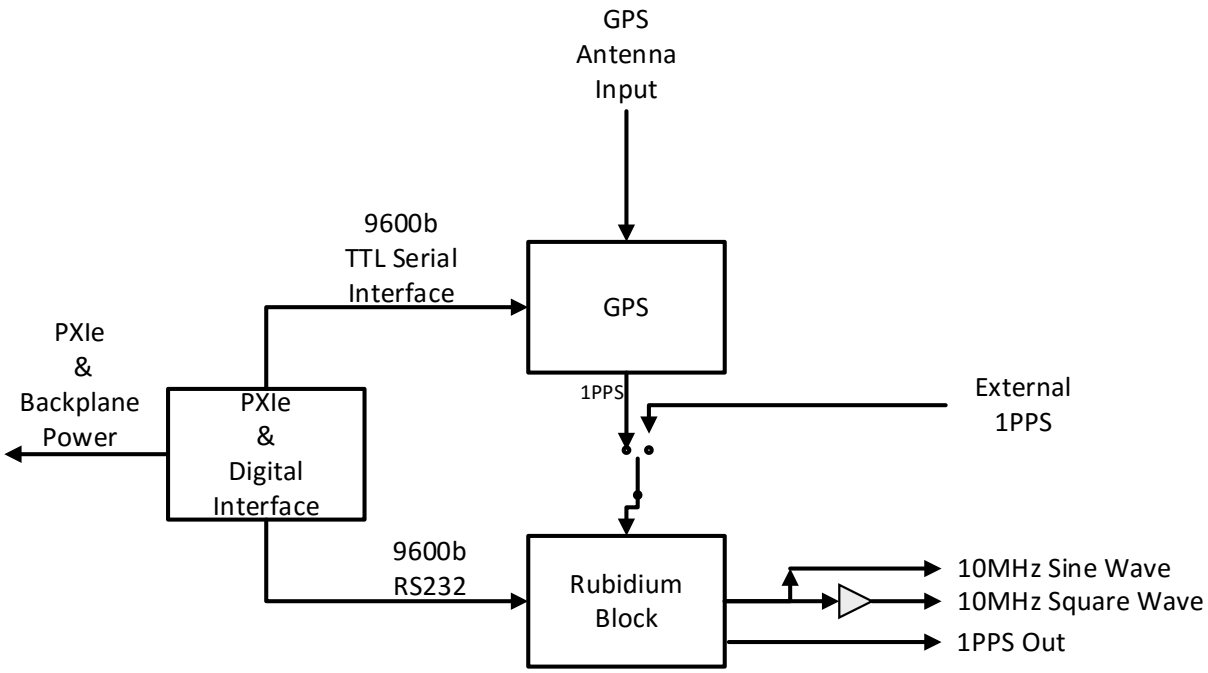

Figure 1-3, PXIe-3352 Functional Systems

Rubidium Block

The major component of the PXIe-3352 is the Rubidium block. The Rubidium block is a multifunctional Rubidium Frequency Standard. It is one of the smallest atomic clock standards currently available, where the accuracy and stability are derived from a quantum energy transition that occurs in a free Rubidium atom.

The unit utilizes a unique advanced technology that allows a reduction in size without sacrificing performance. The standard unit provides outputs of 10MHz and 1PPS.

The Rubidium is comprised of a unique DFLL (Digital Frequency Lock Loop), where a high performance crystal oscillator is locked to the Rubidium atomic line using an embedded microprocessor and a special patented algorithm. The algorithm improves temperature stability and enables very fine digital frequency control.

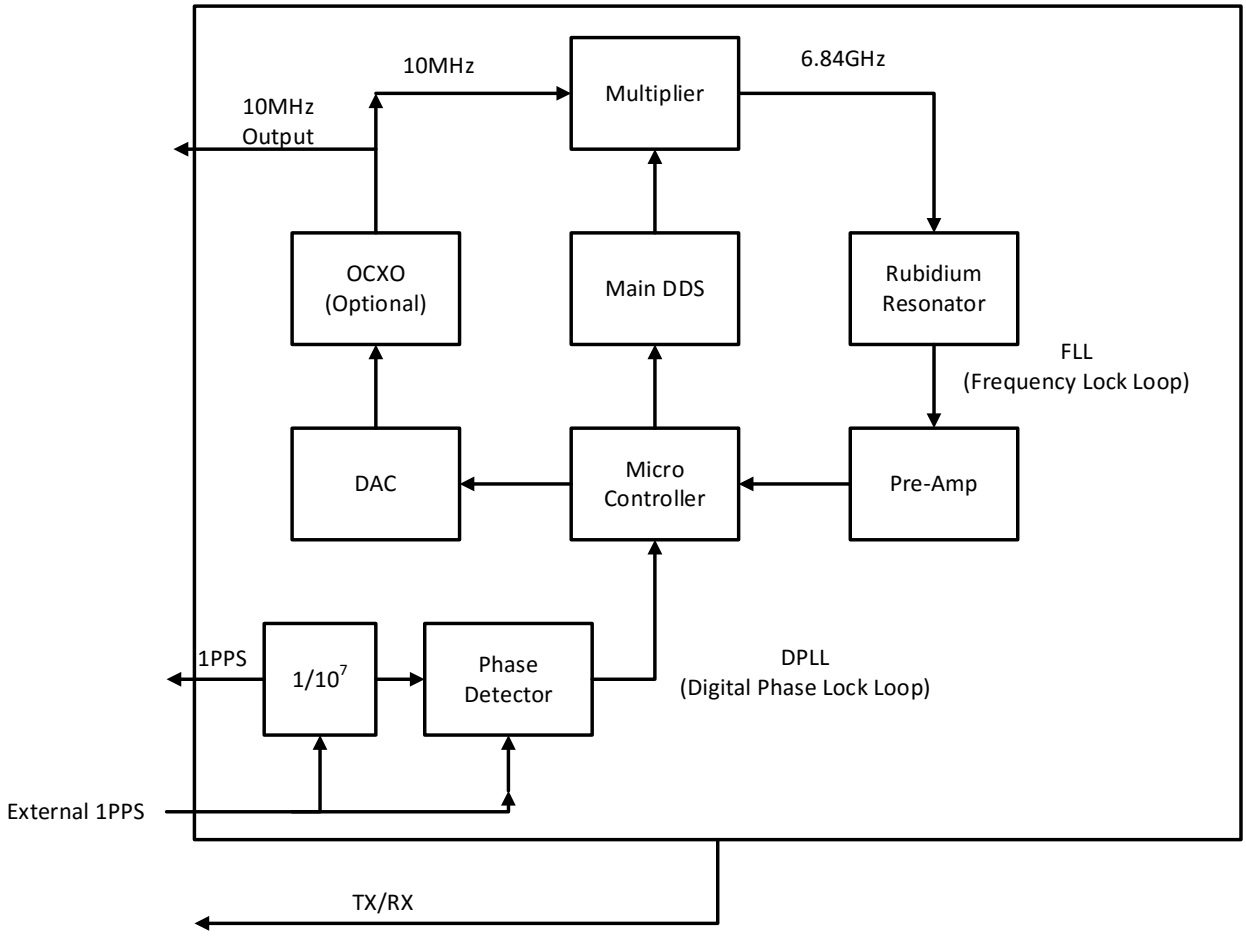

Figure 1-4, Rubidium Oscillator Block Diagram

The Physics Package ("Rubidium Resonator" in Figure 1-4) includes a lamp, subassembly, a cavity subassembly, a "C-Field" coil, and a double magnetic shield. The lamp is RF-discharged: a Rb87 lamp that emits a light that is directed into the cavity subassembly. The light is filtered by a Rb85 filter cell, transmitted

through a Rb87 resonance cell, and finally detected by a photo-diode detector. The resonance cell is located inside the microwave cavity.

A Step Recovery Diode (SRD), located in the cavity generates a nominal frequency of 90 MHz.

When this frequency deviates from the precise Rb87 resonance frequency, the photo-diode senses a change in the light transmitted through the resonance cell. This change is amplified by the preamplifier and used to control the OCXO.

The atomic resonance frequency, however, is sensitive to external magnetic fields. Therefore, a double magnetic shield is used to attenuate external fields by a factor of about 5000. The “CField” coils set the magnetic field. Controlling the current via this coil enables the analog frequency adjustments that were described before.

When GPS satellites are not available, the system performance reverts to that of a stand-alone Rubidium. (This period is called the Holdover Period.)

RS232 Interface

The Rubidium block also includes electronics boards that control the unit’s operation and RS232 interface to communicate with electronics outside of the unit.

GPS Block

The GPS block is a self-contained high performance Global Position System receiver. It can simultaneously acquire on 66 channels and track on up to 22 channels. The main purpose of the GPS block is to provide a GPS based 1 PPS output to train and discipline the Rubidium oscillator. This technique results in improved long-term stability comparable to that of a Cesium-frequency standard. The GPS block requires a 3.3 VDC lithium battery in order to retain the positioning lock data during power down. Without a 3.3 VDC lithium battery present, the GPS cannot function.

Control of the Rubidium oscillator is available to enable or disable outputs or to query it for information such as serial number, operating hours, operating temperature, event history, self-test, and other performance indicators.

PXIe and Digital Interface

The PXIe interface allows the FPGA to communicate data and commands between the PXIe chassis and the PXIe-3352. The FPGA then translates the data and commands via 9600 baud rate TTL serial to the GPS IC and via 9600 baud rate RS-232 to the Rubidium block.

External DC Power Supported

If the PXI mainframe is powered down, power may still be applied to the Rubidium oscillator via a front panel external DC power input. This keeps the Rubidium oscillator very stable over time and eliminates the effects of retrace. The GPS receiver maintains its location information during power down, saving the time it takes for the receiver to do a position fix, because it has an internal battery to power its SRAM and real time clock.

Front Panel

Connectors:

Connector	Connector Type	Reference Designator	Description
Sine WAVE OUT	SMA	J1	Rubidium Module Sine Wave Out
SQ WAVE OUT	SMA	J2	Rubidium Module Square Wave Out
1PPS IN	SMA	J3	External 1 PPS Input
1PPS OUT	SMA	J4	1 PPS Output from Rubidium Module
GPS ANT	SMA	J5	External GPS Antenna Input
Ext PWR	DC Jack 2.5 mm ID 5.5 mm OD	J6	External +12 VDC @1.5 A Center Positive for Rubidium Module

LED Indicators

LED	Indication
FAIL	Unit failure
ACC	PXIe access
LOCK	Rubidium Module Output Frequency Locked

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Chapter 2
Specifications

Output Characteristics

Output Frequency

- 10 MHz

Output Channels

- Sinewave Output Channel
- Squarewave (CMOS) Output Channel

Amplitude

- Sine Wave: 10 dBm ± 2 dBm into 50 Ω
- CMOS: 2.5 V into 10 kΩ

Phase Noise (sine output)

- 10 Hz offset: -102 dBc/Hz
- 100 Hz offset: -135 dBc/Hz
- 1 kHz offset: -145 dBc/Hz
- 10 kHz offset: -150 dBc/Hz

Spectral Purity (sine output)

- Harmonics: <-44 dBc (up to 70 MHz)
- Spurious: <-80 dBc (10 Hz-100 kHz from carrier)

Timebase Characteristics

Initial Accuracy (@ 25° C)

- 5×10^{-11}

Stability

- Frequency Drift: 5×10^{-11}/month
- Frequency Retrace: $< 5 \times 10^{-11}$
- Allan Variance (1 s): 3×10^{-11}
- Allan Variance (100 s): 5×10^{-12}

Warm Up (@ 25° C)

- <4 minutes to lock
- <5 minutes to reach 5 x 10^{-10}

Receiver Architecture

- Tracking: 22 parallel channels
- Acquisition: 66 simultaneous satellites

Operating Frequency

- L1 (1575.42 MHz), C/A code

Receiver Sensitivity (typical)

- Tracking: -161 dBm
- Cold Start: -143 dBm

Timing Accuracy (1 pps)

- ± 11 ns

Acquisition Time

- Hot: <1 s, typical
- Warm: <30 s, typical
- Cold: <32 s, typical

Interface

Power Requirements

- +3.3 VDC at 1.2 A
- +12 VDC at 2.5 A

Front Panel I/O and Indicators

Outputs (SMA)

- Sine Wave: 10 MHz, 10 dBm, 50 Ω
- Square Wave: 10 MHz, 2.5 V, 10 kΩ
- 1 PPS: 3.3V, pulse width <20µs

Inputs

- External Rubidium Power: 12 V @ 1.5 A
- GPS Antenna (SMA): 50 Ω
- 1 PPS (SMA): 3.3V CMOS, pulse width <10 µs

Status Lights

- Red: Sysfail

- Amber: Access
- Yellow: Rubidium locked

Software

Driver Installations

- LabWindows/CVI, 32-bit and 64-bit
- LabVIEW, 32-bit and 64-bit

Executable

- Interactive Control Soft Front Panel

Environmental

Temperature/Altitude

- Operating: 0° C to 55° C/10,000 ft
- Storage: -40° C to 75° C/15,000 ft

Relative Humidity

- 5 to 95%, non–condensing <30° C
- 5 to 75%, non–condensing <40° C

Mechanical

- Shock: 30 g, 11 ms, ½ sinewave
- Vibration: 0.013 in (pk-pk), 5 to 55 Hz
- Bench Handling: 4-inch drop at 45°

CE Certifications

- Emissions/Immunity: EN61326: 1997 + A1: 1998, Class A
- Safety: EN61010-1: 1993 + A2: 1995

MTBF (MIL-HDBK-217 FN2, GB GC, 25°)

- 35,740 hrs

Mechanical

Weight

- 1.26 lbs (0.567 kg)

Dimensions

- 2 Slot Width PXI Express Module

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Chapter 3
Getting Started

Unpacking and Inspection

WARNING

Use standard ESD procedures including ground straps and static-safe work surfaces whenever handling the PXIe-3352 module.

Remove the PXIe-3352 module and inspect it for damage. If any damage is apparent, inform the carrier immediately. Retain shipping carton and packing material for the carrier's inspection.

Verify that the pieces in the package you received contain the correct module option. Notify our Customer Support department (see front pages for contact information) if the module appears damaged in any way. Do not attempt to install a damaged module into a PXIe chassis.

The module is shipped in an anti-static bag to prevent electrostatic damage to the module. Do not remove the module from the anti-static bag unless it is in a static-controlled area.

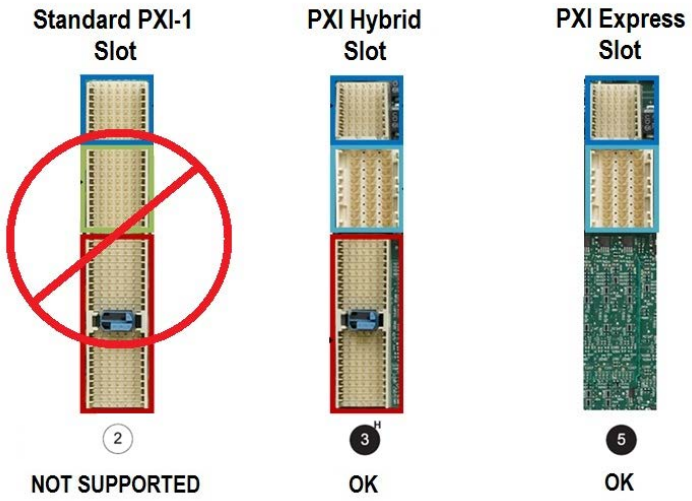
Installing the Module into a PXI Express Chassis

WARNING

The PXIe-3352 module is NOT hot-swappable. The power to the PXI Express compatible chassis must be turned off before installing a PXIe-3352. Plugging the module in before the power is off may result in damage to the electronics.

Note: The PXIe-3352 can be installed into any available PXI hybrid or Type 1 PXI Express slot as shown in the diagram below. **Do not attempt to install a PXIe-3352 into a standard PXI-1 slot.**

Slots in a PXI chassis that are legal for the PXIe-3352 are identified by a slot number inscribed within a filled circle. There can be the letter "H" for Hybrid to the upper right of the circle as well. The slot number inscribed within an un-filled circle indicates a standard PXI-1 slot, therefore installation into this slot should not be attempted at risk of damaging both the PXI backplane connector and the PXIe-3352's fabric connector. The diagram below depicts the slot types, both legal and illegal, along with slot-identifying glyphs that are found below each slot of any PXI mainframe which conforms to the PXI specification.



When inserting the module into the chassis, it should be gently rocked back and forth to seat the connectors into the backplane receptacles.

Initial Power On

1. Drivers must be installed prior to hardware installation (see ***Software Installation***).
2. Turn off the chassis power before installing the PXIe-3352.
3. Once the module is properly installed in the chassis, connect the GPS antenna to the GPS ANT connector. Make sure that there is open view to the sky or if indoors, no metal obstruction is above the antenna.
4. Turn on the chassis power.

   The FAIL LED will illuminate for ~0.5s and then turn off if the module passes the internal power on self test (POST).

   If the PXIe-3352 fails POST, the FAIL LED will continue to be illuminated. Should this happen, turn the chassis power off, re-install or make certain the PXIe-3352 is properly installed in the chassis, and turn the chassis power back on.
5. Turn on or re-start the computer connected to the chassis.
6. If this is the first time the PXIe-3352 is turned on, wait 5 minutes or until the yellow Lock LED is turned on.

Figure 3-1, Front Panel, LOCK LED

Software Installation

Prior to hardware installation of the PXIe-3352, install the following four software drivers:

1. VISA software, available from your PXI slot 0 device vendor
2. Windows PXI Device Driver (from LabVIEW driver installer)
3. LabWindows/CVI Instrument Driver (optional)
4. LabVIEW Instrument Driver (optional)

Note: *You will need system administrator priveleges to install these software items.*

Installing the VISA driver

The LabVIEW and LabWindows/CVI driver communicate with the instrument using the VISA software interface layer. The VISA software is provided by the manufacturer of your PXI controller. Obtain the VISA software from your PXI controller vendor, and follow their instructions for installing on your computer.

Installing the PXI device driver

The PXI Device Driver is included on both the LabWindows / CVI Instrument Driver Installer and the LabVIEW Instrument Driver Installer. You MUST install this driver so that the instrument will be properly recognized by Windows.

If you execute the LabVIEW Driver Installer, the PXI device driver is installed by default.

If you execute the LabWindows/CVI driver installer, the installer creates a subdirectory named “Windows Driver” inside the directory selected for installation. By default, on a 64-bit operating system, this directory will be:

C:\Program Files (x86)\IVI Foundation\VISA\WinNT\ri3352e

On a 32-bit operating system, the default would be:

C:\Program Files\IVI Foundation\VISA\WinNT\ri3352e

To install the PXI device driver:

1. Use the Windows explorer to navigate to the “Windows Driver” subdirectory.
2. Right-mouse click on the file “ri3352e.inf”.
3. Select “Install”.

Installing the LabVIEW instrument driver

1. Insert the install media (C) into your computer.
2. Navigate to the “Drivers” folder on the install media.
3. Navigate to the LabVIEW Driver folder.
4. Double-click on the file “setup.exe”.
5. The driver installer will provide you with a choice for a standard or customer installation.
   a. The standard installation will install the Windows PXI device driver for the 3352e. It will also install the driver for the version(s) of LabVIEW that is currently installed on your computer.
   b. The customer installation allows you to select which version(s) of LabVIEW for which the driver will be installed. If you are running a version of LabVIEW that is not supported by the installer, you can select an older version of driver to use. For example, if you are running LabVIEW 2013, you can install the LabVIEW 2011 version and let LabVIEW re-compile the driver when it is first used.
6. The driver installer creates a directory “Astronics ri3352e” within the “instr.lib” subdirectory of the version of LabVIEW you are using.

Installing the LabWindows/CVI instrument driver

1. Insert the install media (C) into your computer.
2. Navigate to the “Drivers” folder on the install media.
3. Select the version of the installer that meets your needs.
   a. Select the “InstallerWithRTE” folder if you do NOT have a version of the LabWindows/CVI run-time engine installed on your computer. The executable soft front panel requires the LabWindows/CVI run-time engine

to work properly.

b. Select the “InstallerWithoutRTE” folder if you already have a version of the LabWindows/CVI run-time engine installed on your computer.

4. Double-click on the file “setup.exe”.
5. Follow the command prompts, and select the destination folder for installation.
6. By default, the installer will place the files within the VISA directory structure.

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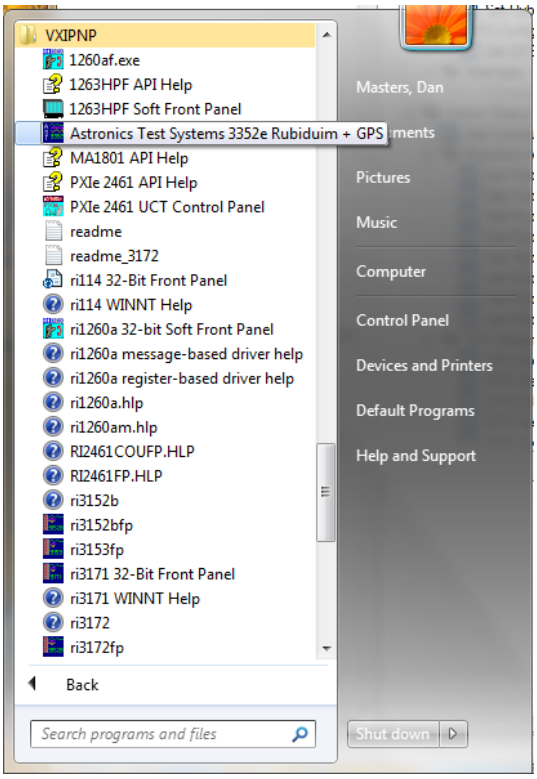
Chapter 4
Software Operation

Using the Soft Front Panel

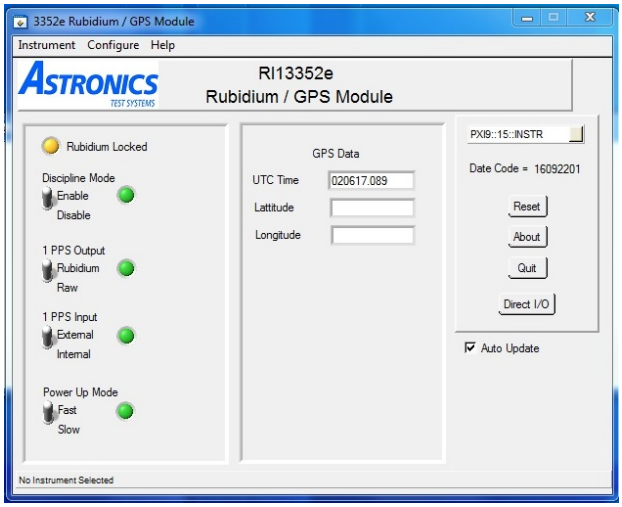
The soft front panel allows the operator interactive control over the PXIe-3352 to allow instrument operation. All major functions are provided.

Starting the Soft Front Panel

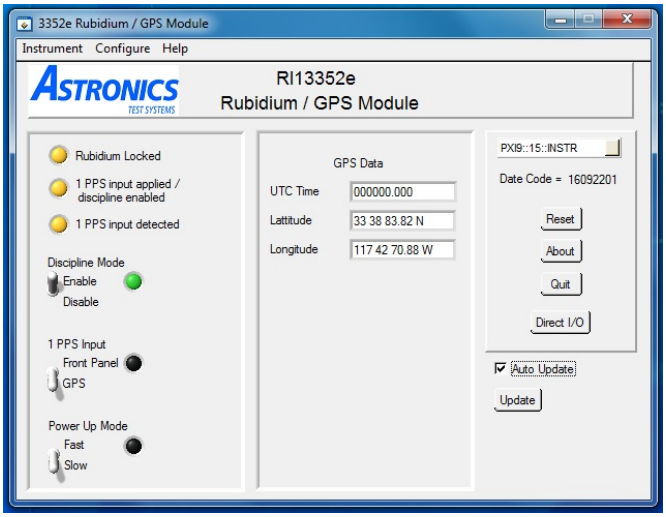
The Soft Front Panel application is installed when you install the LabWindows / CVI driver. After the Soft Front Panel is installed, you may start it by selecting "Start -> All Programs -> VXIPNP -> Astronics Test Systems 3352e Rubidium + GPS" from the task bar.



If the Rubidium has warmed up, the front panel may look like as follows. It may take up to 32 seconds to get the GPS to lock from the cold start.



GPS module is selected by dragging the Discipline Mode switch to its “ENABLE” position. Once the GPS module is locked onto a sufficient number of GPS satellites, the front panel will display the Latitude and Longitude information. At the same time, the “1PPS Input Detected” soft LED will be illuminated.



If the 1PPS Input switch is set to “GPS”, then the Rubidium module is disciplined by the GPS. Otherwise, an external 1 PPS source is required to discipline the Rubidium oscillator.

If Discipline Mode is disabled, the Rubidium oscillator will be running on its own calibrated clock source. The clock that is output from the 1PPS OUT port is always sourced by the Rubidium oscillator.

Using the LabWindows / CVI Driver

The LabWindows / CVI driver provides a 'C' language programming interface. This driver also includes a 32-bit and 64-bit DLL that can be used within various programming environments such as Microsoft Visual Studio C++ and C#.

The first step to using any of the functions in the driver is to call the "ri3352e_init()" function. This function takes the VISA descriptor that identifies which instrument is being accessed and returns a "handle". All of the other functions in the driver use this handle.

The last step in using the driver is to call the "ri3352e_close()" function. Each time you make a call to the "ri3352e_init()" function, it returns a new handle and allocates some memory for that driver session. Calling the "ri3352e_close()" functions releases the memory and resources associated with the handle.

A skeleton program will look something like what is shown below.

```
#include <ri3352e.h>

int main(int argc, char *argv[])
{
      ViSession hdl3352e;
      ViStatus err;

      // call the initialize function
      err = ri3352e_init("PXI32::15::INSTR", VI_TRUE, VI_TRUE,
                                                      &hdl3352e);

      // check the error code
      if (err < 0)
      {
            // do something / report error
            ViChar errMsg[256];
            ri3352e_error_message(hdl, err, errMsg);

            printf("ri3352e_init() returned error code %d\n", err);
            printf("error message = '%s'\n", errMsg);
            return err;
      }
```

```
        // use other functions of the driver
        // …


        // done using the driver, call ri3352e_close()
        err = ri3352e_close( hdl3352e );
}
```

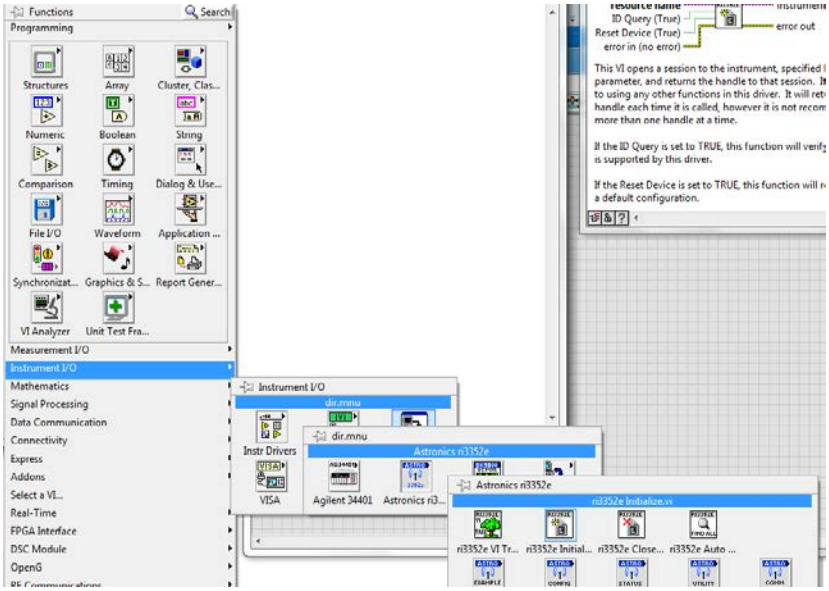
The various functions in the driver allow you to configure the Rubidium and GPS modules within the 3352e. They also provide a means to retrieve information from these modules. For detailed information on the driver, consult the help information in the help file “ri3352e.hlp” that is included with the driver.

Using the LabVIEW Driver

The LabVIEW driver provides the means to control and interact with the 3352e from within the National Instruments LabVIEW programming environment.

The first step in using any of the VIs in the LabVIEW driver is to initialize the instrument using the “ri3352e Initialize.vi”. You can select this from within a LabVIEW diagram by right-mouse clicking and selecting

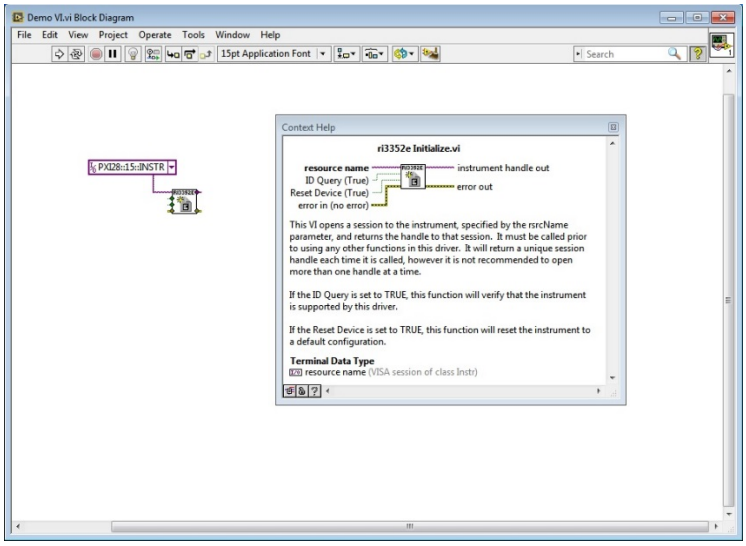
Instrument I/O -> Instr Drivers -> Astronics ri3352e ->ri3352e Initialize.vi



Once in the diagram, the VI must be supplied with the instrument descriptor for the 3352e. This will be assigned by the VISA software provided by the PXI controller. A typical instrument descriptor is “PXI28::15::INSTR”.

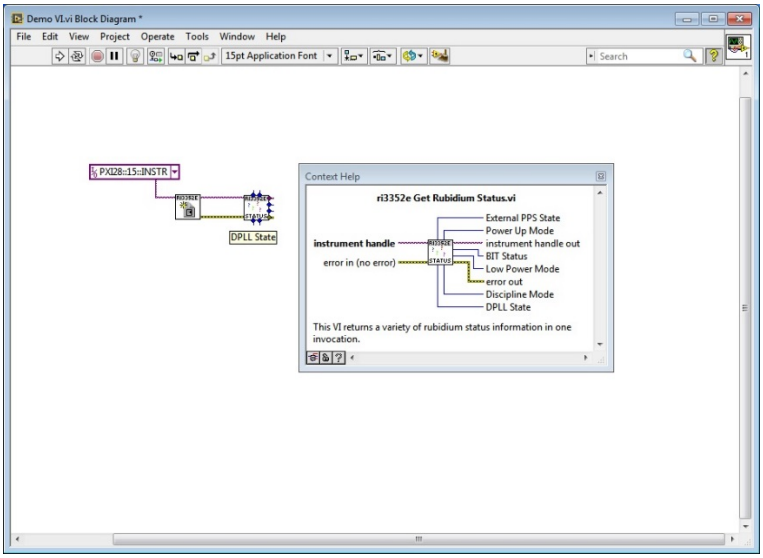
A rudimentary VI block diagram with just the ri3352e Intiialize.vi is shown below.

This VI shows that the instrument descriptor has been selected and wired into the VI.



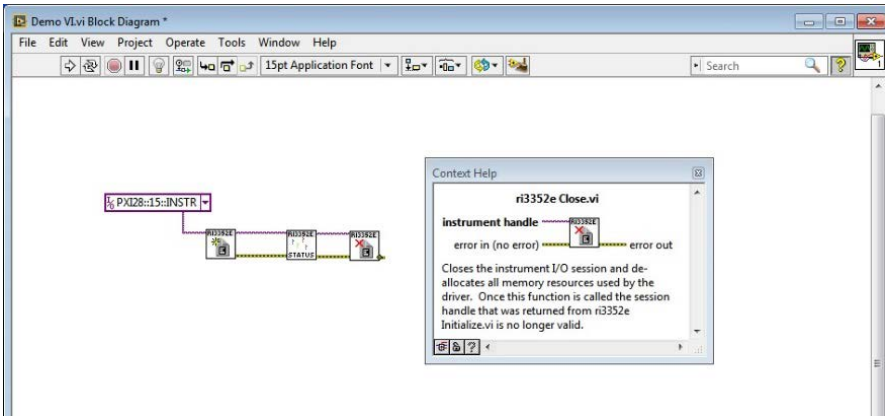
The next step is to add the various driver VIs that provide the information you need in your application. The image below demonstrates that a second VI has been added to the diagram. This VI, “ri3352e Get Rubidium Status.vi”, retrieves status information from the Rubidium module in the 3352e.

One requirement for using the driver is to wire the “instrument handle out” output from one VI to the “instrument handle” input on the next VI. A second requirement for using the driver is to wire the “error out” output from one VI to the “error in” input of the next VI. These two connections are shown in the diagram below:



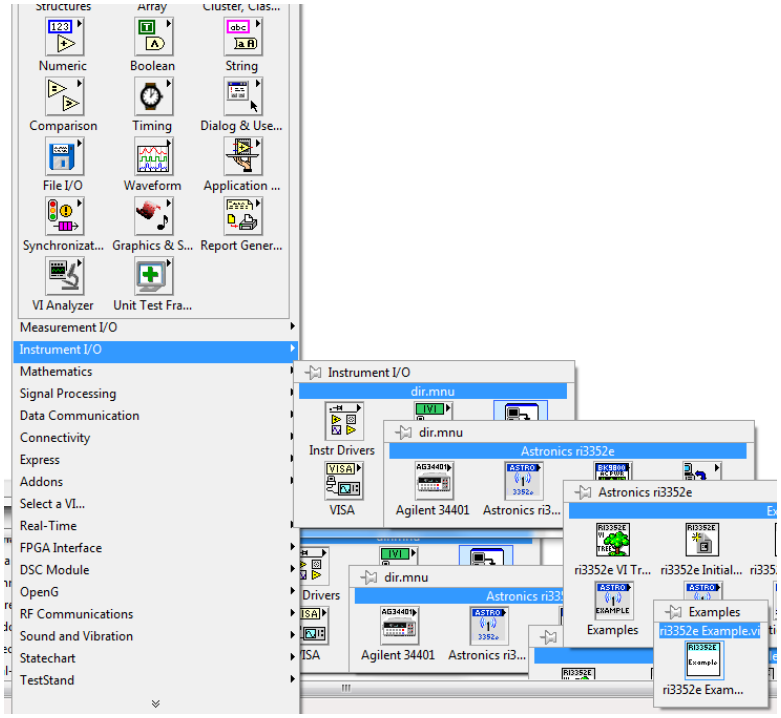
The last recommendation, as with the LabWindows/CVI driver, is that every handle you open with the “ri3352e Initialize.vi” should be closed with the “ri3352e Close.vi”. Every time you execute the “ri3352e Initialize.vi”, it opens a new handle to the instrument, and that handle allocates some memory. Repeated use of the “ri3352e Initialize.vi” without closing it via the “ri3352e Close.vi” will ultimately result in an execution error.

The use of the “ri3352e Close.vi” as the last VI in the chain is shown in the diagram below:

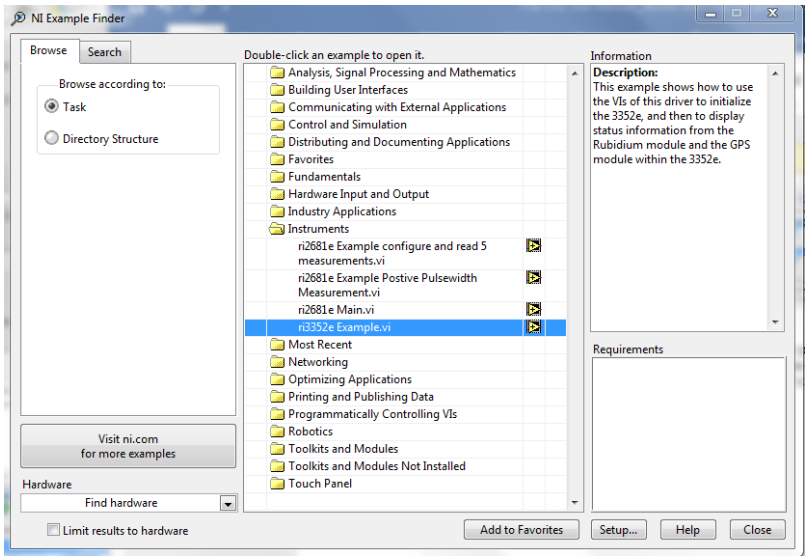


The LabVIEW driver contains an executable example VI. You can locate this in one of two ways:

Select the menu item “Instrument I/O -> Instr Drivers -> Astronics ri3352e -> Examples -> ri3352e Example”. Then open the front panel on the VI.



Alternatively, from the LabVIEW menu of any front panel, you can select “Help -> Find Examples…”. This will launch the NI Example Finder. From there, you can look under the “instruments” folder and select the “ri3352e Example.vi”



You may find full help information on the driver by selecting the “Help -> Astronics ri3352e -> ri3352e LabVIEW Help” menu item from any VI’s front panel.

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