SOLUTION
BROCHURE

Open Architecture for Communications Research

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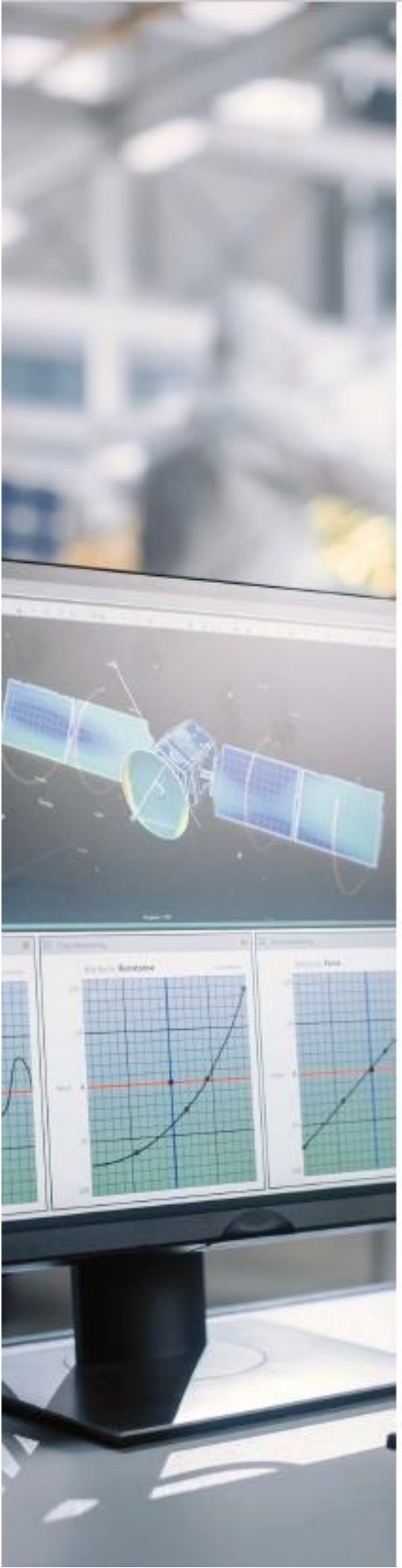

Solution Brochure

Open Architecture for Communications Research

Trends in Wireless Communications

As wireless communications systems evolve beyond 5G, expand to low-Earth orbit, and extend to new frequencies and bandwidths, researchers and systems engineers are tasked with bringing new capabilities from concept to the lab to deployment. A major obstacle on this journey is the time it takes to migrate IP from simulation to firmware, and to build up boards and infrastructure to form a testbed for assessing the real-world performance of novel algorithms, waveforms, and components. COTS software defined radios from NI with an integrated software workflow can help you develop, test, and deploy communications IP faster.

Application Requirements:

- MIMO (multiple input, multiple output) communications systems require phase coherence across all channels
- Wide bandwidth I/Q data must be streamed to a server for advanced CPU- and GPU-based processing
- Directly migrate IP from simulation to real-world hardware testing

FIGURE 01 Engineers and researchers developing communication systems benefit from software approaches that allow them to quickly transition from software simulation to prototyping hardware.

Reference Architecture Overview

The Open Architecture for Communications Research (OACR) is NI's blueprint for a system that meets key requirements of a hardware testbed for prototyping novel wireless technology. Follow NI's recommended solution to build up a MIMO research system as quickly as possible; this reference architecture has been validated by NI engineers to ensure it delivers the specified performance. Based on COTS hardware and open-source software, this solution is ideal for rapidly transitioning IP through its development lifecycle: from software simulation to proof-of-concept demonstration to tactical deployment.

Multichannel Systems

For accurate beamforming and direction finding in MIMO systems, it is necessary for the transmit (TX) and receive (RX) chains of a wireless system to be synchronized across an array. NI RF modules provide phase coherency via the sharing of local oscillators, reference clocks, and triggers.

Data Streaming

Wide bandwidth I/Q data necessitates high throughput streaming interfaces. OACR allows users to stream data across 10 gigabit ethernet (GbE) links to avoid bottlenecks in moving data from I/O to processing.

Digital Signal Processing (DSP)

Capabilities such as forward error correction, low density parity check (LDPC) decoding and encoding, turbo code decoding, digital beamforming, and zero-forcing precoding require inline processing of signals. NI incorporates Xilinx FPGAs onboard instruments like Vector Signal Transceivers and FlexRIO.

Machine Learning and Knowledge-Aided Computing

Today's cognitive radio system operates differently from yesterday's. And tomorrow's will operate differently from today's. That's because cognitive radios are constantly learning and evolving, adapting to new channel conditions. Machine learning algorithms make this possible, and so NI provides interfaces to CPU and GPU-based compute servers via PCI Express, 100 GbE, and Xilinx Aurora, to enable cognitive capability.

Solution Details

A Validated Design Pattern

For this reference architecture, NI has selected a configuration of software-connected COTS hardware from NI and third parties that satisfy the requirements of a wireless testbed. Furthermore, NI has implemented a fully operational 32-channel system and measured its performance. The following resources are freely available to users of the reference architecture:

- Complete bill of materials including rack, cables, and other hardware required for system assembly
- User manual including system assembly instructions and measured specifications
- Reference software, built upon an open-source stack, that demonstrates control of the system

System Overview

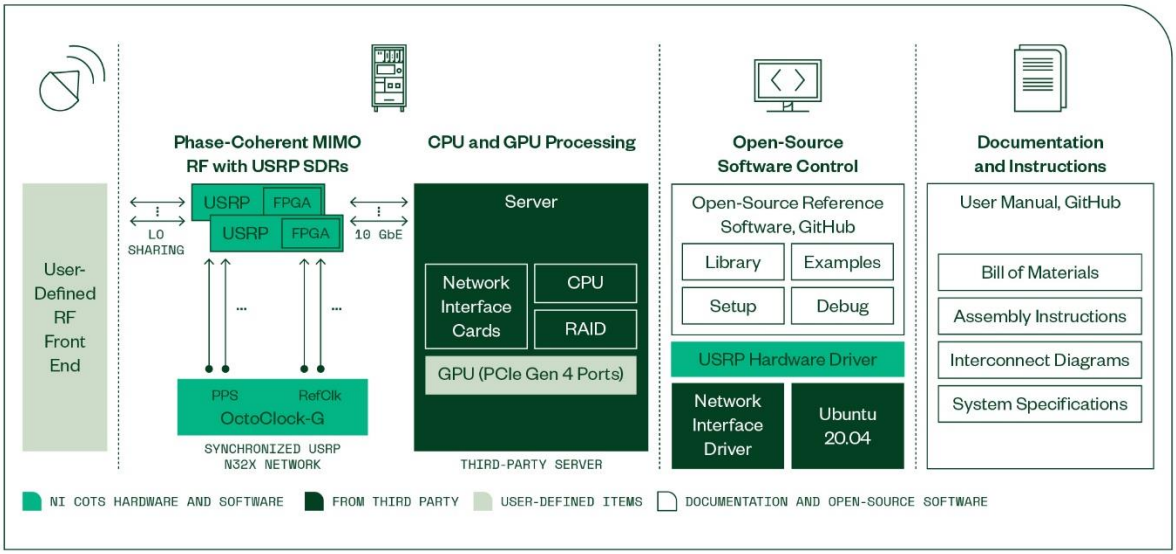

FIGURE 02 The Open Architecture for Communications Research provides the hardware, software, and documentation that accelerates path from concept to prototype.

Key Specifications & Features

- Direct conversion RF sampling
- Up to 200 MHz instantaneous bandwidth per channel
- 3 MHz – 6 GHz total RF frequency coverage
- Phase coherent operation via shared local oscillator, PPS, and 10 MHz reference clock signals
    - <0.2° average channel-to-channel skew over 1 hour
    - <0.1° average channel-to-channel skew over 10 runs
- Scalable multi-channel architecture
- Controlled with open-source software
- Up to 33.33 MSp/s on 32 channels simultaneously—streaming received data to disk or memory

- CPU and FPGA processing nodes
- Open PCIe slots for user customization
- Ideal for both over-the-air (OTA) and cabled operation

FIGURE 03 Example Testbed with Server and USRPs Installed

NI COTS Hardware Components

USRP N320 and N321 Software Defined Radios

The USRP N320 and N321 are networked software defined radios that provide reliability and fault tolerance for deployment in large-scale and distributed wireless systems. They are high-performance SDRs that use a unique RF design by Ettus Research to provide 2 RX and 2 TX channels in a half-wide RU form factor. Each channel provides up to 200 MHz of instantaneous bandwidth and covers a frequency range from 3 MHz to 6 GHz. The baseband processor uses the Xilinx Zynq-7100 SoC to deliver a large user-programmable FPGA for real-time, low latency processing and a dual-core ARM CPU for stand-alone operation.

Support for 1 GbE, 10 GbE, and Aurora interfaces over two SFP+ ports and 1 QSFP+ port enables high-throughput IQ streaming to a host PC or FPGA coprocessor. Its flexible synchronization architecture includes support for LO sharing for TX and RX, 10 MHz clock reference, PPS time reference, and GPSDO; White Rabbit enables implementation of phase-coherent MIMO configurations. The USRP N320/1 leverages recent software developments in UHD to simplify control and management of multiple devices over the network with the unique capability to remotely administrate tasks such as debugging, updating software, rebooting, resetting to factory state, and monitoring system health.

The USRP N321 features 2 four-way power splitters for distributing an LO signal to other USRP N32x units in a multi-USRP system.

FIGURE 04 USRP N32x SDRs provide RF front ends, I/O, LO synthesis, and power splitters for distributing LO, as well as an available FPGA processing node.

CDA-2990 Clock Distribution Device with GPSDO (OctoClock-G)

The CDA-2990 is an 8-channel, 10 MHz Clock Distribution Device that helps you synchronize systems that include USRP Software Defined Radio Devices. It accepts both external 10 MHz and pulse-per-second (PPS) input signals and amplifies and distributes the signals to eight output ports. The CDA-2990 is available in a configuration for distributing externally supplied signals. In the Open Architecture for Communications Research, NI recommends the GPS-disciplined oscillator (GPSDO)-enabled option, which integrates a GPS-disciplined oven-controlled crystal oscillator (OCXO) that generates the 10 MHz and PPS signals internally.

FIGURE 05 The CDA-2990 provides clock synchronization to a network of USRP N32x SDRs.

Validated Third-Party COTS Components

The Open Architecture for Communications Research incorporates hardware from third-party vendors. The following system components have been validated and are recommended for up to 32-channel systems.

Server

Directly stream large volumes of data from a multi-USRP system to a compute server to assess novel cognitive radar algorithms. A server with many available PCIe slots offers users the flexibility to insert GPUs for improved real-time processing power, additional SSDs, or additional network interface cards to increase channel count.

Supermicro 4124GS-TNR—Server with dual AMD EPYC™ CPUs and 10 PCIe Gen 4 x16 slots. Numerous PCIe lanes from the CPU support many 10 GbE connections and the PCIe processing required for high-channel-count systems.

Trenton Server—Server with dual 3rd generation Intel® Xeon® Ice Lake processors, 11 Gen 4.0 PCIe slots (5 x16 slots, 6 x8 slots), and 24x DDR4-3200 ECC RDIMM slots for high-channel-count systems.

Network Interface Cards (NICs)

Network Interface Cards allow USRPs to stream data to a server over 10 GbE links.

Intel® X710-DA4—supports x4 10 GbE connections.
Intel® E810-CQDA2—supports x2 100 GbE connections, or, with a breakout cable, x8 10 GbE connections.

High-Performance Data Storage

High volume and speed are necessary for writing wide bandwidth I/Q data to disk for post-processing or playback. NI recommends using SSD drives in a RAID 0 configuration to achieve high data read and write speeds.

HighPoint SSD7505—PCIe carrier board that holds x4 M.2 drives and supports either a software or hardware RAID configuration.
Sabrent 2 TB Rocket 4 Plus—NVME M.2 SSD drive that supports consecutive write rates of more than 6 GB/s.

Note: For a complete list of validated hardware, see the User Manual and GitHub

Software

Utilize a validated open-source software stack to set up, synchronize, and control wireless systems built following the Open Architecture for Communications Research. Find prebuilt example code for controlling the reference architecture, as well as system setup documentation at the following link:

https://github.com/EttusResearch/refarch-multich

Reference Architecture Software

In the Multichannel RF Reference Architecture GitHub repository, NI provides a library of functions for configuring and controlling a network of multiple USRPs, as well as reference examples that utilize the library to demonstrate highly synchronized transmission and receiving on multiple channels. These examples have been validated by NI for up to 32 Transmit x 32 Receive channels and allow for scaling to even higher channel count systems. The library and example are written in C++ and make use of the UHD and RFNoC APIs.

UHD API

The USRP Hardware Driver™ (UHD) software API supports application development on all USRP SDR products. Using a common software interface is critical as it increases code portability, allowing applications to transition seamlessly to other USRP SDR platforms when development requirements expand, or new platforms are available. UHD also offers cross-platform support for multiple industry standard development environments and frameworks, including RFNoC, GNU Radio, LabVIEW, MathWorks MATLAB® software, and MathWorks Simulink® software.

In the Open Architecture for Communications Research reference software, UHD is used to transport user waveform samples to and from USRP hardware as well as control various parameters (e.g., sampling rate, center frequency, gains, etc.) of the radio. UHD GPP driver and firmware code is written in C/C++ while the code developed for the FPGA is written in Verilog. The majority of the UHD code base is open source, including code that executes on the host, as well as code targeted to the USRP FPGA.

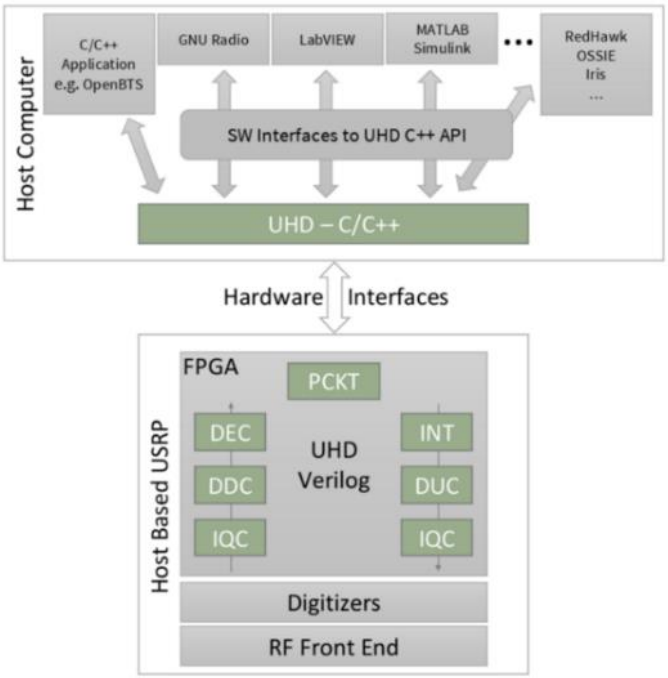

FIGURE 06 Components of the USRP Hardware Driver (UHD)

RFNoC API

RFNoC is a network-distributed heterogeneous processing tool with a focus on enabling FPGA processing in USRP devices. It allows you to move data on and off of an FPGA in a transparent way, thus enabling seamless use of both host-based and FPGA-based processing in an application. It provides a way to leverage FPGA processing capabilities and IP in your application, which can scale across multiple FPGAs and devices across a network. The Open Architecture for Communications Research reference software utilizes the RFNoC API to connect, synchronize, and control the system of USRPs. Utilizing RFNoC, sample signals can be loaded onto the USRPs and transmitted.

NI Solutions for SATCOM and Telemetry Validation

Beyond research and prototyping of communications systems, NI offers solutions for system-level validation and functional and parametric test.

The NI solution for SATCOM and telemetry systems validation consists of COTS modular hardware and flexible software tools to address RF signal fidelity, system level validation, and digital system test requirements. The solution is built on the PXIe modular test platform that can be customized to meet your specific IO performance requirements.

The NI Vector Signal Transceiver (VST) is the central RF technology for this solution. On its own, the VST can transmit and receive TT&C and SATCOM data link signals performing key signal fidelity measurements such as modulation accuracy, transmit power, and more. The VST can be augmented with a PXIe FlexRIO coprocessor with full-rate streaming to and from an open FPGA capable of hosting real-time, inline signal processing and channel models. With a coprocessor configuration, the VST is transformed into an RF channel emulator—unlocking the ability to do full system-level validation.

Digital system test is accomplished with the use of NI FlexRIO modules as well, yet with a digital front-end configuration. NI FlexRIO combines a large user-programmable FPGA with a serial or parallel digital IO to meet the system interfacing and IP protocol requirements of satellite payload subsystems test. With NI FlexRIO, engineers can import custom digital protocols to emulated digital interfaces without using custom hardware.

PXIe System Platform

- 3U Modular Instrumentation Chassis
- Expandable to 18 slots
- Data Transfer up to 24 GB/s
- Integrated Clocking/Triggers

For more information on testing communications systems, visit:
https://www.ni.com/en-gb/solutions/aerospace-defense/communications-navigation.html

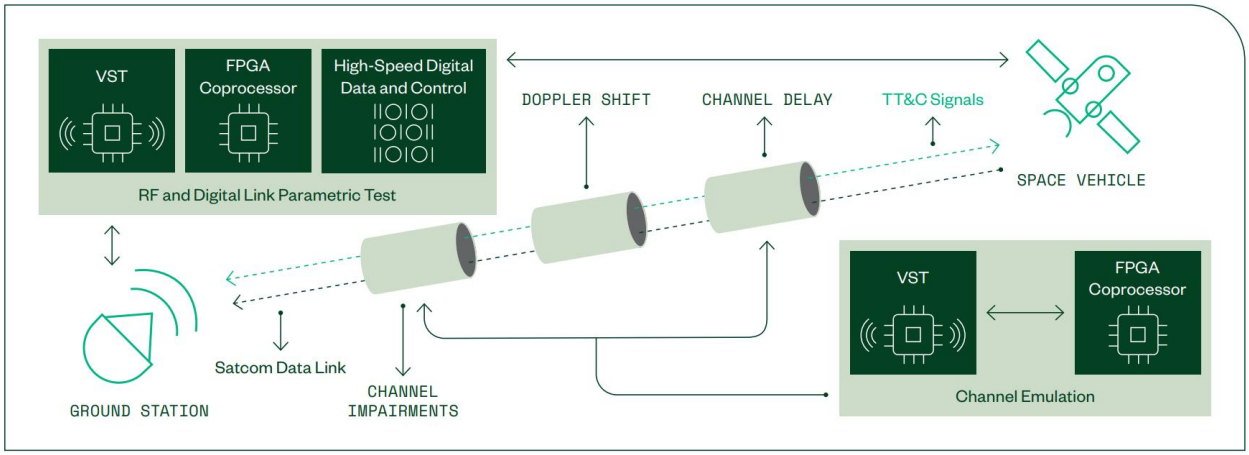

FIGURE 07 Common SATCOM and Telemetry Tests

ATTRIBUTION STATEMENT

NI Services and Support

NI offers a variety of solution integration options customized to your application-specific requirements. You can use your own internal integration teams for full system control or leverage the expertise of our worldwide network of NI Partners to obtain a turnkey system.

Contact your account manager or call or email us to learn more about how NI can help you increase product quality and accelerate test timelines at (888) 280-7645 or info@ni.com.

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