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Open Architecture for Radar and EW Research

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Trends in Radar

Radar systems are experiencing considerable technology disruption because of the rapidly changing electromagnetic battlespace. Active electronically scanned arrays, ultra-wideband technology, and cognitive radar systems present new design and test challenges for even the most experienced organizations.

Rapidly Prototype Radar Waveforms and Architectures

Threats and countermeasures continue to evolve at a rapid pace. Today, radar must track agile, hypersonic weapons, resolve swarms of drones, and detect low-RCS aircraft. Radar system developers are expected to prototype new concepts quickly, such as cognitive techniques or fully digital beamforming, to counteract emerging threats, increase performance and capability, and assure operation in contested EM environments. COTS software defined radios (SDRs) with an integrated software workflow help accelerate the transition from concept to testbed to deployed system.



FIGURE 01

Northrop Grumman E-2D Advanced Hawkeye: Airborne Early Warning Command and Control

“Using COTS equipment greatly reduced our efforts to design complex radar systems. We could focus more on DSP rather than on designing RF I/O over and over again.”

Dr. Piotr Samczyński
Warsaw University of Technology Institute of Electronic Systems



Reference Architecture Overview

The Open Architecture for Radar and EW Research is NI's blueprint for a system that meets key requirements of a hardware testbed for prototyping novel radar and EW technology. Follow NI's recommended solution to build up a multi-channel radar/EW research system as quickly as possible; this reference architecture has been validated by NI engineers to ensure it delivers the specified performance. Based on COTS Hardware and open-source software, this solution is ideal for rapidly transitioning radar IP through its development lifecycle: from software simulation to proof-of-concept demonstration to tactical deployment.

Architectures for Multichannel Radar/EW Research and Prototyping

Modern radar systems incorporate capability including cognitive function, multi-channel operation, and machine learning / artificial intelligence. To prototype novel capability for such systems, systems engineers and researchers must quickly develop a testbed for evaluating new ideas. The NI hardware platform provides key capabilities for radar and EW research.

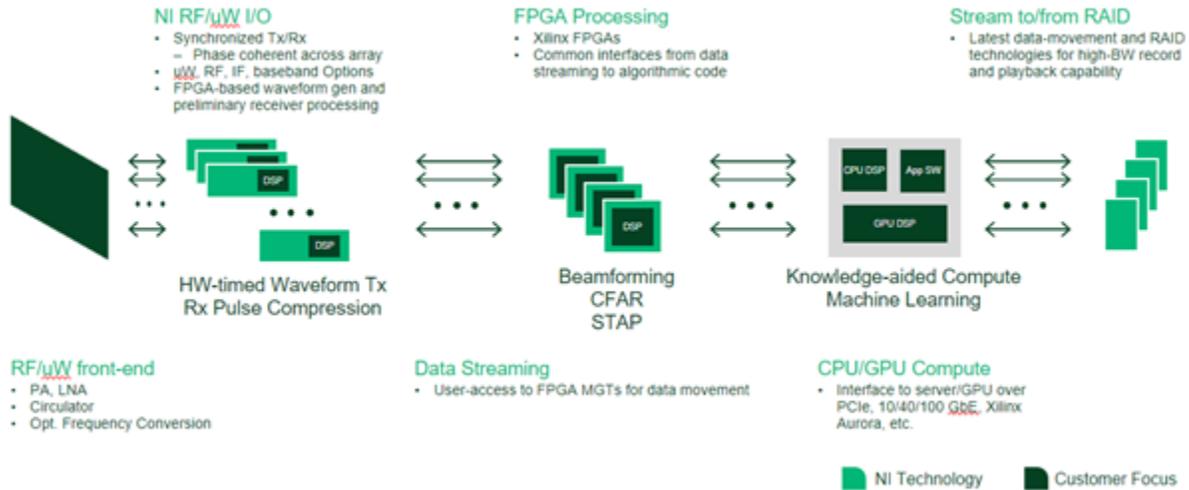


FIGURE 03

Radar researchers can focus more on their novel front end or DSP when the RF I/O, processing modules, and data movement infrastructure are provided by COTS components.



Multichannel Systems

For accurate ranging and positioning of targets, it is necessary for the transmit (Tx) and receive (Rx) chains of a radar system to be synchronized. For multi-channel systems, this becomes yet more important since multiple Tx and Rx chains must be synchronized across an array. NI COTS modular instruments based on the PXI platform provide phase coherency via the sharing of local oscillators, reference clocks, sampling clocks, and triggers.

Data Streaming

Wide bandwidth I/Q data necessitates high throughput streaming interfaces. NI provides users with access to FPGA multigigabit transceivers (MGTs) to avoid bottlenecks in moving data from I/O to processing.

Digital Signal Processing (DSP)

Novel capability such as spectral interference avoidance, clutter suppression, and automatic target recognition requires inline processing of radar return signals. NI incorporates Xilinx FPGAs onboard instruments like Vector Signal Transceivers and FlexRIO. This allows engineers and researchers to execute calculations like space-time adaptive processing (STAP), constant false alarm rate (CFAR), and beamforming with hardware-level latency and performance.

Machine Learning / Knowledge-Aided Computing

Today's cognitive radar system operates differently from yesterday's. And tomorrow's will operate differently from today's. That's because cognitive radars are constantly learning and evolving, adapting to new targets, new countermeasures, and new channel conditions. Machine learning algorithms make this possible, and so NI provides interfaces to CPU and GPU-based compute servers via PCI Express, 100 GbE, and Xilinx Aurora, to enable cognitive capability.



Solution Details

A Validated Design Pattern

For this reference architecture, NI has selected a configuration of software-connected COTS hardware from NI and third parties that satisfy the requirements of a radar/EW testbed. Furthermore, NI has implemented a fully operational 32-channel system and measured its performance. The following resources are freely available to users of the reference architecture:

- Complete bill of materials including rack, cables, and other hardware required for system assembly
- User manual including system assembly instructions and measured specifications
- Reference software, built upon an open-source stack, that demonstrates control of the system

System Overview

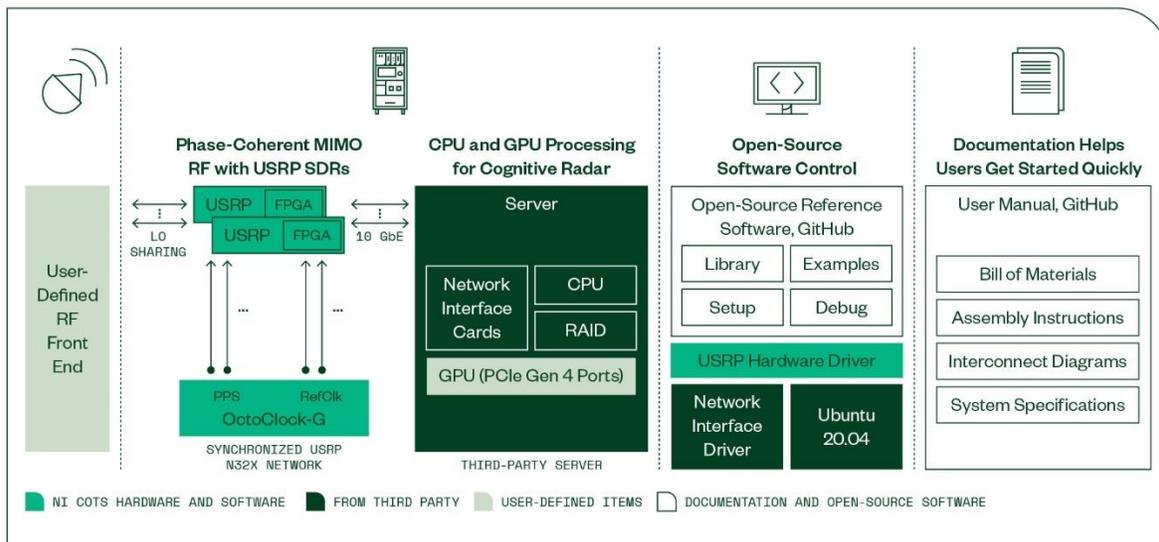


FIGURE 04

The Open Architecture for Radar and EW Research provides the hardware, software, and documentation that accelerates path from concept to prototype



Key Specifications & Features

- Direct conversion RF sampling
- Up to 200 MHz instantaneous bandwidth per channel
- 3 MHz – 6 GHz total RF frequency coverage
- Phase coherent operation via shared local oscillator, PPS, and 10 MHz reference clock signals
- Scalable multi-channel architecture
- Controlled with open-source software
- Up to 33.33 MSp/s on 32 channels simultaneously streaming data to disk or memory
- CPU and FPGA processing nodes
- Open PCIe slots for user customization
- Ideal for both over-the-air (OTA) and cabled operation



FIGURE 05

Example Testbed With Server and USRPs Installed



NI COTS Hardware Components

USRP N320 and N321 Software Defined Radios

The USRP N320 and N321 are networked software defined radios that provide reliability and fault-tolerance for deployment in large scale and distributed wireless systems. They are high-performance SDRs that use a unique RF design by Ettus Research to provide 2 Rx and 2 Tx channels in a half-wide RU form factor. Each channel provides up to 200 MHz of instantaneous bandwidth, and covers a frequency range from 3 MHz to 6 GHz. The baseband processor uses the Xilinx Zynq-7100 SoC to deliver a large user programmable FPGA for real-time, low latency processing and a dual-core ARM CPU for stand-alone operation.

Support for 1 GbE, 10 GbE, and Aurora interfaces over two SFP+ ports and 1 QSFP+ port enables high throughput IQ streaming to a host PC or FPGA coprocessor. A flexible synchronization architecture with support for LO sharing for TX and RX, 10 MHz clock reference, PPS time reference, GPSDO, and White Rabbit enables implementation of phase coherent MIMO configurations. The USRP N320/1 leverages recent software developments in UHD to simplify control and management of multiple devices over the network with the unique capability to remotely administrate tasks such as debugging, updating software, rebooting, resetting to factory state, and monitoring system health.

The USRP N321 features 2 four-way power splitters for distributing an LO signal to other USRP N32x units in a multi-USRP system.



FIGURE 06

In NI's Open Architecture for Radar and EW, the USRP N32x SDRs provide RF front ends, I/O, LO synthesis, power splitters for distributing LO, as well as an available FPGA processing node



CDA-2990 Clock Distribution Device with GPSDO (OctoClock-G)

The CDA-2990 is an 8-Channel, 10 MHz Clock Distribution Device that helps you synchronize systems that include USRP Software Defined Radio Devices. It accepts both external 10 MHz and pulse-per-second (PPS) input signals and amplifies and distributes the signals to eight output ports. The CDA-2990 is available in a configuration for distributing externally supplied signals. In the Open Architecture for Radar and EW Research, NI recommends the GPS-disciplined oscillator (GPSDO)-enabled option, which integrates a GPS-disciplined oven-controlled crystal oscillator (OCXO) that generates the 10 MHz and PPS signals internally.



FIGURE 07

The CDA-2990 provides clock synchronization to a network of USRP N32x SDRs



Validated Third-Party COTS Components

The Open Architecture for Radar and EW Research incorporates hardware from third-party vendors. The following system components have been validated and are recommended for up to 32-channel systems.

Server

Directly stream large volumes of data from a multi-USRP system to a compute server to assess novel cognitive radar algorithms. A server with many available PCIe slots offers users the flexibility to insert GPUs for improved real-time processing power, additional SSDs, or additional network interface cards to increase channel count.

Supermicro 4124GS-TNR—Server with dual AMD EPYC™ CPUs and 10 PCIe Gen 4 x16 slots. Numerous PCIe lanes from the CPU support many 10 GbE connections and the PCIe processing required for high-channel-count systems.

Trenton Server—Server with dual 3rd generation Intel® Xeon® Ice Lake processors, 11 Gen 4.0 PCIe slots (5 x16 slots, 6 x8 slots), and 24x DDR4-3200 ECC RDIMM slots for high-channel-count systems.

Network Interface Cards (NICs)

Network Interface Cards allow USRPs to stream data to a server over 10 GbE links.

Intel® X710-DA4—supports x4 10 GbE connections.

Intel® E810-CQDA2—supports x2 100 GbE connections, or, with a breakout cable, x8 10 GbE connections.

High Performance Data Storage

High volume and speed are necessary for writing wide bandwidth I/Q data to disk for post-processing or playback. NI recommends using SSD drives in a RAID 0 configuration to achieve high data read and write speeds.

HighPoint SSD7505—PCIe carrier board that holds x4 M.2 drives and supports either a software or hardware RAID configuration.

Sabrent 2TB Rocket 4 PLUS—NVME M.2 SSD drive that supports consecutive write rates of more than 6 GB/s.

Note: For a complete list of validated hardware, see the OARER User Manual and GitHub



Software

Utilize a validated open-source software stack to set up, synchronize, and control radar systems built following the Open Architecture for Radar and EW research. Find prebuilt example code for controlling the reference architecture, as well as system setup documentation here:

<https://github.com/EttusResearch/refarch-multich>

Multichannel RF Reference Architecture

In the Open Architecture for Radar and EW Research GitHub repository, NI provides a library of functions for configuring and controlling a network of multiple USRPS, as well as reference examples that utilize the library to demonstrate highly synchronized transmission and receiving on multiple channels. These examples have been validated by NI for up to 32 Transmit x 32 Receive channels and allow for scaling to even higher channel count systems. The library and example are written in C++ and make use of the UHD and RFNoC APIs.

UHD API

The USRP Hardware Driver™ (UHD) software API supports application development on all USRP SDR products. Using a common software interface is critical as it increases code portability, allowing applications to transition seamlessly to other USRP SDR platforms when development requirements expand or new platforms are available. UHD also offers cross-platform support for multiple industry standard development environments and frameworks, including RFNoC, GNU Radio, LabVIEW, MathWorks MATLAB® software, and MathWorks Simulink® software.

In the Open Architecture for Radar and EW Research reference software, UHD is used to transport user waveform samples to and from USRP hardware as well as control various parameters (e.g., sampling rate, center frequency, gains, etc.) of the radio. UHD GPP driver and firmware code is written in C/C++ while the code developed for the FPGA is written in Verilog. The majority of the UHD code base is open source, including code that executes on the host, as well as code targeted to the USRP FPGA.

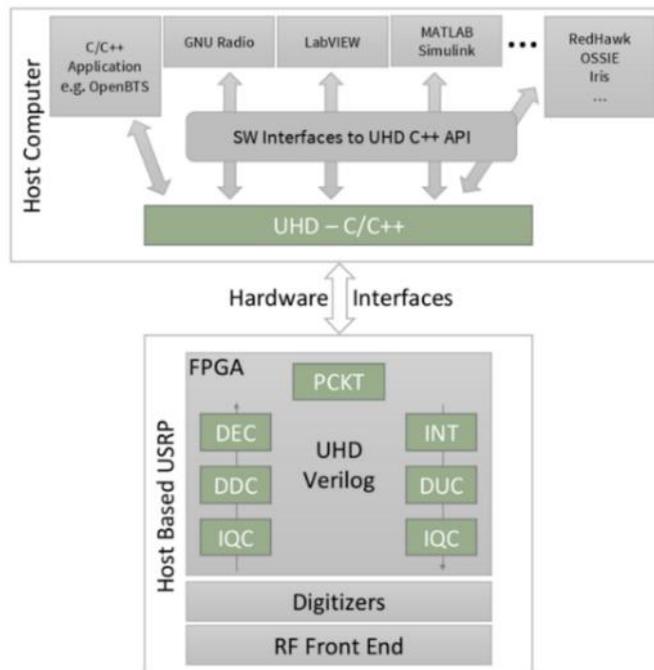


FIGURE 08

Components of the USRP Hardware Driver (UHD)

RFNoC API

RFNoC is a network-distributed heterogeneous processing tool with a focus on enabling FPGA processing in USRP devices. It allows you to move data on and off of an FPGA in a transparent way, thus enabling seamless use of both host-based and FPGA-based processing in an application. It provides a way to leverage FPGA processing capabilities and IP in your application, which can scale across multiple FPGAs and devices across a network. The Open Architecture for Radar and EW Research reference software utilizes the RFNoC API to connect, synchronize, and control the system of USRPs. Utilizing RFNoC, sample signals can be loaded onto the USRPs and transmitted.



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