

Protocol Analyzer for Digital Communication Validation

Kaitlyn Mazzarella (NI) Saravana Kumar Muthusamy (Soliton)





Agenda

NI Connect 2023: Technical Session

- Introduction & market challenges (5 mins)
- Overview of NI & Soliton's solution: software and hardware (10 mins)
 - PVS, PA, SDC, PXI
- Deep Dive into latest protocol software: Protocol Analyzer (20 mins)
- Q&A (remaining 10-15 mins)

About Us

N

- NI equips engineers and enterprises with systems that accelerate productivity, innovation, and discovery.
- Primarily focused on the semiconductor, electronics, aerospace/defense, and transportation industries.
- \$1.3B revenue in 2020
- 22% investment in R&D
- ~40 countries with NI operations
- 35,000+ customers worldwide



- Soliton works with global companies, from startups to Fortune 500, to help them increase their competitiveness and release great products through Digital Transformation Services.
- Primarily focused on the semiconductor, electronics, medical devices, automotive and transportation industries.
- 25 years of excellence
- 3,000+ customers worldwide

NI and Soliton have signed a strategic partnership agreement to jointly develop bench and enterprise software for Semiconductor Validation automation and Spec+Data Management

Challenges with Protocol Interface Validation



Lab Validation Challenges

- Increasing device complexity
- Ever-changing requirements
- New protocol evolution, such as MIPI I3C
- Validation of these interfaces are tedious job, but critical
- Achieving full spec coverage can be difficult for DIY
- High cost of tests

וח

- Pressure to reduce go-to-market time
- Lack of IP reuse / duplicate efforts
- Inconsistent data across teams

Standardized & Turnkey Solution Can Help

- Reduce time and cost: tool & framework development, maintenance
- Flexibility with hardware: protocol validation is done
 with software
- Quickly access and interpret protocol waveforms and data
- Easy debug and reporting with interactive software
- Faster RTM: reduce protocol validation time from weeks to hours
- Enable measurement IP reuse
- Reproduce & deploy solutions globally

Digital Protocol Validation Solution

Exerciser to Compliance Tester

Π





Protocol Validation Solution

- Protocol compliance tester
- Validate digital interface for specific protocol compliance (e.g., MIPI I3C, I2C, SPI, SPMI)
- Timing, electrical, functional & fault reliability tests
- Hardware: Works with PXIe-657x Digital
 Pattern Instrument

Hardware



Semiconductor Device Control (Protocol Exerciser)

- Interactive & automated device communication via digital interface
- Perform register R/W & static DIO
- MIPI I3C, I2C, SPI, RFFE
- Hardware: Works with PXIe-657x



PXI Digital Pattern Instrument (PXIe-657x): Includes Digital Pattern Editor for configuring pin maps, specs, levels, timing, and patterns

Oscilloscopes: High performance portfolio of NI scopes



Protocol Analyzer



Why Protocol Analyzer?



Protocol bus sniffer Debug & Analyze the waveform during DUT bring up



Verify device performance in system

Signal integrity Testing Functional Testing

Challenges with Traditional Protocol Analyzer Oscilloscope Based and Box Type

Π

| \$\$\$ | | |
|--|---|-------------------|
| Requires Costly Oscilloscopes that supports Protocol Decoding | rotocol Supports dditional hardware or plugin | omation |
| Depends on exact model of the oscilloscope or box type equipment | upport for protocol al measurements history | tomated apture |

Protocol Analyzer and Decoder



Turn your scopes into powerful protocol analyzers

SOFTWARE

Л

- · Verifies device performance in system & signal integrity testing for MIPI I3C, I2C protocols, and more
- Decode and annotate the captured protocol waveform
- Measures and reports the timing and voltage parameters
- Open architecture to support any scopes
- Provides detailed and insightful data logs
- Easy to automate from external programming environment through APIs

HARDWARE

- Protocol Analyzer software works with Oscilloscopes
- Captures the protocol packet information while SW decodes



Key Advantages

| Convert your existing scopes into analyzers. Doesn't need additional hardware | |
|--|--|
| | |

Hardware Agnostic solution



Easy to add new Protocols with simple software plugin

Performs both Protocol Decoding and Full Electrical Measurements Comes with automation APIs to enable automation from external applications

Maintains capture history and logs the decoded information into insightful TDMS files

Protocol Analyzer Software Preview



Enable Interactive Debug Semi Device Control + Protocol Analyzer

Л

Graphical Time domain signals with Data Overlayed - Enables Interactive waveform debug window to identify problems



SDC Small Panel

- Interactive Register Read write

<u>Key Highlights:</u>

- 1. Seamless integration with NI's SDC
- 2. Can be used as Bus monitors when multiple masters act on the bus

Protocol timing measurements

MIPI I3C[®] Protocol Test Coverage

Parametric Measurements

- ✓ tLOW_OD (Low period of SCL clock)
- ✓ tHIGH_OD (High period of SCL clock)
- ✓ tfDA_OD (Fall time of SDA signal)
- ✓ tSU_OD (Data setup time during open-drain mode)
- ✓ tCAS (Clock after start condition)
- ✓ tCBP (Clock before stop condition)
- ✓ fSCL (SCL Clock Frequency)

ח

- ✓ tLOW_PP (SCL Clock Low Period)
- ✓ tHIGH_PP (SCL Clock High Period)
- ✓ tSCO (Clock in to Data out for slave)
- ✓ tCR (SCL Clock Rise Time)
- ✓ tCF (SCL Clock Fall Time)
- ✓ tHD_PP (SDA signal Data Hold in Push-pull mode)
- ✓ tSU_PP (SDA signal Data Setup in Push-pull mode)
- ✓ tCASr (Clock after Repeated start condition)
- ✓ tCBSr (Clock before Repeated start condition)
- ✓ VIL (Low level input voltage)
- ✓ VIH (High level input voltage)
- ✓ VOL (Low level output voltage)
- ✓ VOH (High level output voltage)
- ✓ Legacy I2C Timing Parameters

Functional Validation

- Verify if the correctness of MIPI I3C[®] packet structure
 Presence of Start, Stop, Repeated Start at right
 - places
 - ✓ Number of clocks with proper ACK bits
- Parse and display different portions/packets of the protocol like Start, Stop, Device Address, ACK/NACK bit, etc
- ✓ Reports faults/errors in the MIPI I3C[®] packet structure
- Ability to differentiate and display Write and Read Data
- Supports below transactions
 - ✓ SDR Write
 - ✓ SDR Read
 - SDR Combined Format
 - ✓ SDR CCC Command
- ✓ Ability to detect HDR Stop and Restart Patterns

I2C Protocol Test Coverage

Parametric Measurements

✓ fSCL(SCL Clock Frequency)

וח

- ✓ tSU;STA (Setup Time for a Repeated Start Condition)
- ✓ tHD;STA (Hold Time (repeated) Start Condition)
- ✓ tLOW (Low Period of the SCL Clock)
- ✓ tHIGH (High Period of the SCL Clock)
- ✓ tSU;DAT (Data Setup Time)
- ✓ tHD;DAT (Data Hold Time)
- ✓ trCL (Rise Time of SCL Signal)
- ✓ tfCL (Fall Time of SCL signal)
- ✓ trDA (RiseTime of SDA Signal)
- ✓ tfDA (Fall Time of SDA Signal)
- ✓ tSU;STO (Setup time for STOP Condition)
- ✓ tVD;DAT (Data Valid Time)
- ✓ tVD:ACK (Data Valid Acknowledgement Time)
- ✓ VIL (Low level input voltage)
- ✓ VIH (High level input voltage)
- ✓ VOL (Low level output voltage)
- ✓ VOH (High level output voltage)

Functional Validation

- ✓ Verify if the correctness of I2C packet structure
 - Presence of Start, Stop, Repeated Start at right places
 - ✓ Number of clocks with proper ACK bits
- Parse and display different portions/packets of the protocol like Start, Stop, Device Address, ACK/NACK bit, etc
- Reports faults/errors in the I2C packet structure
- ✓ Ability to differentiate and display Write and Read Data
- Supports below transactions
 - ✓ Write
 - ✓ Read
 - ✓ Combined Format

Roadmap



Q&A

Don't forget to check out the full demo in the Experience Lounge in the *Semiconductor & Electronics* section

Give us your feedback! Quick 2 Question Survey

In the mobile app, click into the session you would like to provide feedback for



10:15 AM Multichannel RF Data Recording 11:15 AM and Analysis

Meeting Room 19A

Aerospace & Defense •
 Technical Session

10:15 AM Optimizing Validation Processes: 11:15 AM Building Complex Test Systems with Distributed I/O

- Meeting Room 19B
- Aerospace & Defense •
 Technical Session

10:15 AM Panel: Continuous Integration (Cl/ 11:15 AM CD)—Don't Leave Home without It

- Meeting Room 12A
- Programming Essentials Technical Session

10:15 AM Using Python and TestStand to 11:15 AM Boost Your Test Development

Ballroom G

 Product & Technology • Technical Session

10:15 AM What Does Left Shifting Test 11:15 AM Mean in the NI Ecosystem?

Meeting Room 18A
 Transportation - Technical Session

〈 Tue May 23

🛨 Add to Schedule 🛛 🏥 iCal 🛛 👤 Check In

Optimizing Validation Processes: Building Complex Test Systems with Distributed I/O

Tue May 23 10:15 AM - 11:15 AM

Map Meeting Room 19B Aerospace & Defense • Technical Session

Surveys

Take Session Survey

In this session, learn to improve efficiency and reduce non-recurring engineering costs in validation labs by connecting multiple distributed line-replaceable unit (LRU) test systems. Also learn how to abstract LRUs and construct complex test systems faster and more efficiently using existing distributed I/O and edge computation technology.

Click "Take the Session Survey"

ni.com

NI CONFIDENTIAL