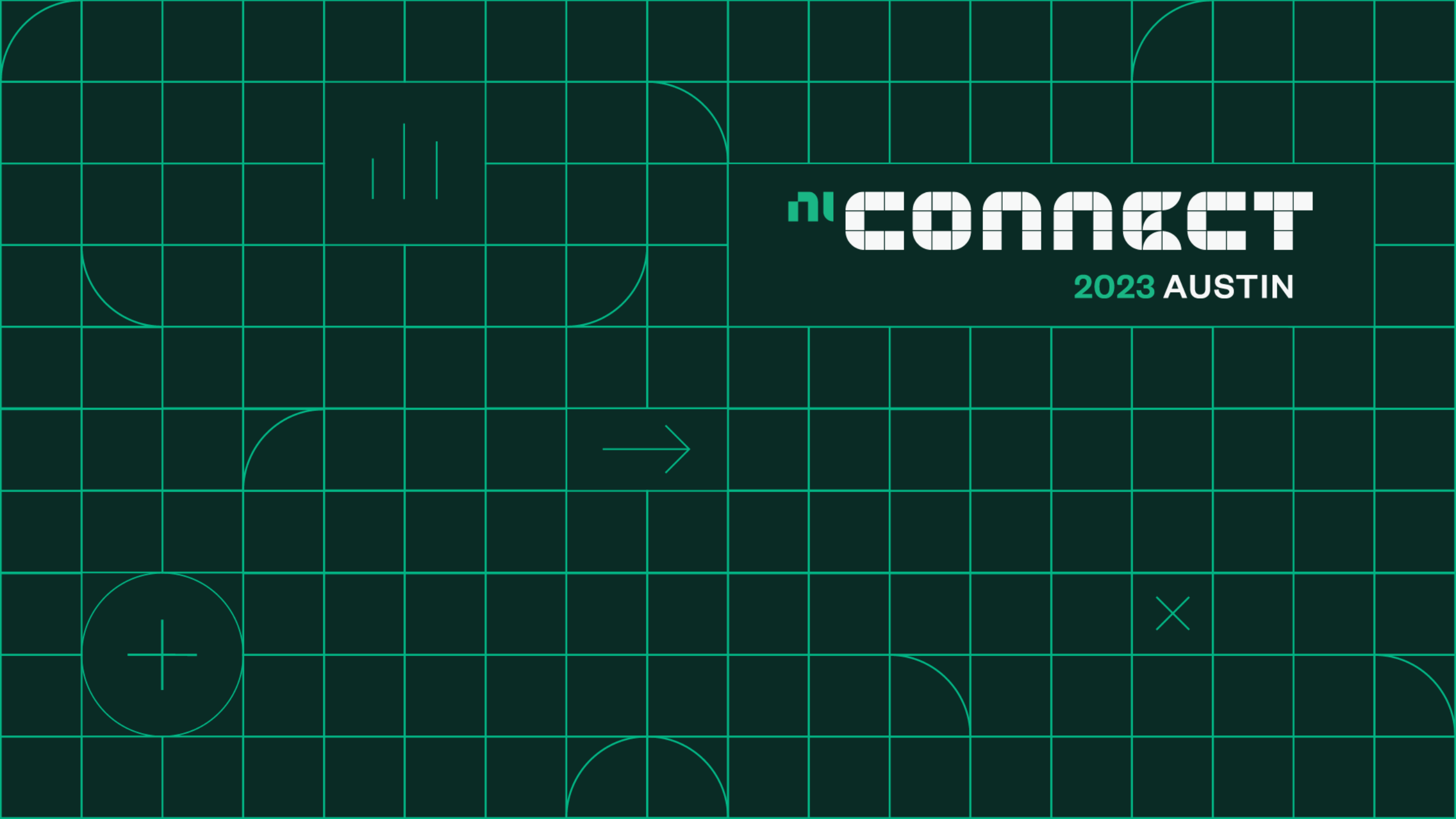

WELCOME TO AUSTIN


CONNECT
2023 AUSTIN

Is parametric test technology keeping up with massive investments in semiconductor foundry market?

Seshank Malap
OFFERING MANAGER, SEMICONDUCTOR

What Process Technology does Bionic 16 use?

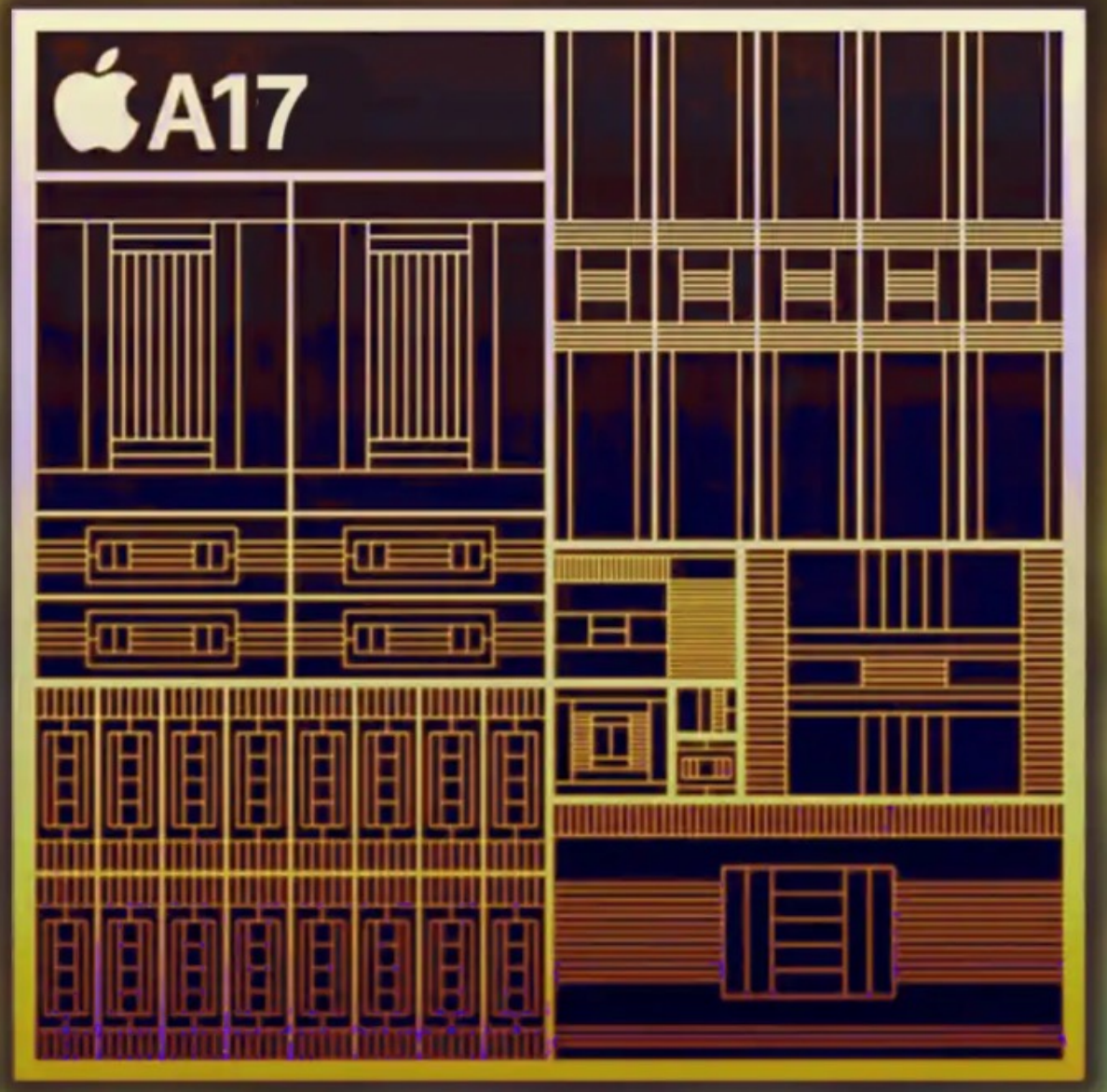
2 high-performance cores
Fastest mobile CPU
20% lower power

CPU performance

A16 Bionic 2022

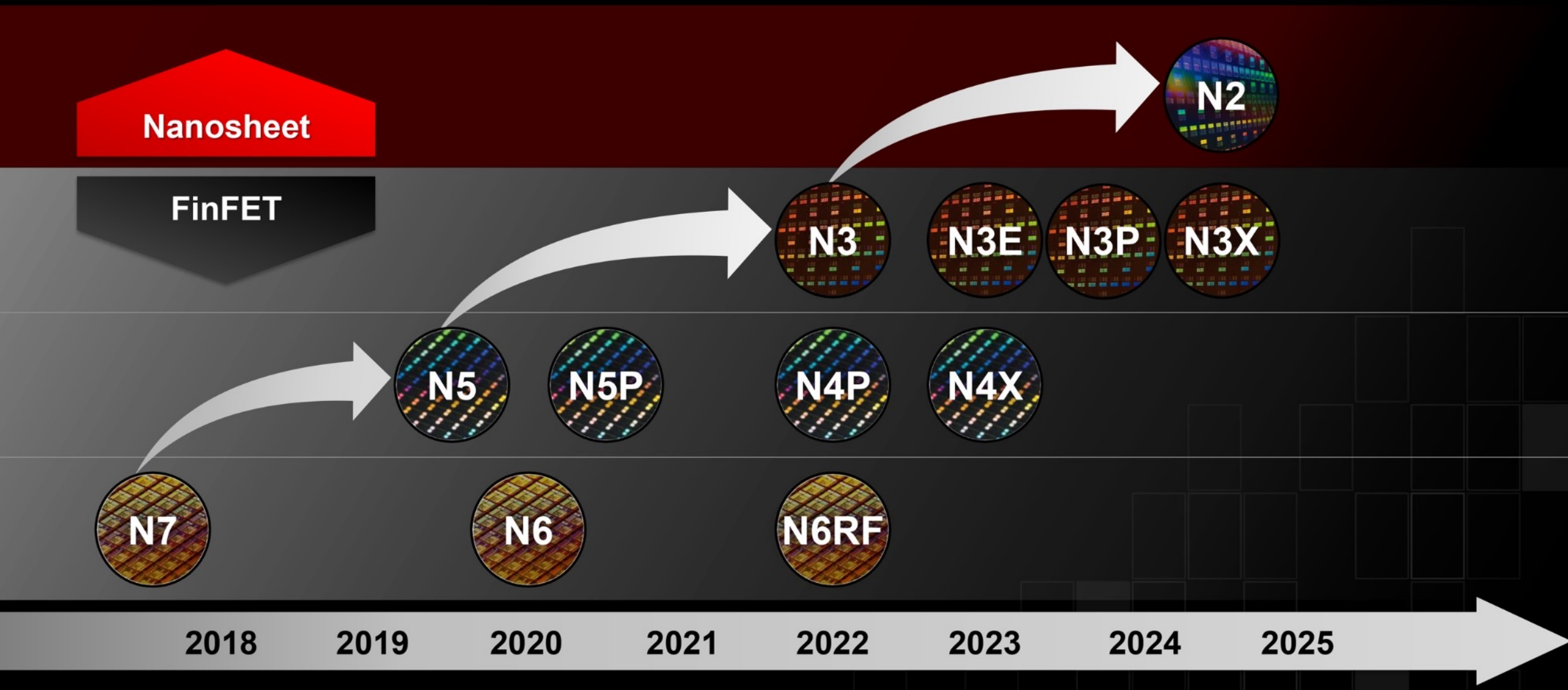
A13 Bionic 2019

Nearest competitor 2022

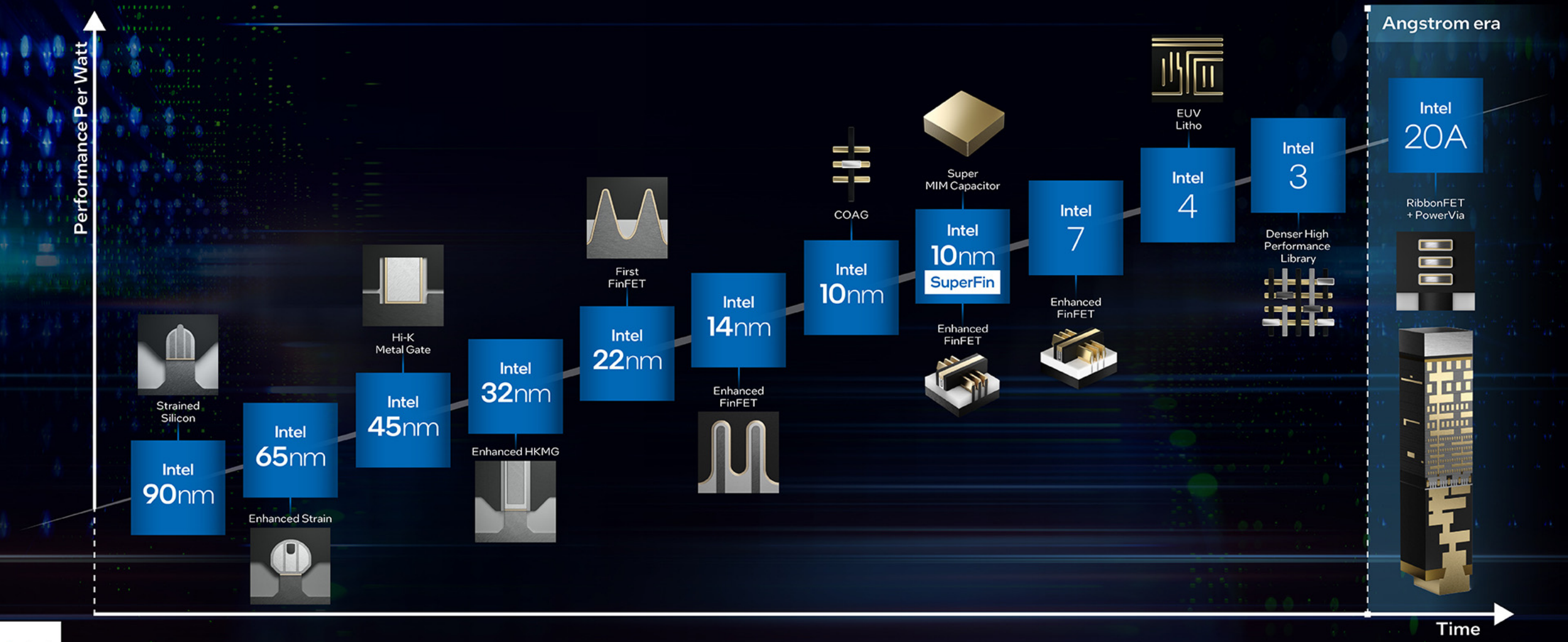

A17

Industry-leading Advanced Technology Portfolio

tsmc Unleash Innovation



Intel Process Technology Innovations



intel.

accelerated

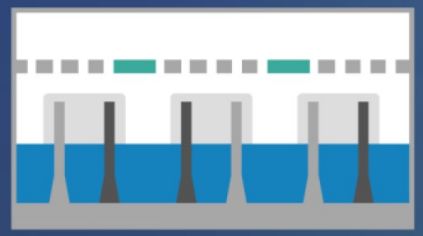
*Graphic is for illustrative purposes only and is not to scale

High NA EUV Enables 1nm and beyond

scaling roadmap continues to 1 nm and beyond

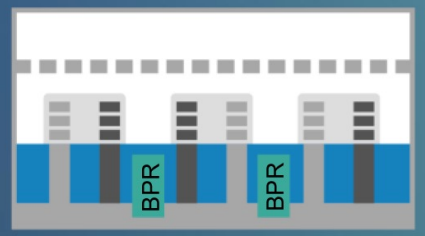
Slide 4
29 Sept. 2021

3 nm	2 nm	1,5 nm	1 nm and beyond
PP: 44-48, MP: 21-24	PP: 40-44, MP: 18-21	PP: 40-44, MP: 18-21	PP: 38-42, MP: 15-18



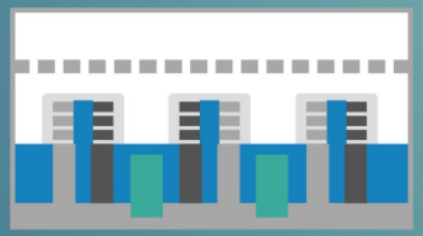
FinFET

5T



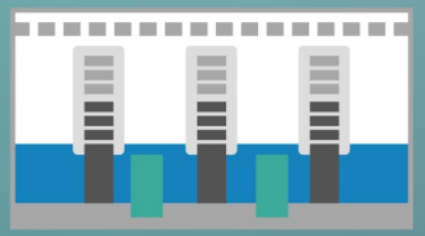
Nanosheets, BPR

5T



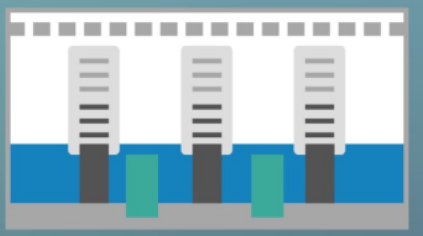
Forksheets, VHV std cell arch.

<5T



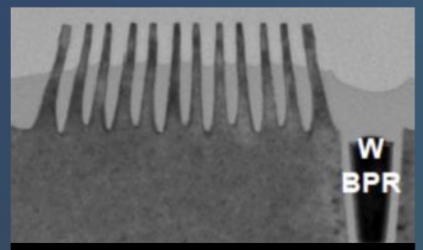
CFET, BEOL w/airgaps

4T

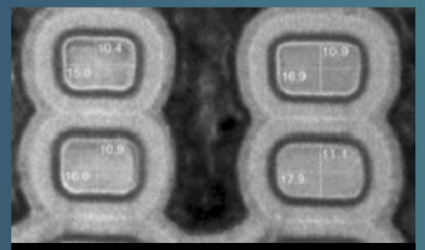


2D atomic channels

<4T



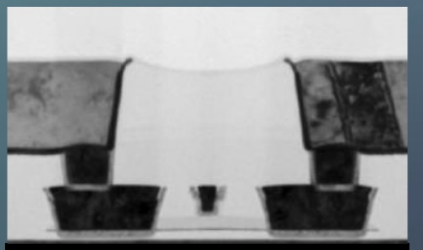
Buried power rail (BPR)



Nanosheets

Forksheets

Metal etch w/ airgaps

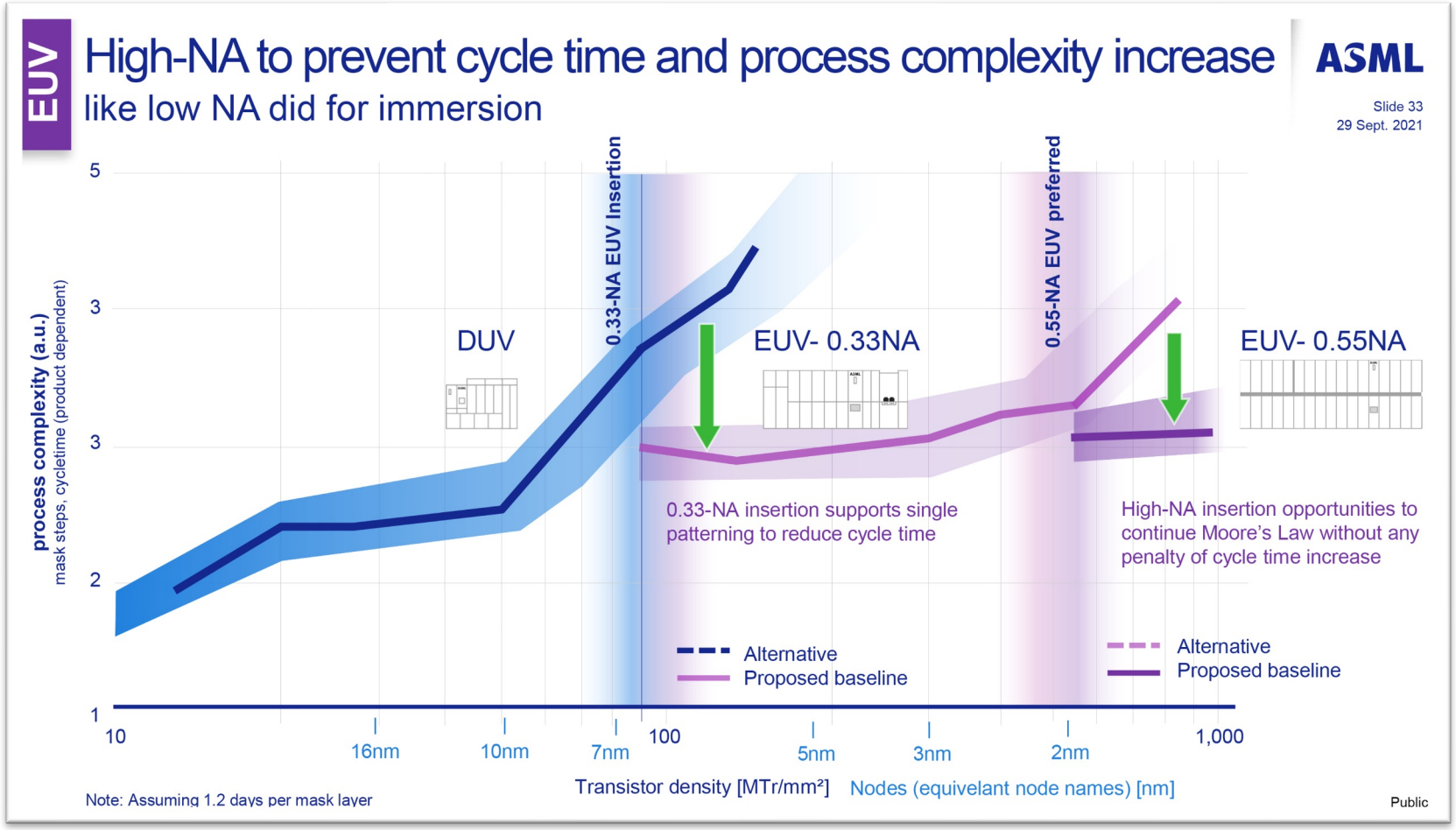


Metal etch w/ airgaps

PP: Poly Pitch (nm)

Path To High NA Extreme Ultraviolet Lithography

- **EUV (0.3NA) Lithography:**
  - Deployed in 2019 for 7nm
  - Pitches as tight as 36nm.
- **High NA EUV (0.55)**
  - Numerical Aperture Extreme Ultraviolet Lithography
  - Planned 2023 deployment
  - Will enable 2nm and beyond with smaller number of patterning steps



High NA EUVL –> High Density Electrical Correlation

- Advent of High-NA EUV lithography and reduced resist thickness exacerbates the optical metrology issue of detecting defects, hence reducing yield.
- Key is the development of wafer (electrical) inspection strategies which traditionally rely on optical techniques..
- ...Electrical tests of metallized patterns are increasingly being set up to look for correlations with data obtained with optical and e-beam inspection techniques. This allows to increase learnings on stochastic patterning failures and to gain more insights into the way they impact yield…

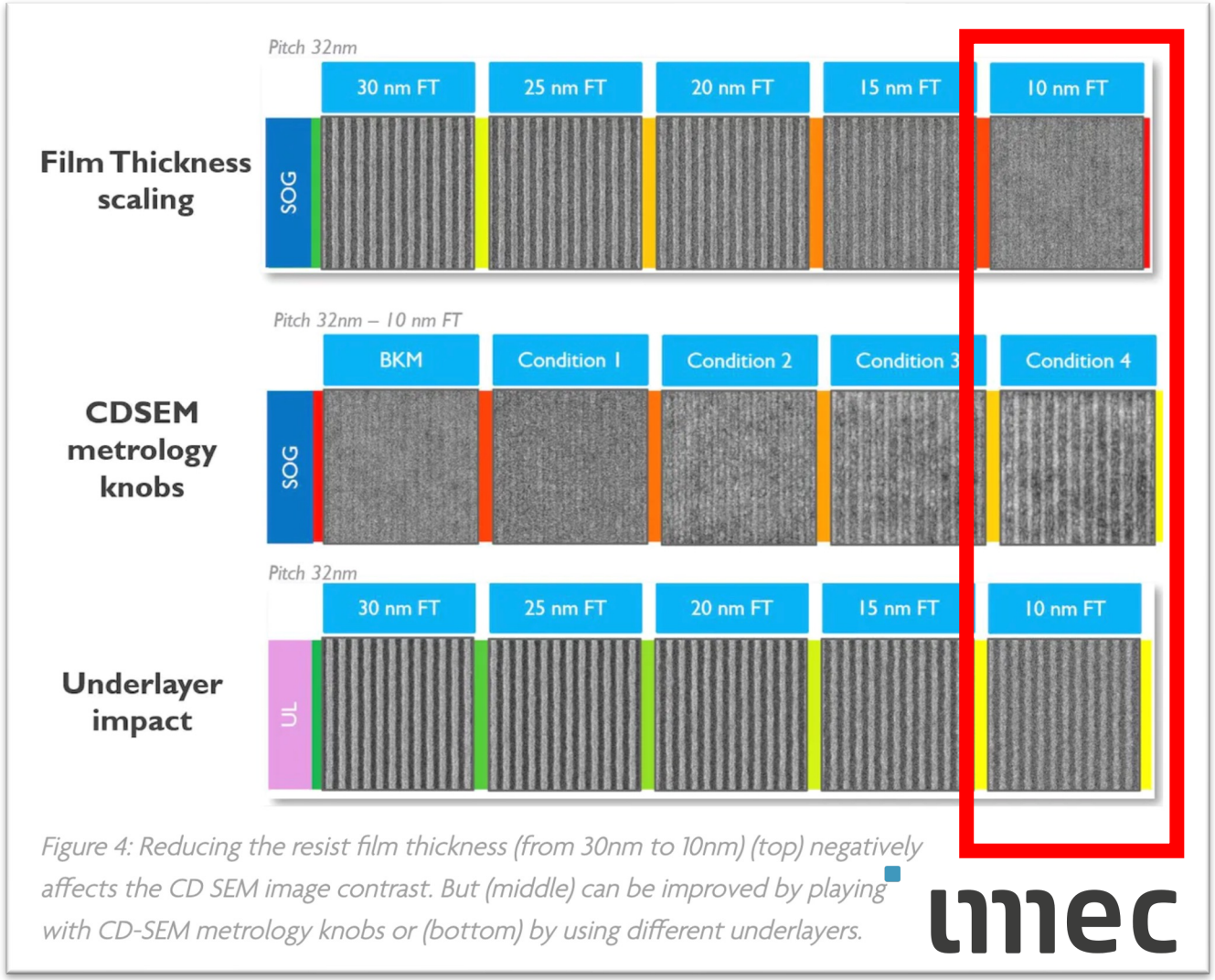


Figure 4: Reducing the resist film thickness (from 30nm to 10nm) (top) negatively affects the CD SEM image contrast. But (middle) can be improved by playing with CD-SEM metrology knobs or (bottom) by using different underlayers.

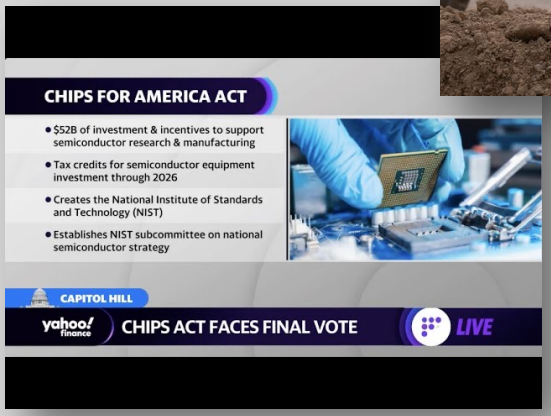
imec

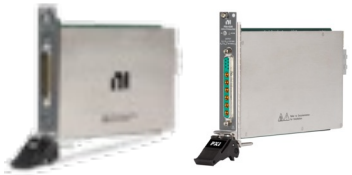
NI’s Impact

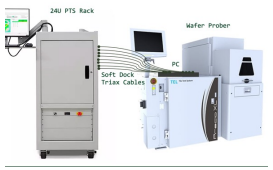
Imec Case Study

NI Investments In Wafer Parametric

- NI today: Highly Parallel WLR systems, ATE interfacing, software & Partner Network…







OEM WAT & WLR systems deployed at major fabs

PXIe-4135 (40W) fA SMU for Parametric Testing

PXIe-4190 Industry 1st CV + IV

Partner WLR system deployments at Major Foundries

PTS-50 50 Ch WLR System

PTS - WLR Enhancements

Low-Current Res SMU for Parametric Testing: PXIe-4135

IV Boundary

- **± 200 V**
- 1 A DC, 3 A Pulse
- 40 W DC, 500 W Pulse
- Current Specs (10 nA range)
- Sensitivity: 10 fA
- Accuracy: 0.05% + 750 fA

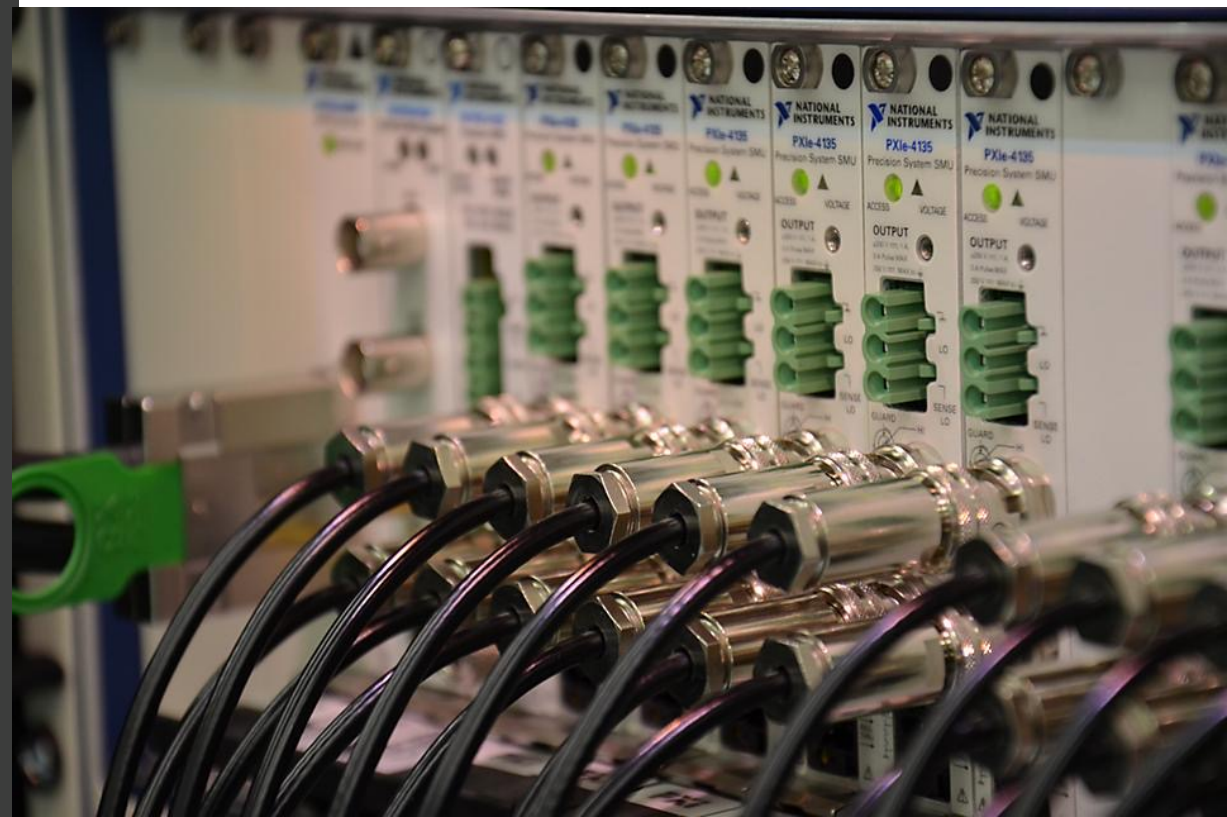
Max Speed:

- Sampling 1.8 MS/s
- Update: 100 kS/s

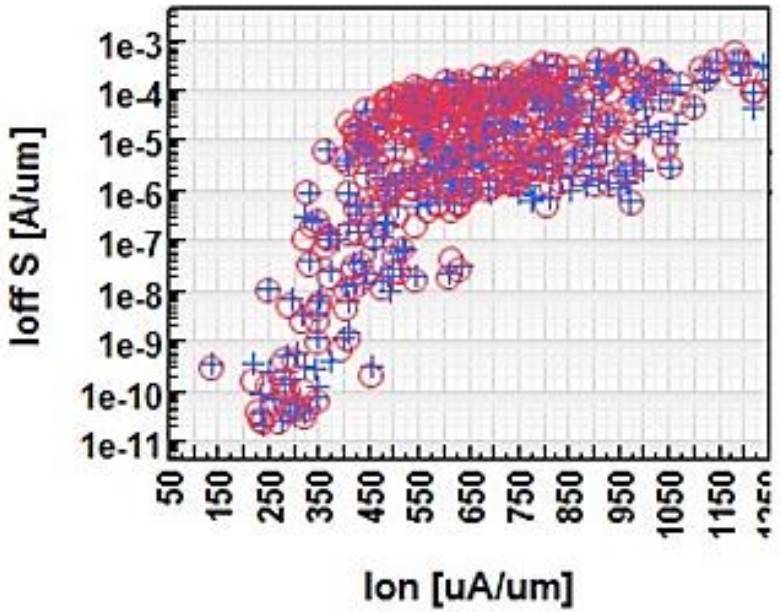
NI SourceAdapt™ Technology

Hardware timing & triggering

Triaxial connectivity

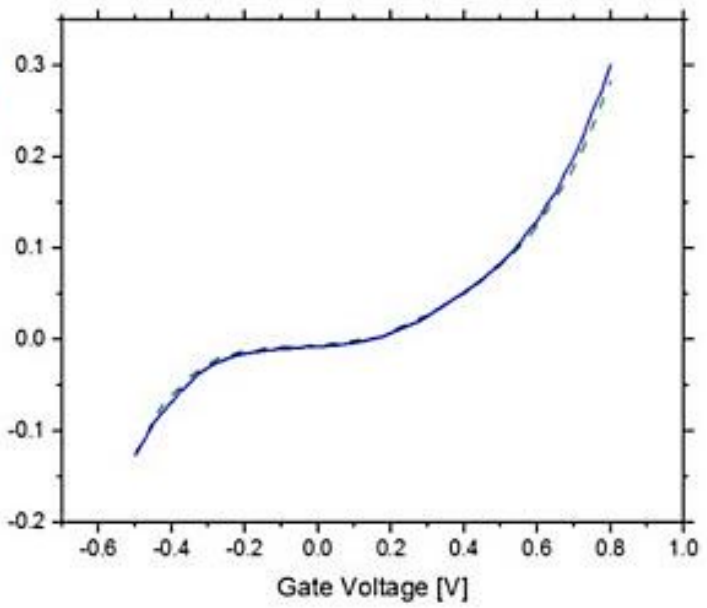


Tight Correlation – 4135 VS Traditional solutions



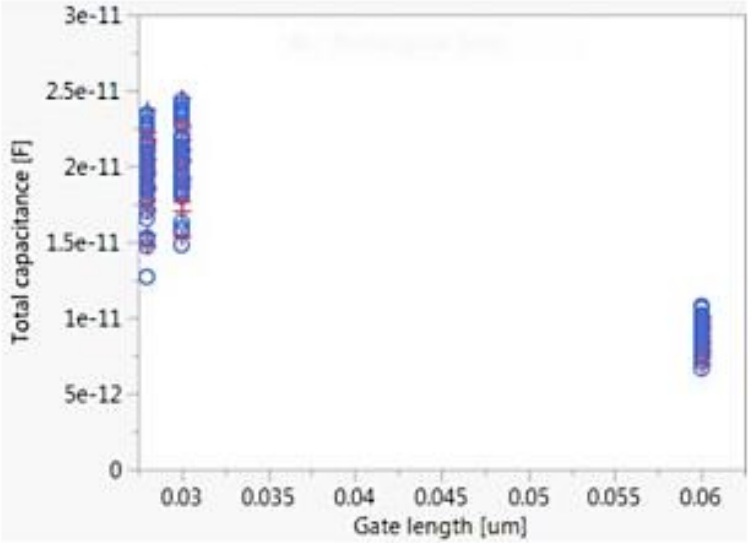
+ test results with PXIe-4135 SMU's
o test results with high end third-party tools

Off-state vs. On-state transistor current measurements: excellent match!



+ test results with PXIe-4135 SMU's
-- test results with high end third-party tools

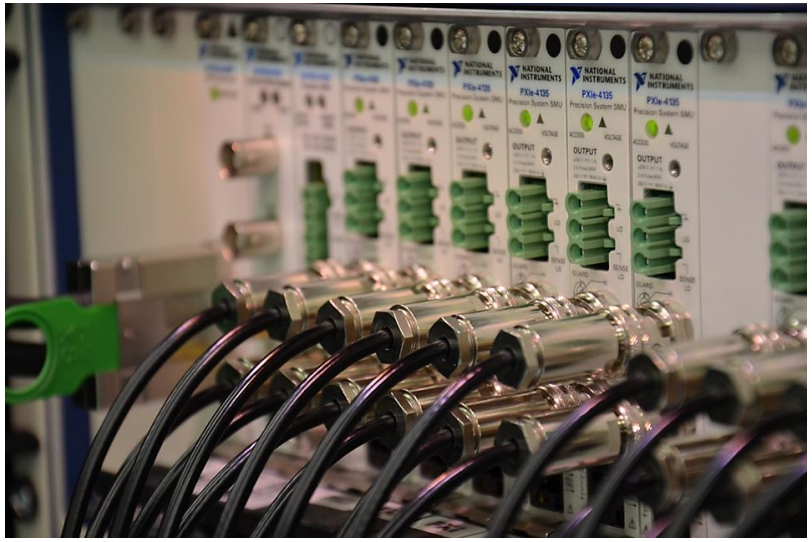
Transistor gate sweeps (gate currents < pA): excellent match!

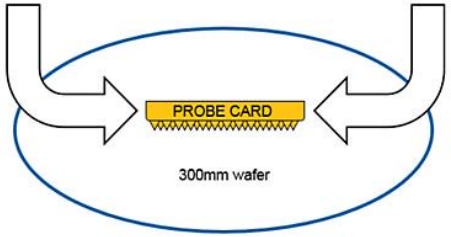


o test results with PXIe-4135 SMU's
+ test results with high end third-party tools

Low-capacitance CV measurements for transistor gates: excellent match!

IMEC's Inline 24 Ch Per-Pin Parallel Inline Testers





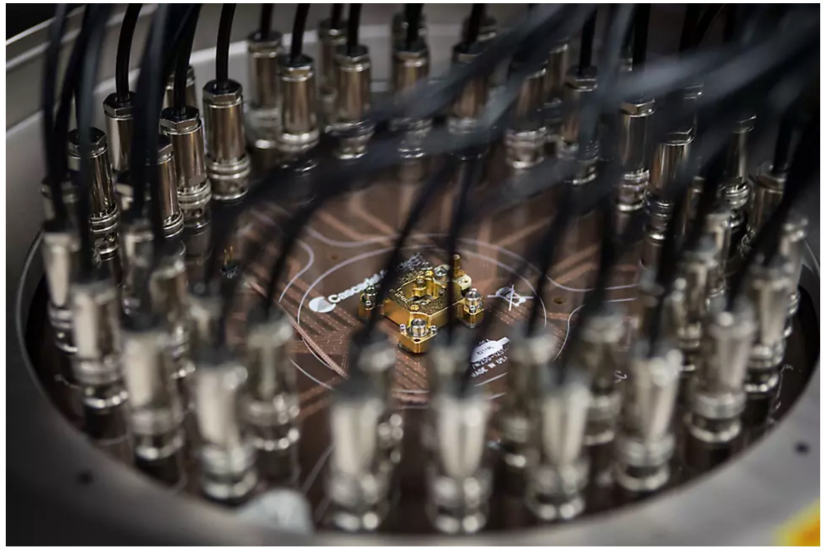


Figure 4. A Custom Probe Card with Triaxial Connectivity, Natively Supported by the NI PXIe-4135 SMU

Example: 12X Faster Test Time/Module

Diode Leakage Measurements:

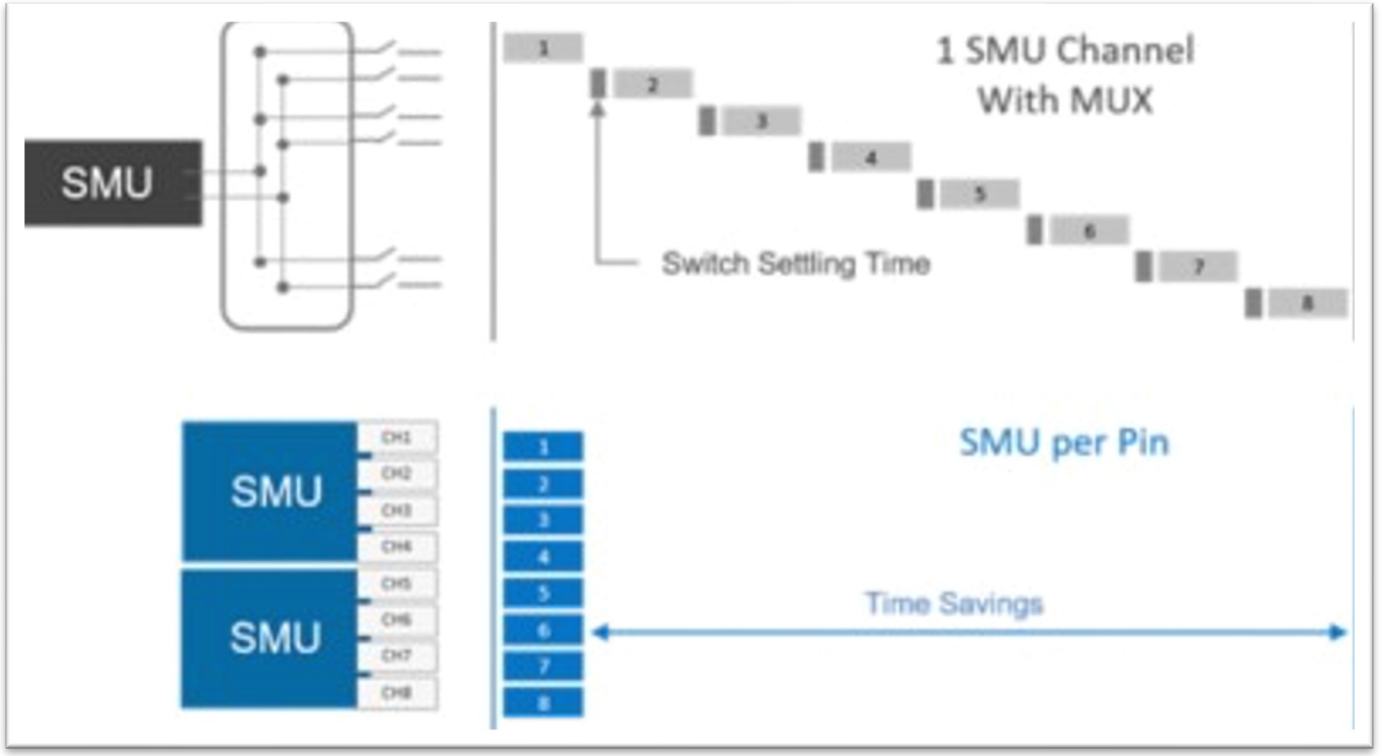
12 Diode Module -> 24 Probe pads

With Switch Matrix:

- Integration time: 32 PLC = 32x20ms = 640ms
- Settling time: 10ms
- Total test time per module: 650ms x 12 = ~7.8S

With NI Per-Pin Parallel System:

- Total test time per (12 diode) module: 640mS
- >12X faster



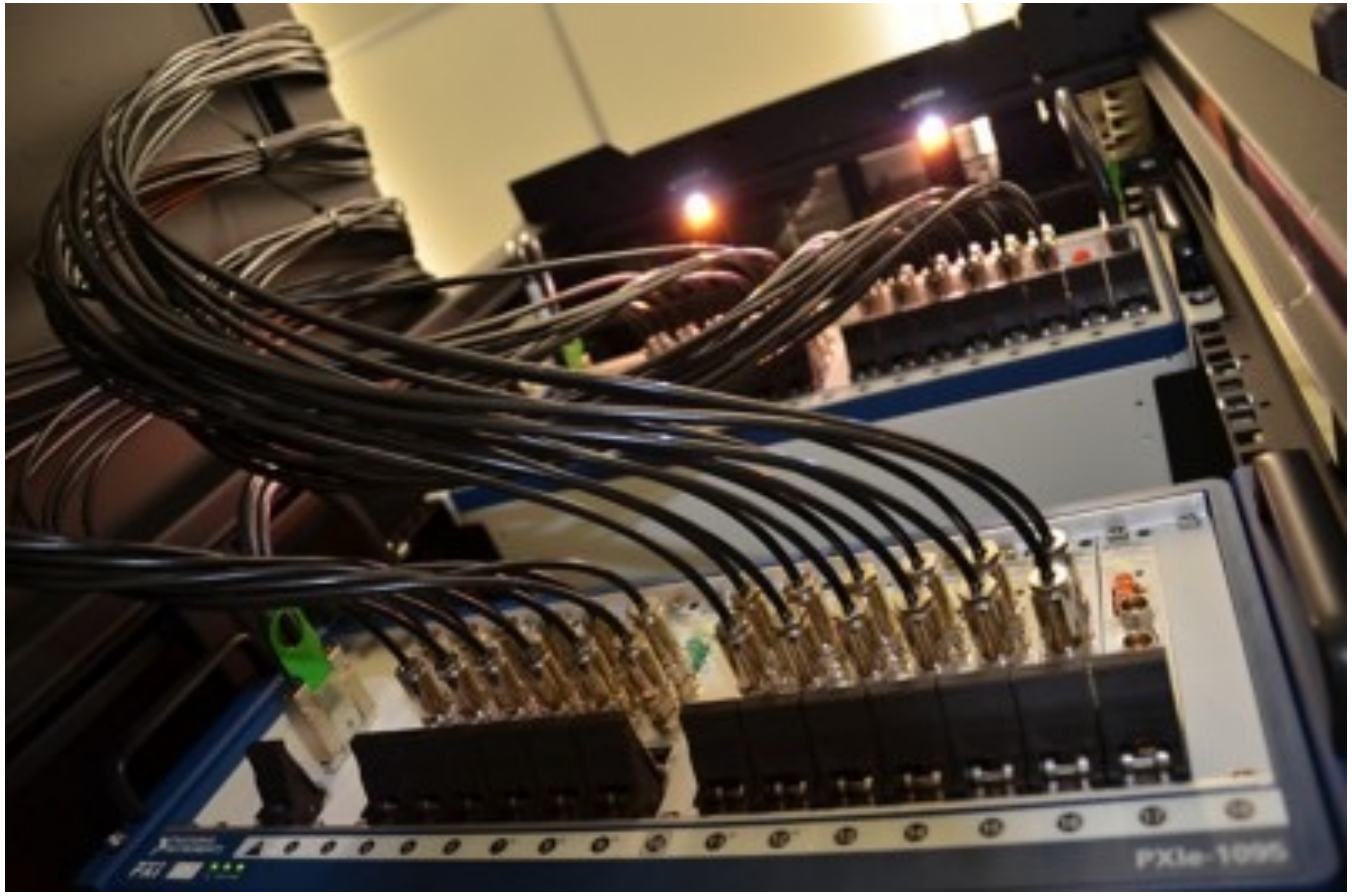
"The test-time reduction using this SMU-per-pin method is nothing short of spectacular, and wouldn’t be possible with large, traditional box SMUs. Our method eliminated switching and serialized-measurement time, reducing total test time to that of testing a single test point.”

—Bart De Wachter, imec Semiconductor Technology and Systems Group Researcher

Reducing Cost of Test & Time of Test

- **3x** Reduction in fab cycle time
- Using **24x** SMU channels
- **20 mins** per wafer from 67 minutes per wafer on traditional setup.
- Massive reduction in wafer loss
- **Increased flexibility** in measurement routines

Improvements	
Project cycle	From 1 month to 3 days
Wafer loss	From 4 wafers down to 1 wafer and wafer still valid for downstream processing
Overall wafer process cost reduction	Reduced by 75%

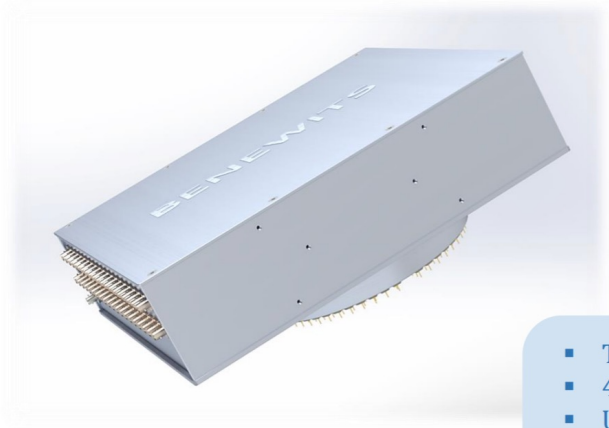


Other Examples

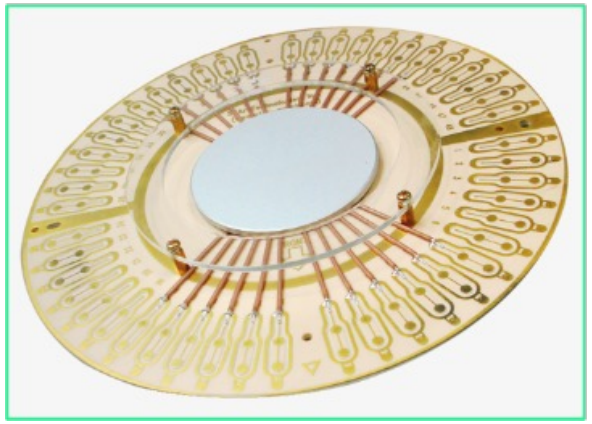
22Ch Zero-footprint WLR system

RT-9000 : *Stand-alone Solution*

High performance parallel testing with lower cost



- Test head interface for parallel test
- 4070/4080 probe card compatible
- Upgradable from 20 pins to 40 pins
- Long life design & easy maintenance



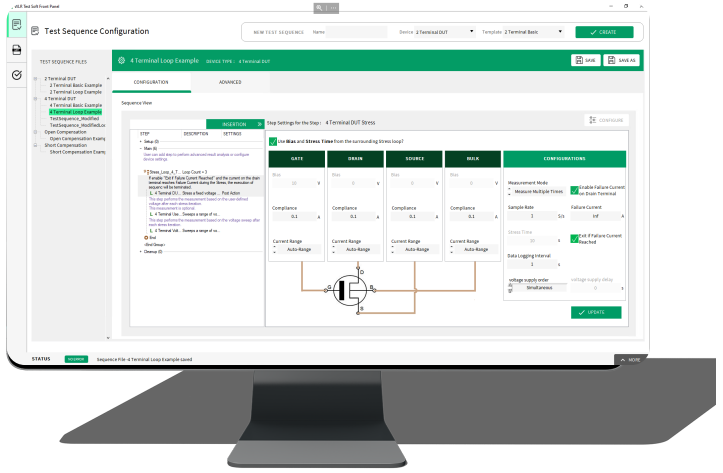
BENE WITS INTERNATIONAL

22ch – Zero-footprint WLR System

96 Ch Highly Parallel WLR System

- Best-in-class measurement speed with NI PXI
- Zero-Switching Solution, Per-pin parallel SMU Architecture

- Optimized for IV (SMU) Testing
- Reduce # of Probe Cells on Test Floor



NI PTS Solution

Parametric Test System

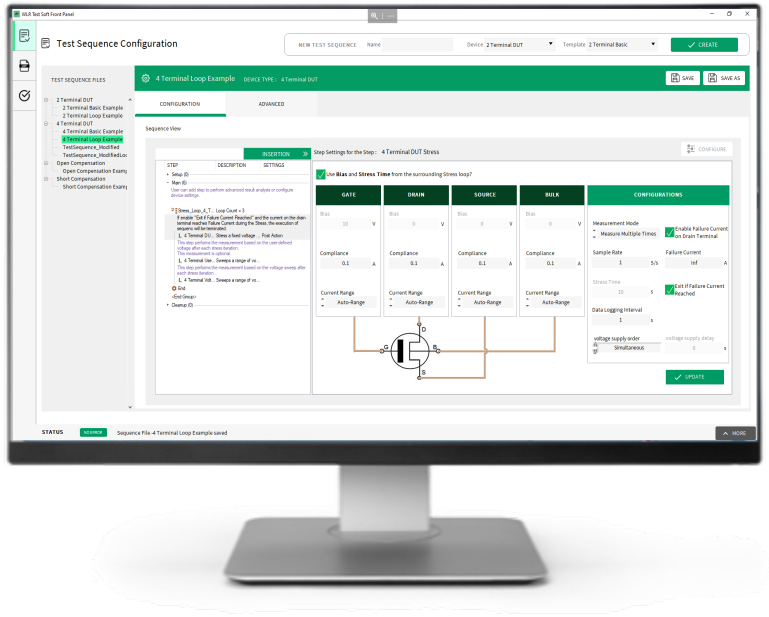
- Up to 50 channels of precision fA-class SMUs (per pin)
  - 200V/1A, 40W
  - Extended pulsing capabilities
- Zero-Switching Solution

Benefits

- Build high-throughput, flexible systems with our massively-parallel SMU-Per-Pin System architecture and scalability
- Deploy custom reliability algorithms leveraging our WLR APIs
- Quickly perform JEDEC compliant reliability measurements without coding through WLR Soft Front Panel

Software

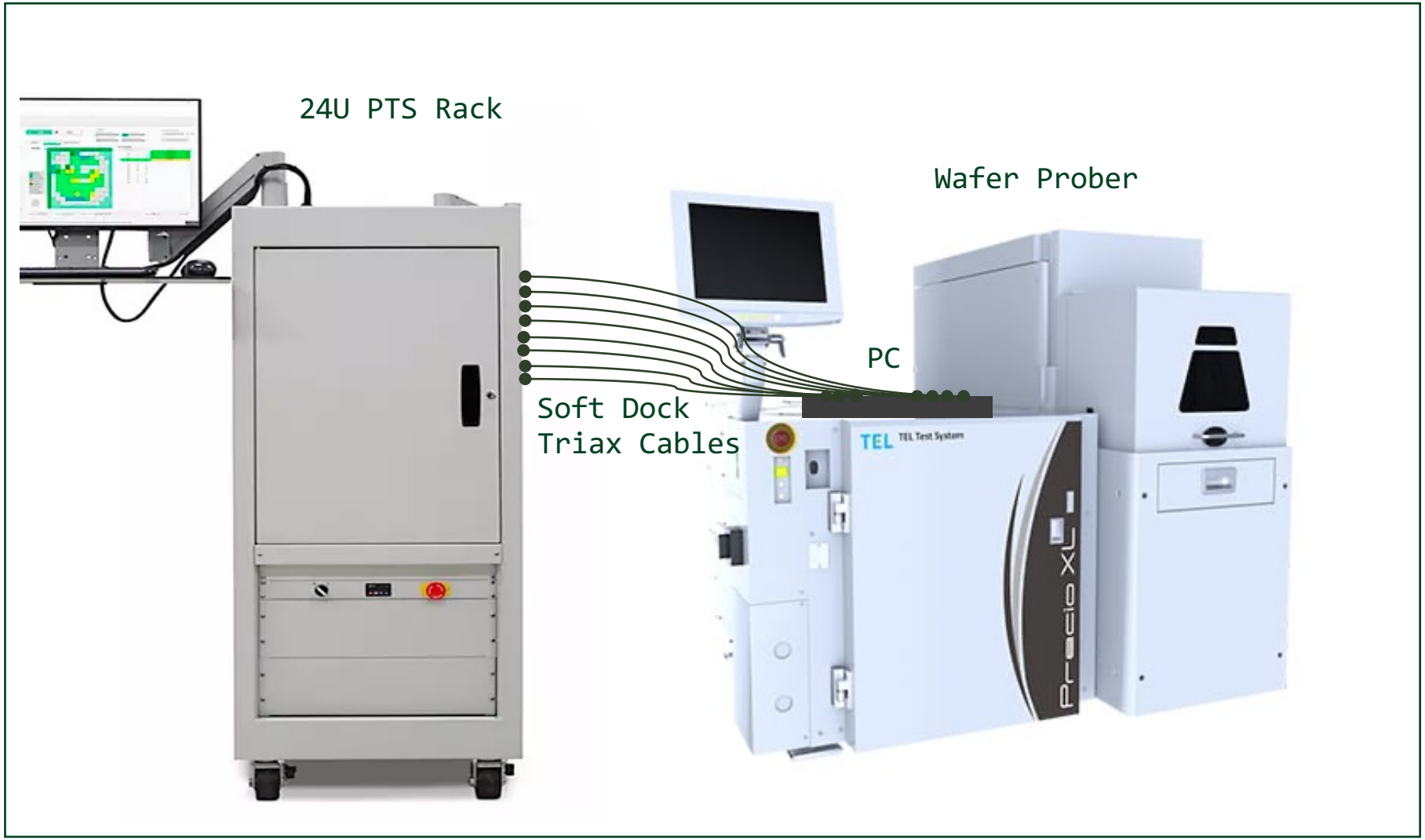
- **"PTS Soft Front Panel"** GUI Application Software containing:
  - Industry-standard test sequencer with prebuilt step templates compliant with JEDEC methodologies (TDDB, BTI, HCI)
  - Built-in database tool for logging and generating reports
  - Customizable operator interface for live debug and monitoring
  - Abstracted parallelism and multithreading functionality
  - Wafer Mapping and Prober Recipe Editor
- **APIs** in **C#, Python, and LabVIEW** for custom development



Test Software

"PTS" Parametric Test Systems

PTS Test Cell Example



PXIe-4190
LCR Meter and SMU

NI's new LCR & SMU ensures the speed, accuracy, usability, and repeatability needed to efficiently perform DC and impedance measurements in a variety of applications.

Product Variants
2 MHz Variant
500 kHz Variant

Key Features

LCR Meter with fF-class capacitance measurements

- Frequency: 40 Hz – 2 MHz
- DC bias: ± 40 V (AC + DC), ± 100 mA
- AC Stimulus: Up to 7.07 Vrms
- Basic Impedance Accuracy: 0.05%

SMU with fA-class current measurements

- ± 40 V, ± 100 mA
- 1 fA sensitivity with best-in-class noise performance

Connectivity

- Triaxial, Coaxial breakout cable options

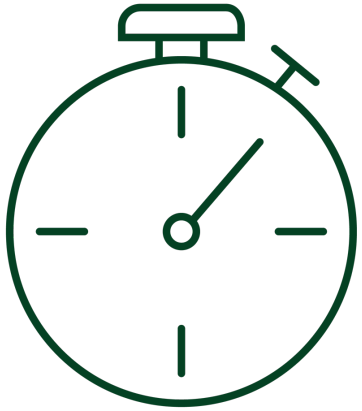
Software

- NI-DCPower driver with added LCR measurement API
- Support for LabVIEW, C, C# .NET, Python

Chassis Support

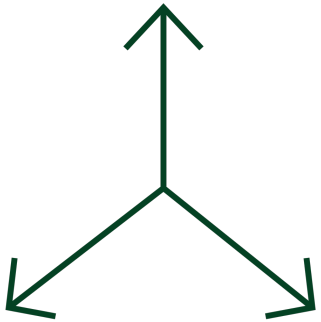
- Supported by all 58W+ cooling chassis

NI Solution Benefits



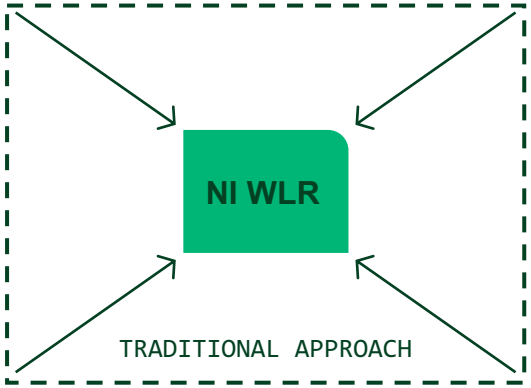
Data Velocity/Throughput

Shorten WLR test cycles from months to days with industry-leading parallelism and measurement speed.



Flexibility

Configurable and upgradeable channel count (up to 100 channels per rack) in a highly flexible SMU-per-pin architecture.



Size / Footprint

Industry-leading channel density and flexible rack size options help optimize use of floor space and minimize power consumption.

Questions