NI CONNECT 2023 AUSTIN

Product Launch

PXIe-7903

Presented by:
James Thornton
Sean Ferguson

Introduction: James Thornton

Senior Product Manager

Platform Product Management

Experience:

- National Instruments (1+ year)
  - Products Managed
    - ATE CC, PXI Systems, GPIB, Serial, C-series controllers and Chassis
- Engineering Automation (6 years)
  - Roles
    - R&D Engineering, Technical Sales, Product Management

Introduction: Sean Ferguson

Principal Software Engineer – System R&D

Aerospace Defense & Government

Agenda

Introduction ……..(1 mins)

What is FlexRIO? ……(12 mins)

FlexRIO-7903 ……..(12 mins)

- Features and Functions
- Target Applications

Technical Deep Dive

- LabView FPGA Implementation……...(25 mins)
  - Demo

Q & A ……..……(10 mins)

Today's Industry Challenges

INCREASING COMPLEXITY

CHANGING REQUIREMENTS

LACK OF MANPOWER

UNREALISTIC SCHEDULES

Think Outside the Box

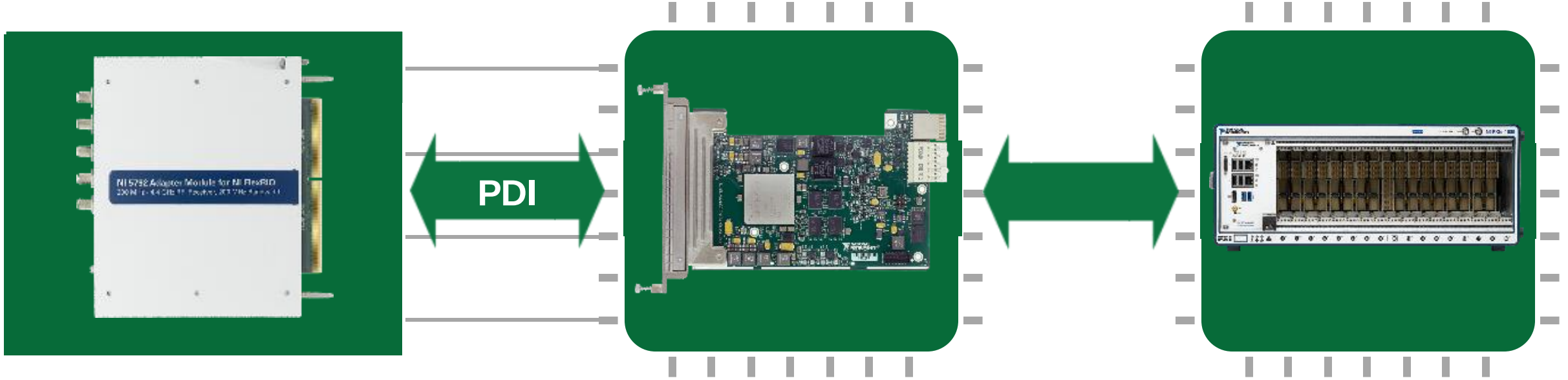
FlexRIO

- Target Applications
  - High speed data converters
  - Custom digital interfacing
  - Real time digital signal processing
  - AND MORE!

- Key Benefits
  - Fully configurable
  - High-speed analog, digital, and RF I/O
  - Accelerate FPGA Programming
    - LabView
  - Uses timing and synchronization capabilities of PXI
    - Synchronize Multiple Modules

Hardware Architecture

FlexRIO with Modular I/O System Architecture



FlexRIO Adapter Module

Interchangeable I/O
Analog, Digital, RF
Custom I/O with MDK

FlexRIO FPGA Module

Kintex-7 FPGA
Up to 2 GB of DRAM
PCIe Gen 2 x 8
Peer-to-peer streaming
(adds inline DSP)

PXI Backplane

Embedded Controllers
Synchronization
Data streaming
Power/cooling

A Wide Variety of FlexRIO I/O

Digital


100 Mbps
SE DIO


300 Mbps
LVDS DIO


300 Mbps
SE/LVDS DIO


1 Gbps
LVDS DIO


Camera Link


RS-485/422

Digitizers


2 ch. 3 GS/s
8-bit AI


2 ch. 1.6 GS/s
12-bit AI


4 ch. 250 MS/s
14-bit AI


2 ch. 250 MS/s
16-bit AI


16 ch. 120 MS/s
16-bit AI


4 ch. 120 MS/s
16-bit AI


32 ch. 50 MS/s
12-bit AI


2 ch. 80 MS/s
14-bit AI


2 ch. 120 MS/s
16-bit AI


2 ch. 40 MS/s
12-bit AI


16 ch. 50 MS/s,
14-bit AI

RF


100MHz BW
4.4 GHz RF I/O


200MHz BW
4.4 GHz RF Tx


200MHz BW
4.4 GHz RF Rx

Transceivers


2 ch. 100 MS/s
14-bit AI
16-bit AO


2 ch. 250 MS/s
14-bit AI
16-bit AO


4 ch. 100 MS/s
16-bit AI
16-bit AO

Signal Generators


2 ch. 1.25 GS/s
14-bit AO

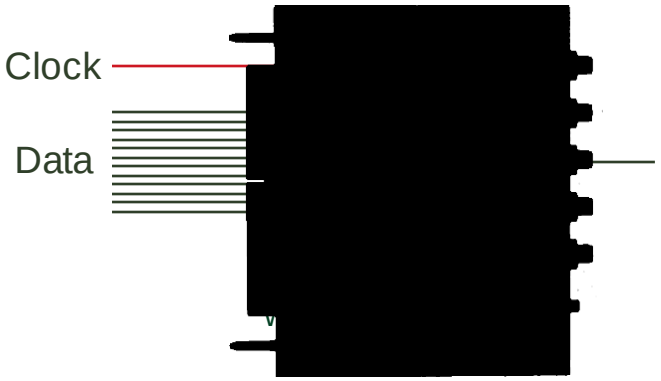

1 ch. 2 GS/s
14-bit AO


32 ch. 1MS/s
16-bit AO


16 ch. 1MS/s
16-bit AO

The Move to High-Speed Serial

Traditional Converters



Uses FPGA GPIO
LVDS bit rates up to ~1.25 Gbps
Difficult to meet static timing

High-speed Serial Converters

12-bit ADC
with JESD204B Interface

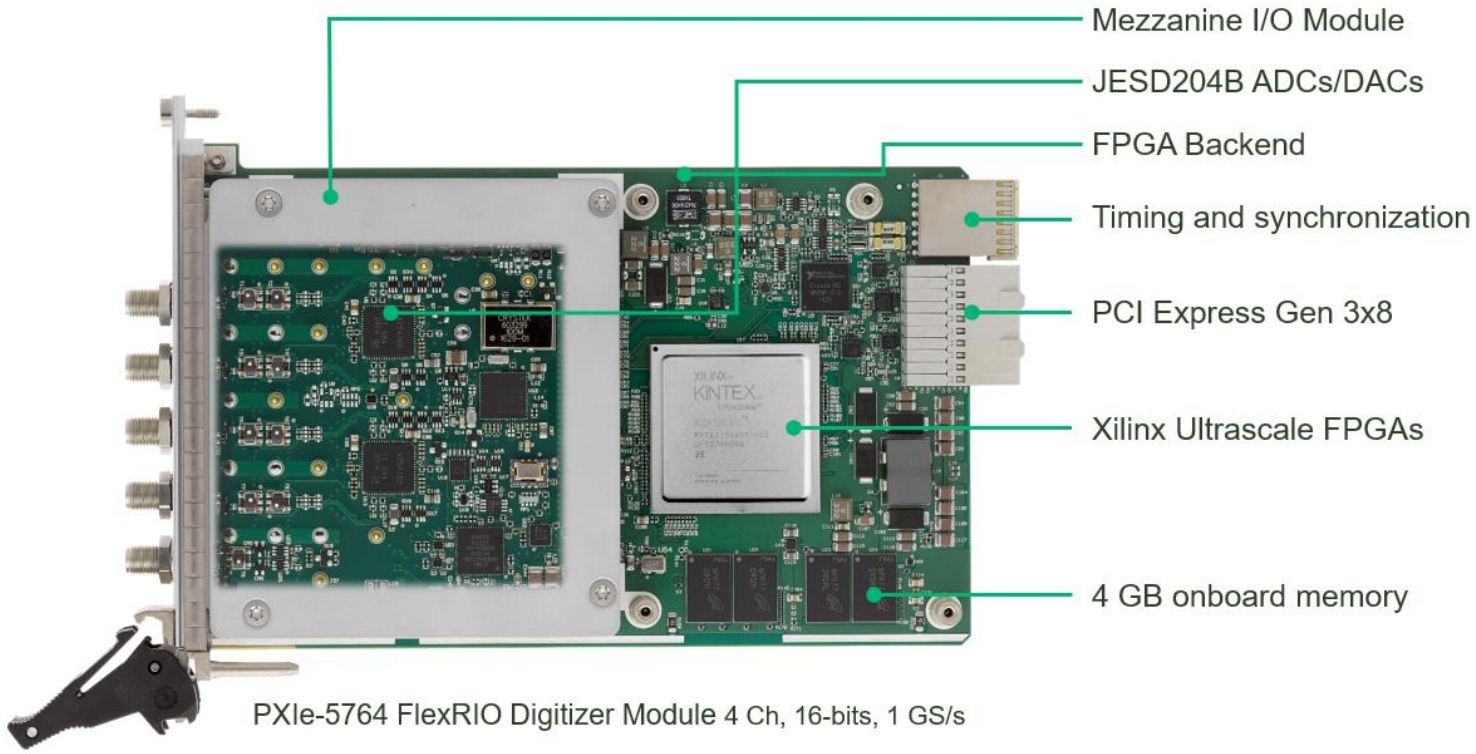
Uses FPGA Multigigabit Transceivers (MGTs)
MGT line rates up to 12.5 Gbps
Defined by JESD204B standard*

- Modular Architecture well suited for **digital interfacing** and **communication** with converters over LVDS
- Converter manufacturers moving to high-speed serial interfaces **with highest performance parts**
- Solves common issues with parallel busses
  - Ex: meeting static timing at higher clock rates

FlexRIO Architectures

High-Speed Serial Converters, Integrated I/O

- Second FlexRIO architecture
- Mezzanine I/O module communicates with FPGA via high-speed serial communication
- Xilinx UltraScale FPGAs
- JESD204B interface standard
  - Supports high bandwidth, high performance, high speed, and multi-channel applications



PXIe-5764 FlexRIO Digitizer Module 4 Ch, 16-bits, 1 GS/s

FlexRIO with Integrated I/O

High-Speed Serial

25 Gbps per lane

16 Gbps per lane

PXIe-7903

Digitizers

4 ch. 500 MS/s
16-bit AI

4 ch. 1 GS/s
16-bit AI

2 ch. 6.4 GS/s
12-bit AI
DC and AC Coupled Variants

Transceivers

2x2 ch. 6.4 GS/s
12-bit AI & AO

Coprocessors

50780 FPGA
Slices

60600 FPGA
Slices

82920 FPGA
Slices

Signal Generators

2 ch. 6.4 GS/s
12-bit AO

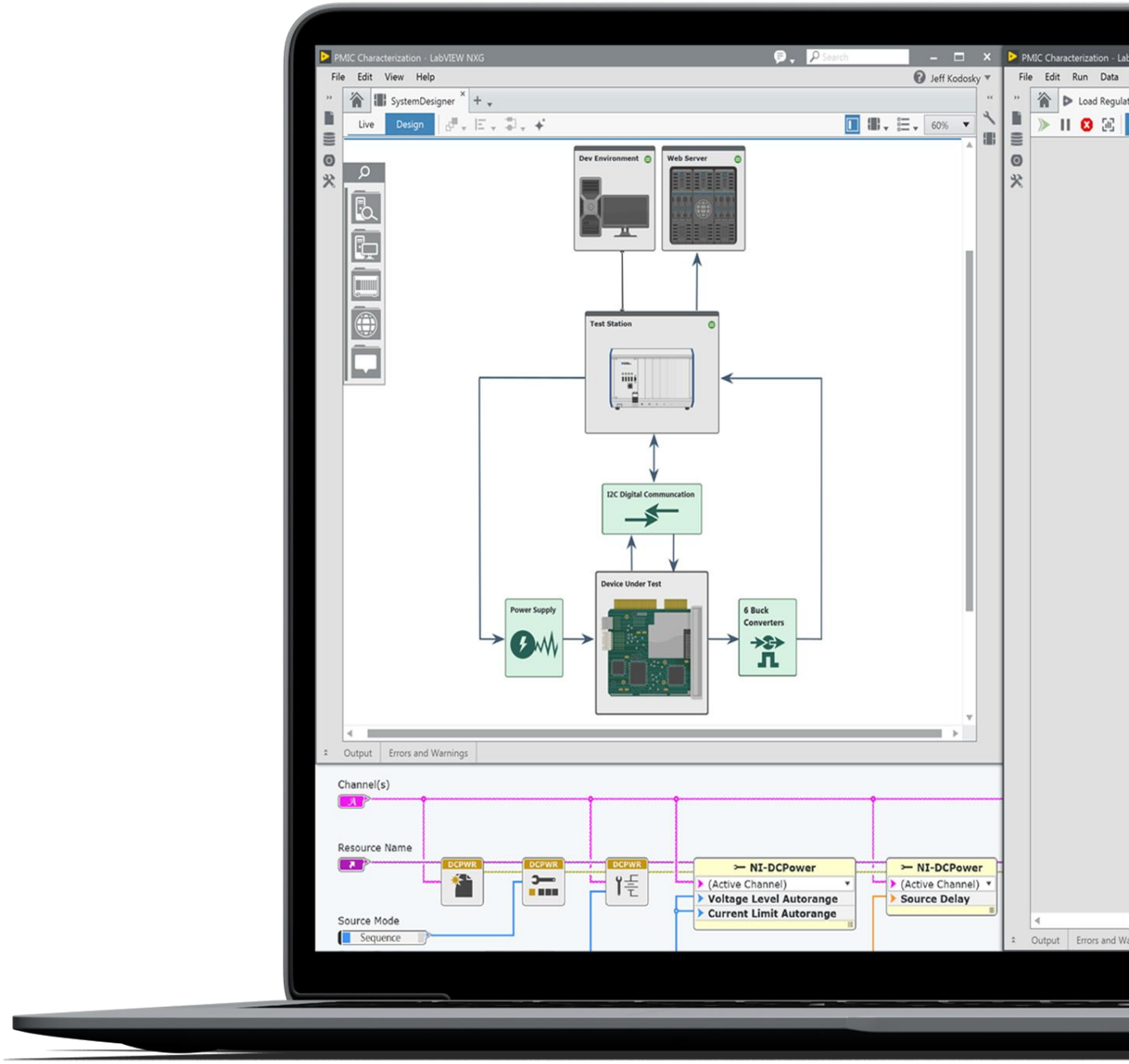
35+ Modules!

Software and IP

Built for Engineering Productivity

We let you focus on solving your biggest engineering challenges by:

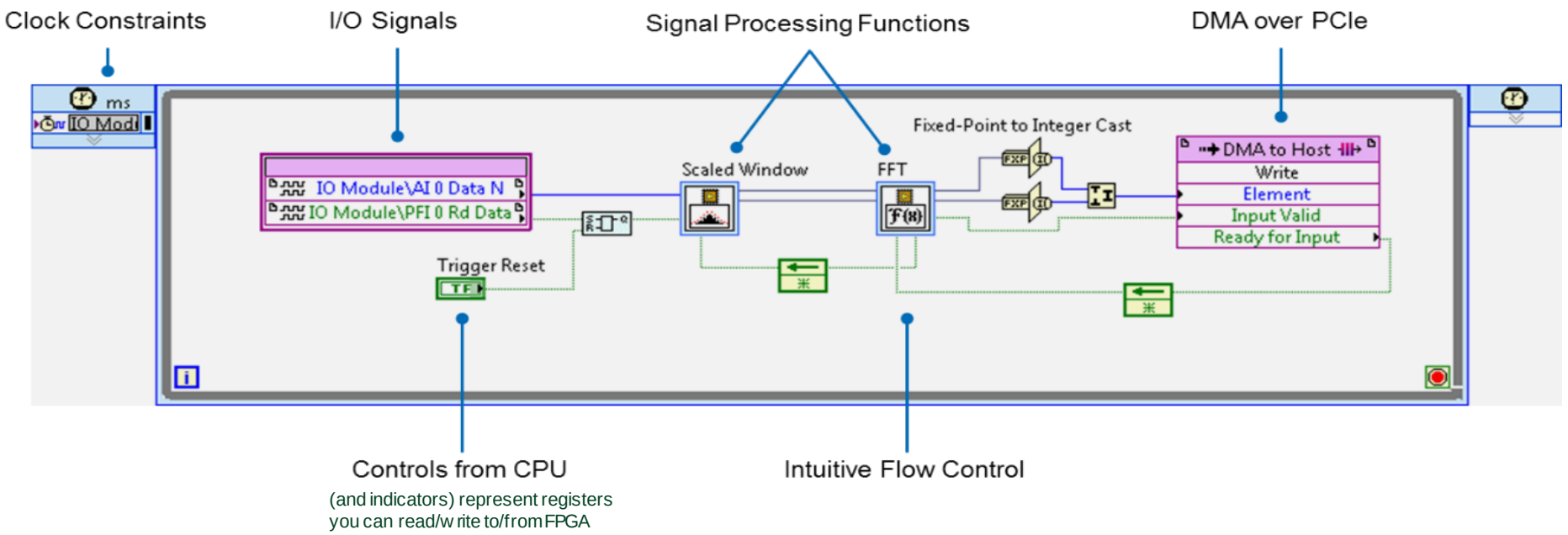
- **Accelerating development** with intuitive graphical programming
- Providing unparalleled hardware connectivity and measurement IP that gets you to **faster measurement results**
- Scaling from simple applications to large team development



A *Quick* Look at LabVIEW FPGA

- Helps you **develop** and **debug** custom hardware logic that you can compile and deploy to NI FPGA hardware
- More **efficiently** and **effectively** design FPGA-based system
  - IP libraries, high fidelity simulator, and debugging features

- The single-cycle Timed Loop was specifically created to write more efficient LabVIEW FPGA code and it specifies the clock rate and domain that will be used to execute the logic inside it.

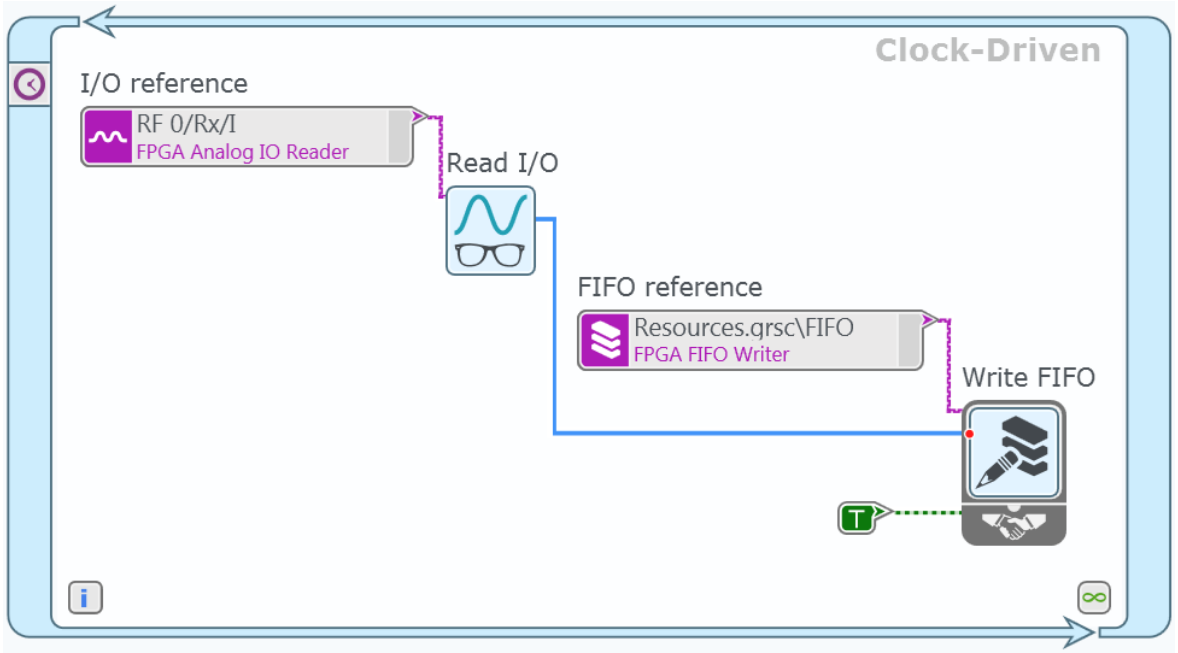


Example

- Code needed to read from an ADC and send that to a host PC through the PCIe bus via a DMA FIFO

~4000 lines of VHDL

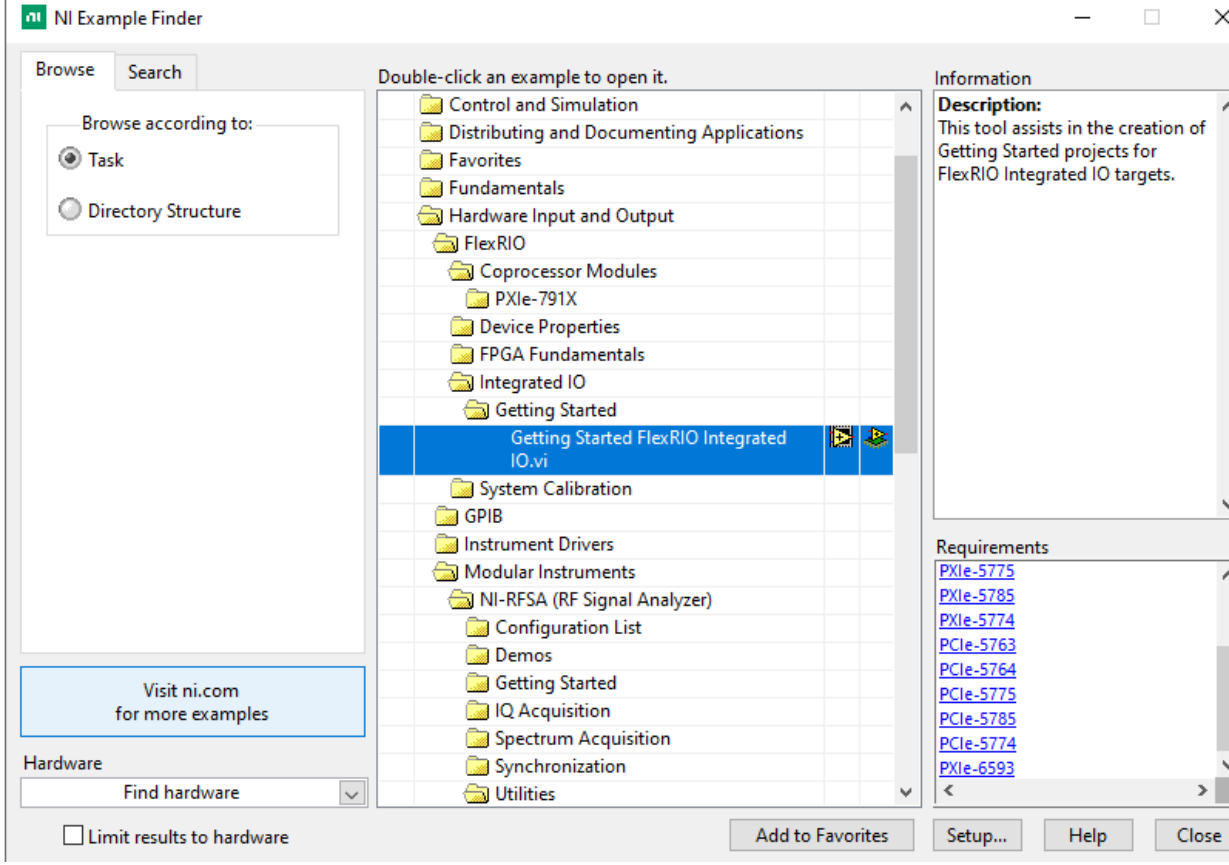
VHDL



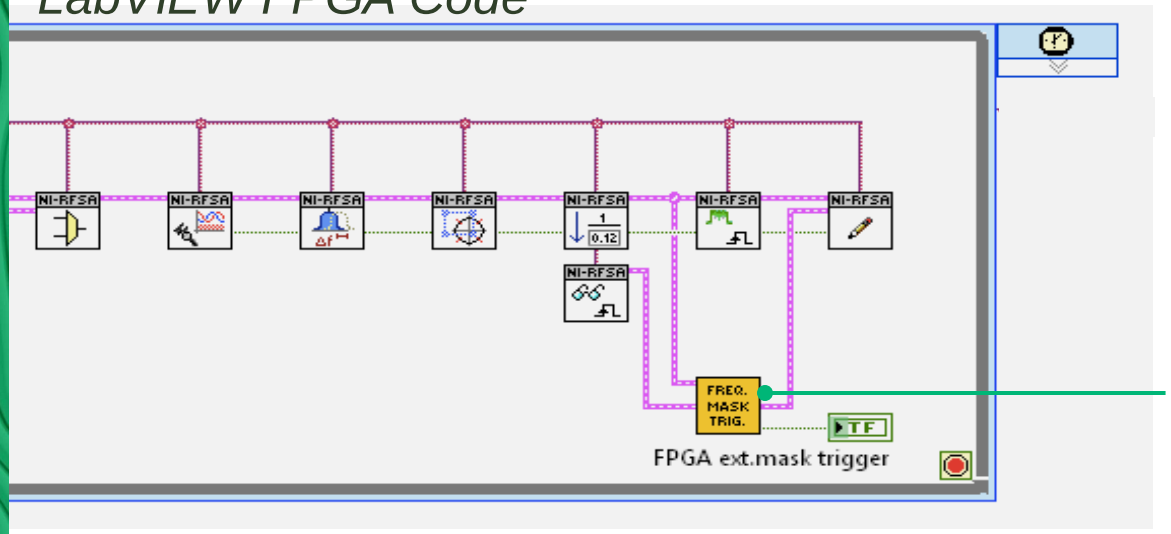
LabVIEW FPGA

Example Finder

- NI provides Example Finder with a built-in filter capability that helps list out all examples that are **applicable** for specific device **models**.



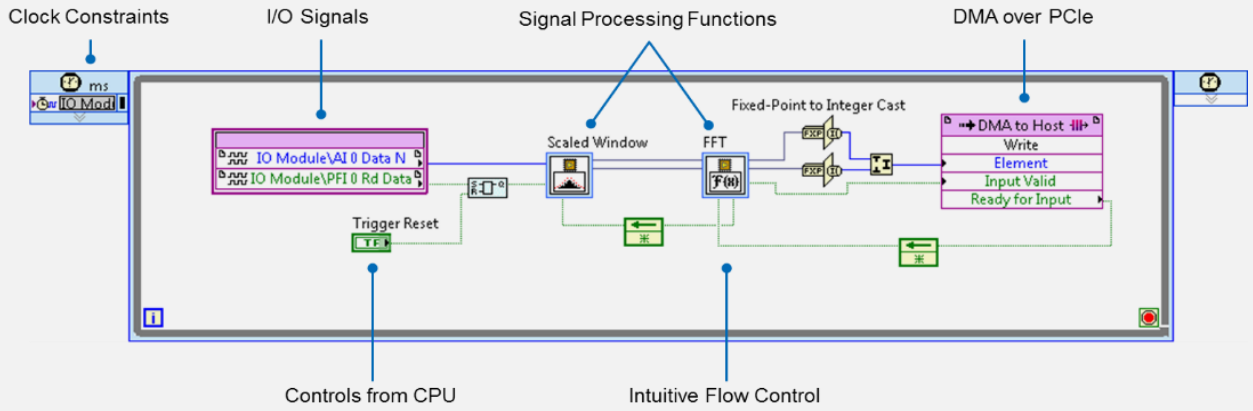
LabVIEW FPGA Code



Application-specific functions

LabVIEW FPGA IP Library

Focus on your algorithms, not infrastructure



Get to a solution faster with extensive libraries of FPGA IP

LabVIEW FPGA IP Commonly used with FlexRIO		
10 Gigabit Ethernet UDP	Edge detection	Persistence display
3-Phase PLL	Equalization	PFT channelizer
Accumulator	Exponential	PID
All-digital PLL	FFT	Pipeline frequency transform (PFT)
Area measurements	Filtering	Polar to X/Y conversion
Bayer decoding	FIR compiler	Power level trigger
Binary morphology	Fixed-point filter design	Power servoing
Binary object detection	Fractional interpolator	Power spectrum
BRAM delay	Fractional resampler	Programmable filter
BRAM FIFO	Frequency domain measurements	Pulse measurements
BRAM packetizer	Frequency mask trigger	Reciprocal
Butterworth filter	Frequency shift	RFFE
Centroid calculation	Halfband decimator	Rising/falling edge detect
Channel emulation	Handshake	RS-232
Channel power	Hardware test sequencer	Scaled window
CIC compiler	I2C	Shading correction
Color extraction	Image operators	Sin & Cos
Color space conversion	Image transforms	Spectrogram
Complex multiply	Instruction sequencer	SPI
Corner detection	IQ impairment correction	Square root
Counters	Line detection	Streaming controller
D latch	Linear interpolation	Streaming IDL
Delay	Lock-in amplifier filter	Synchronous latch
Digital gain	Log	Trigger IDL
Digital pre-distortion	Matrix multiply	Unit delay
Digital pulse processing filter	Matrix transpose	VITA-49 data packing
Discrete delay	Mean, Var, Std deviation	Waveform generation
Discrete normalized integrator	Memory IDL	Waveform match trigger
Divide	Moving average	Waveform math
Dot product	N channel DDC	X/Y to polar conversion
DPO	Natural log	Xilinx Aurora
DRAM FIFO IDL	Noise generation	Zero crossing
DRAM packetizer	Normalized square	Zero order hold
DSP48 node	Notch filter	Z-Transform delay
DUC/DDC compiler		

Product Announcement

PXIe-7903

High Speed Serial

FlexRIO Coprocessor

2-Slot FlexRIO Coprocessor

NI's most powerful, highest speed, PXI FPGA coprocessor, built to maximize data movement and computational power.

PXIe-7903

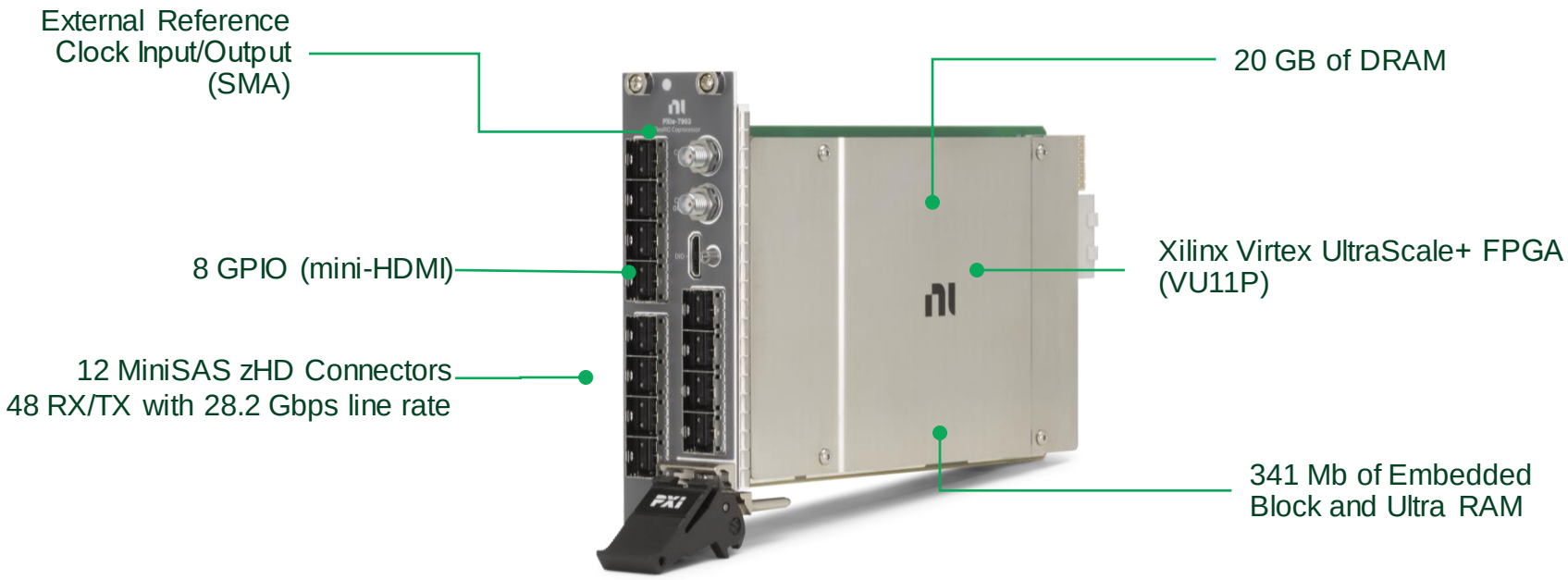
Features

- 12 MiniSAS zHD Connectors
  - 48 RX/TX with 28.2 Gbps line rate
- External Reference Clock Input/Output
- Xilinx Virtex UltraScale+ VU11P FPGA
  - 9,200+ dsp slices
- 20 GB of DRAM (10 GB per bank) w/ up to 25 GB/s write speed
- 8-port DIO terminal (mini-HDMI)
- PCI Express Gen 3x8
- 341 Mb of Embedded Block and Ultra RAM
- Data movement with Ethernet protocols
  - 100 GbE (previously 10 was limit)
  - Aurora 64b/66b

FlexRIO PXIe-7903 FPGA Coprocessor

Target Applications

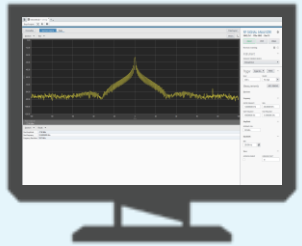
- Radar Target Generation
- Beamforming RF Signals
- Spectral Stitching RF Instruments
- Real-time Spectrum Analysis
- Electronically scanned array characterization
- Multi-channel RF record and playback

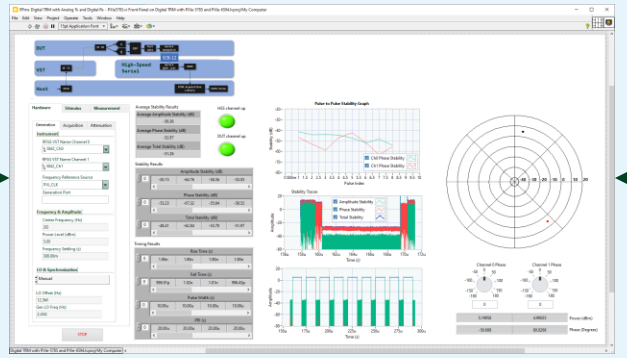


Example Applications

Electronically Scanned Array Characterization

MEASUREMENT SOFTWARE





Creates synthetic RF + Digital test instrument capable of a wide variety of RF parametric and application measurements

NI SYSTEM

RFSA/G/mx

PXIe-5842

VST

VST

RFSA

RFSG

Triggering and Sync

PXIe-7903

Acquisition Library

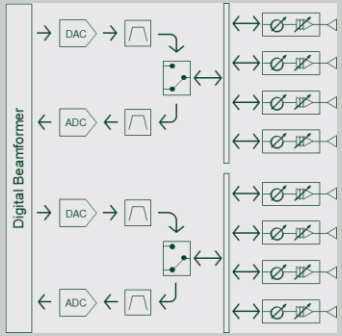
Waveform Engine

DUT Control

HSS/LVDS

Digital Interface

SUT



RF Interface

AI0

AI1

AO0

AO1

ADC0

ADC1

DAC0

DAC1

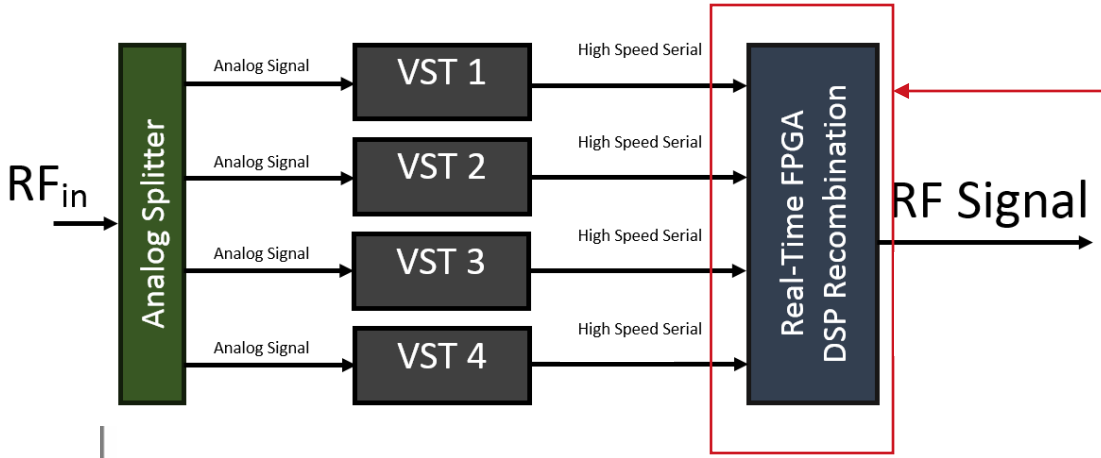
DSP

Digital Interface

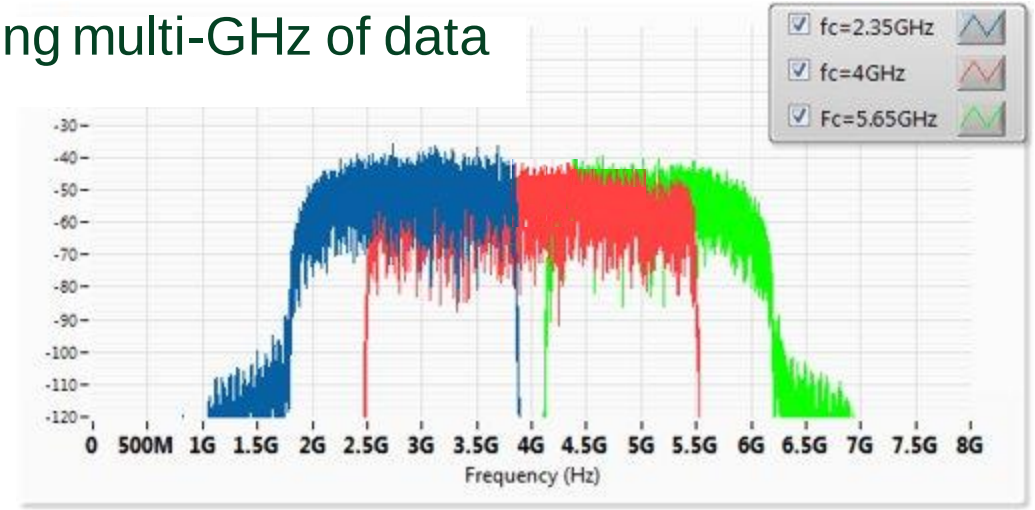
SUT = PXIe-5785 Digital Transceiver

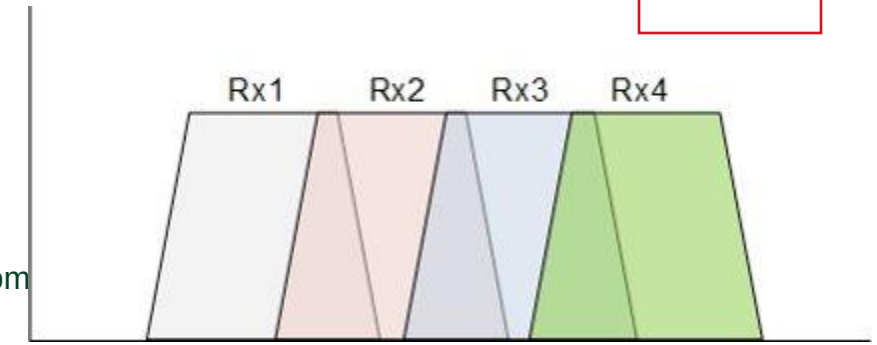
Spectral Stitching

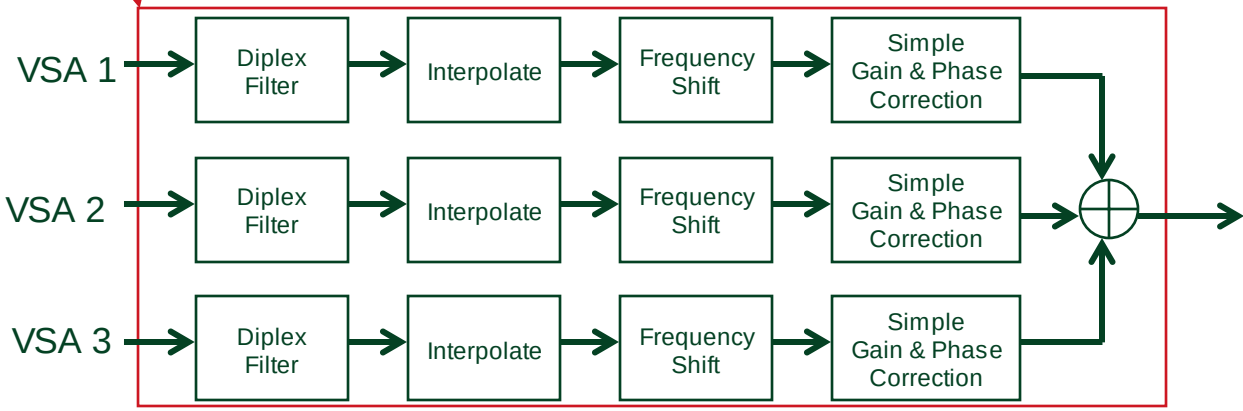
- Combine multiple RF devices together such that they appear as one device
- Happens in real time
- Systems capable of continuously processing and storing multi-GHz of data
- Lots of filters and dsp (math intensive)
  - VU11P has 9,200+ dsp slices



PXIe-7903



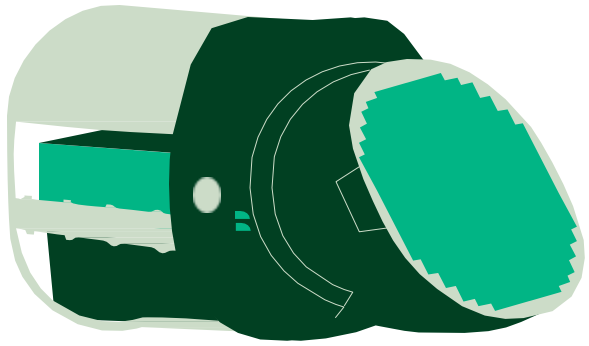




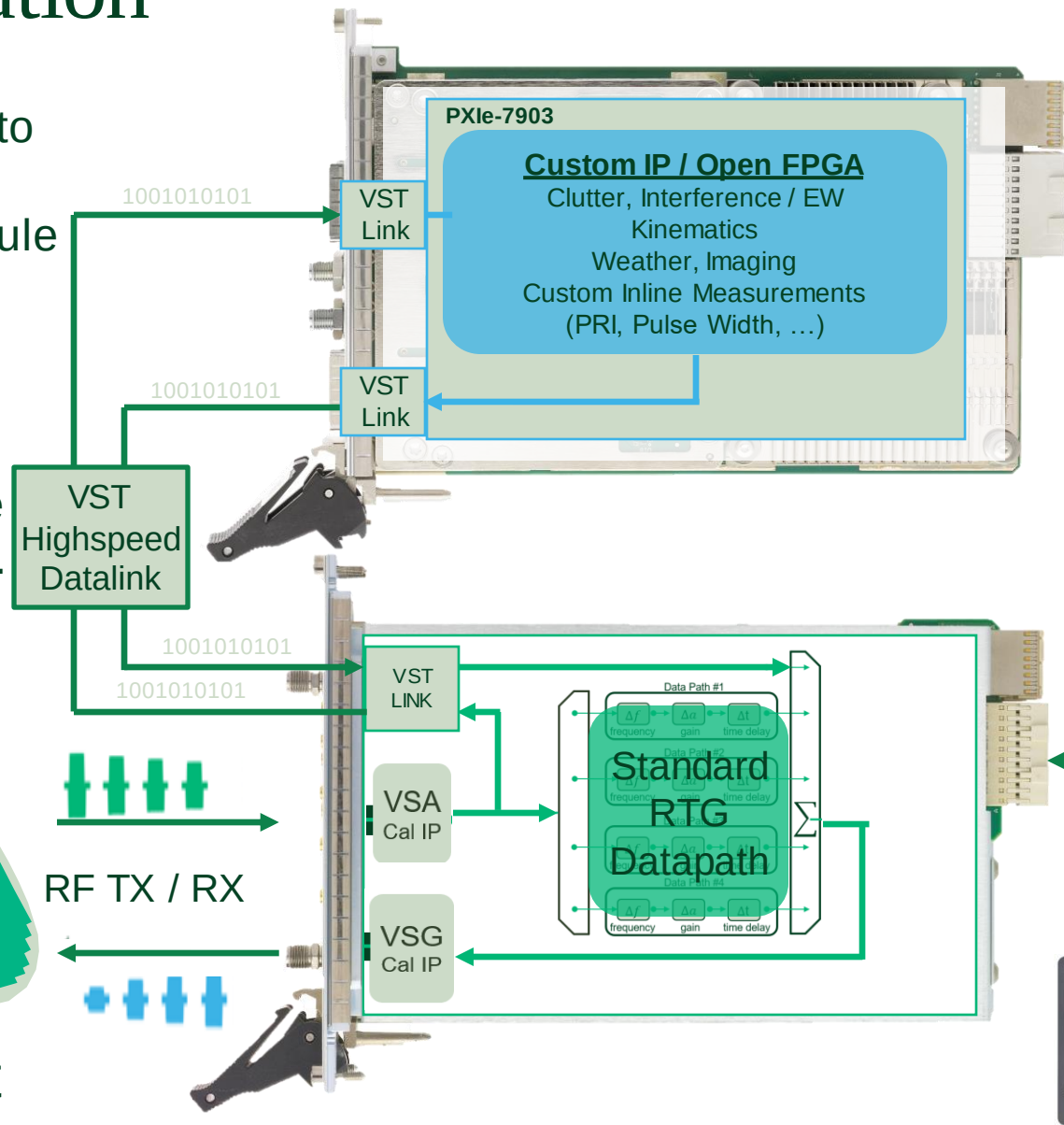
Radar Target Generation

- Latency – time it takes for a radar wave to travel from system to target and back
- VST houses radar target generator module
  - Radar process, RF DSP, correcting input and output signals, etc.

- FlexRIO Coprocessor
  - Enables custom IP integration while retaining calibration of NI RTG core.



Radar Under Test



Case Study & Demo

Multichannel RF Record & Playback Solution

RF / Digital Systems Performance

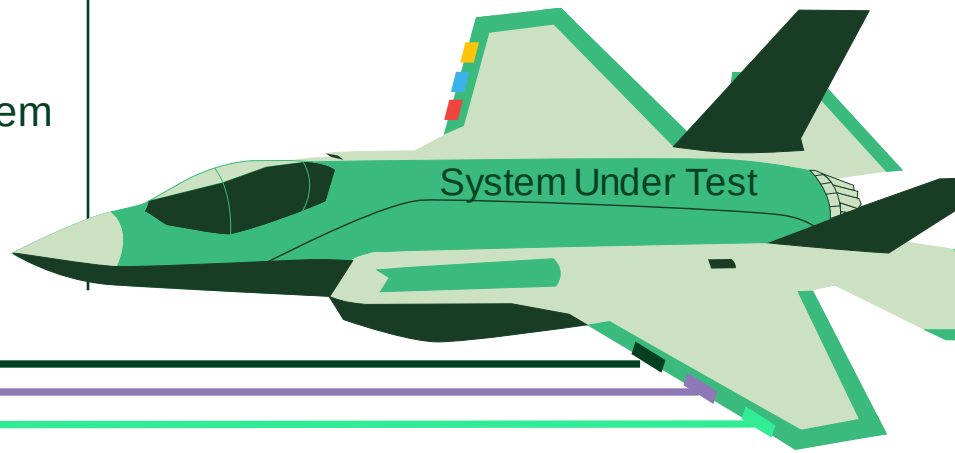
- Wideband RF Recording
  - 1 GHz IBW per channel
- 100 GbE Stream To Disk
  - 40 GB/s (8 GHz IBW)
    360 TB = 2.5 hours at max IBW
- Multi-Channel / Frequency
- Select Partner/Customer Inline or Parallel Processing
- Offline Analysis

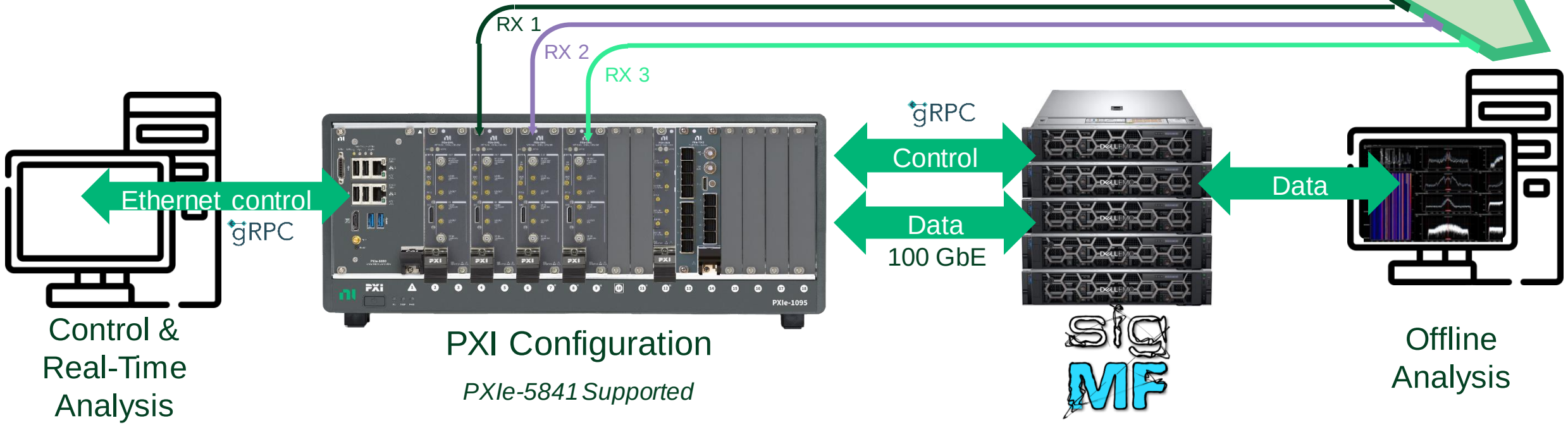
System Calibration & Sync

- Time Synchronization w/ NI-TClk
- Record Trigger Options
  - Software, Digital
- LO Power Calibration
- Wideband Multi-Channel System Equalization Calibration

System Software

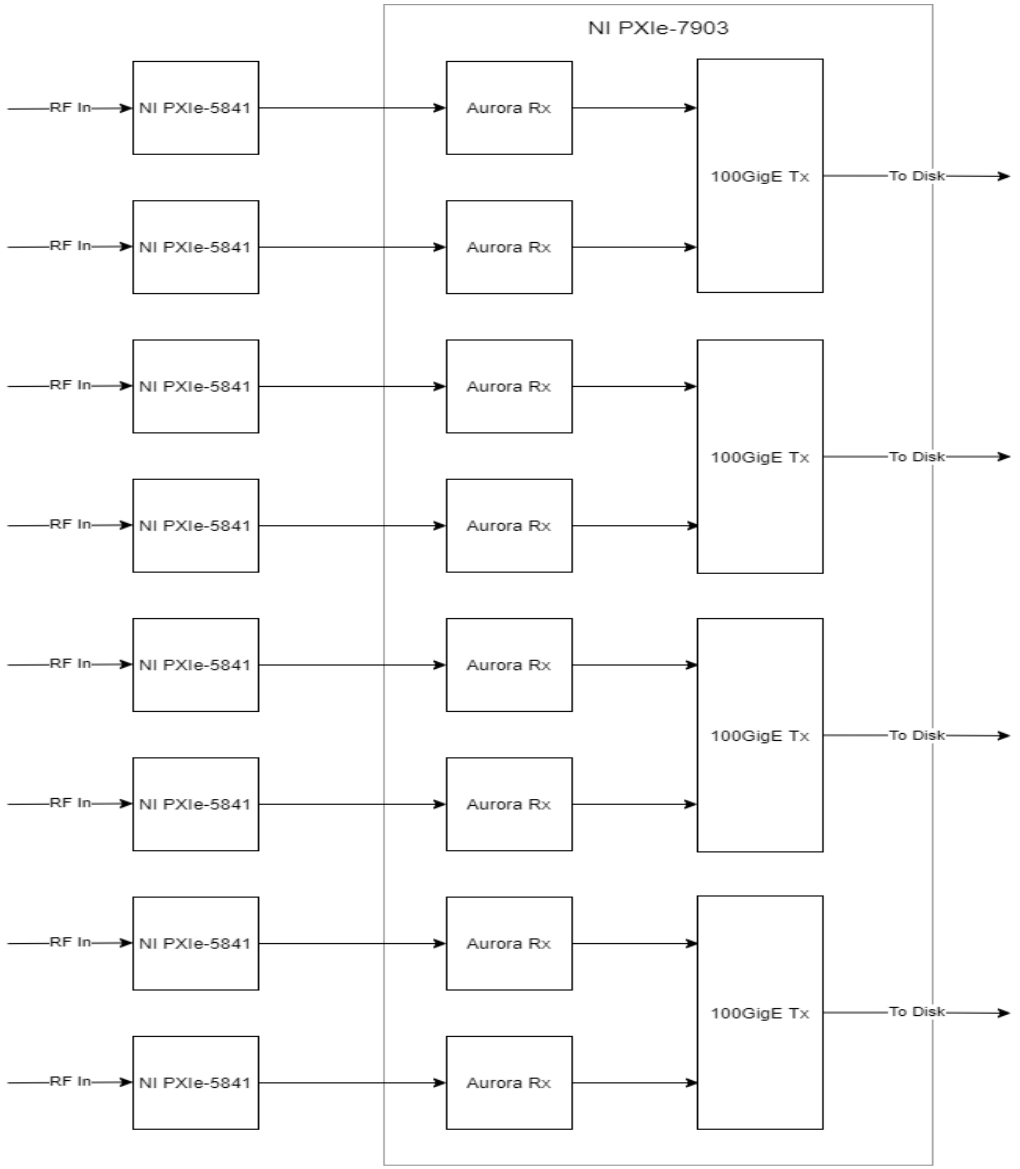
- Remote-access with gRPC
- SigMF metadata file format





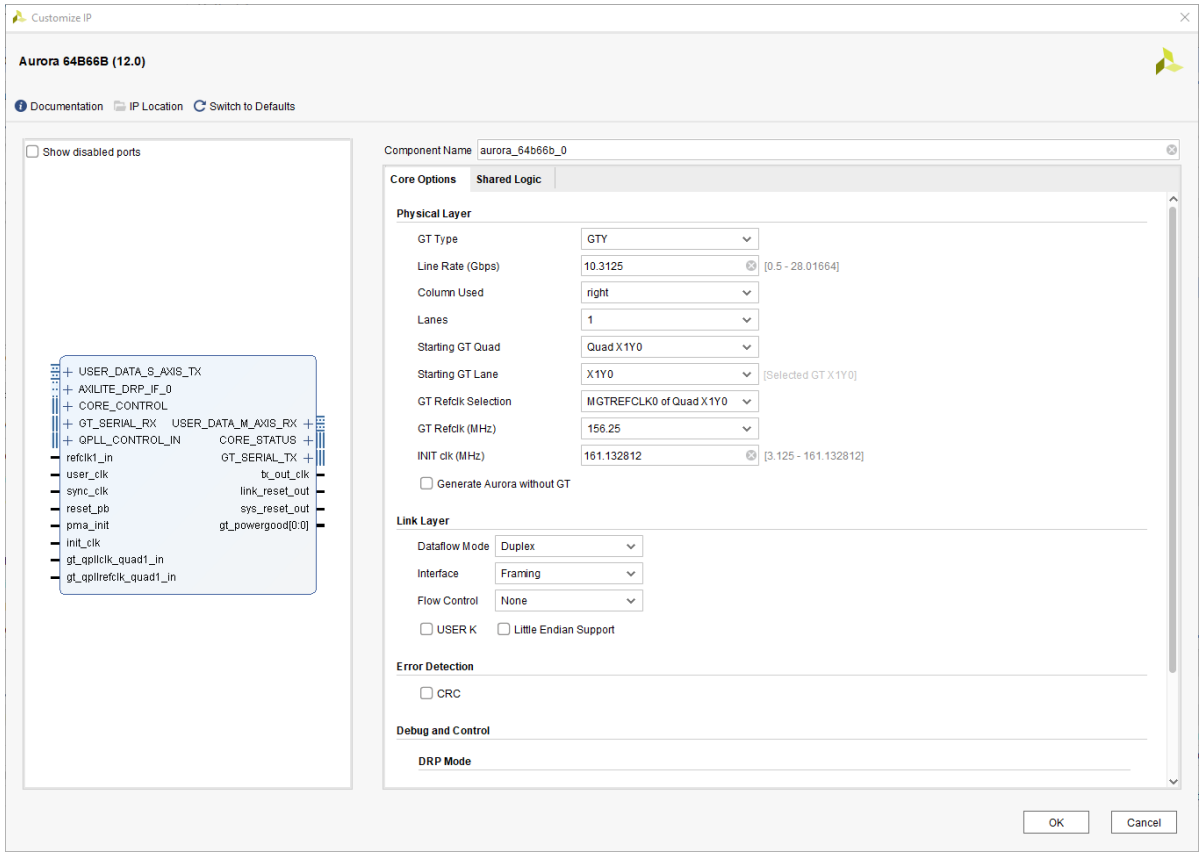
Case Study - Record (& Playback)

- Synchronized RF data is acquired on eight NI PXIe-5841 1 GHz Vector Signal Transceivers
- The IQ data acquired on each NI PXIe-5841 is written to a 4-lane Aurora 64b/66b interface and streamed to a NI PXIe-7903 FPGA co-processor.
- The NI PXIe-7903 multiplexes the IQ data from a pair of 4-lane Aurora interfaces into a single 100GigE UDP packet, for a total of four 100GigE interfaces.



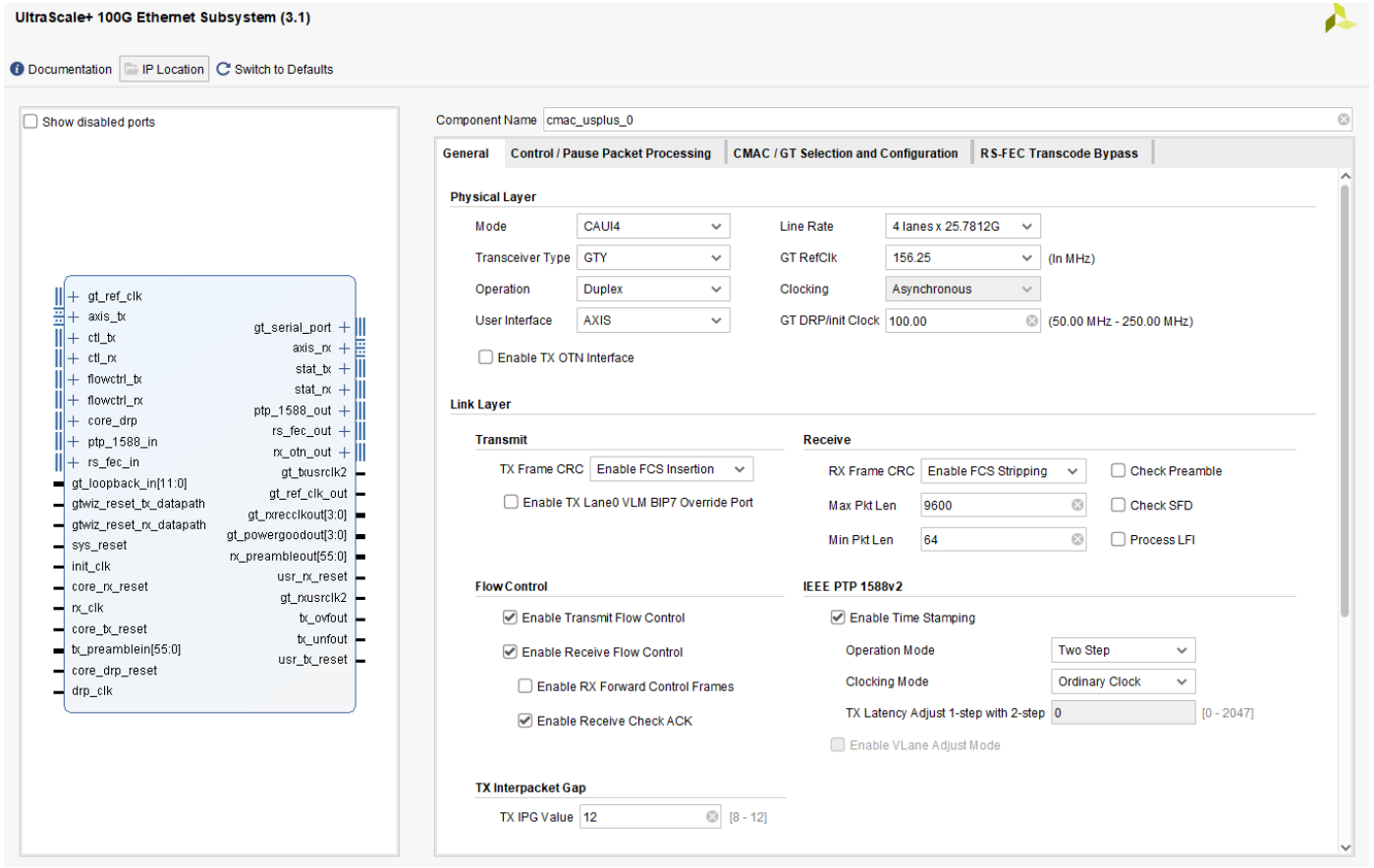
Aurora 64b/66b Interface

- Aurora 64b/66b is a point-to-point protocol developed by Xilinx.
- Uses 64b/66b encoding
- The Xilinx IP wraps the MGTs to provide a simple AXI4-Stream interface for the user.
- Framing mode enables CRC check
- Instrument Design Library for LV2023



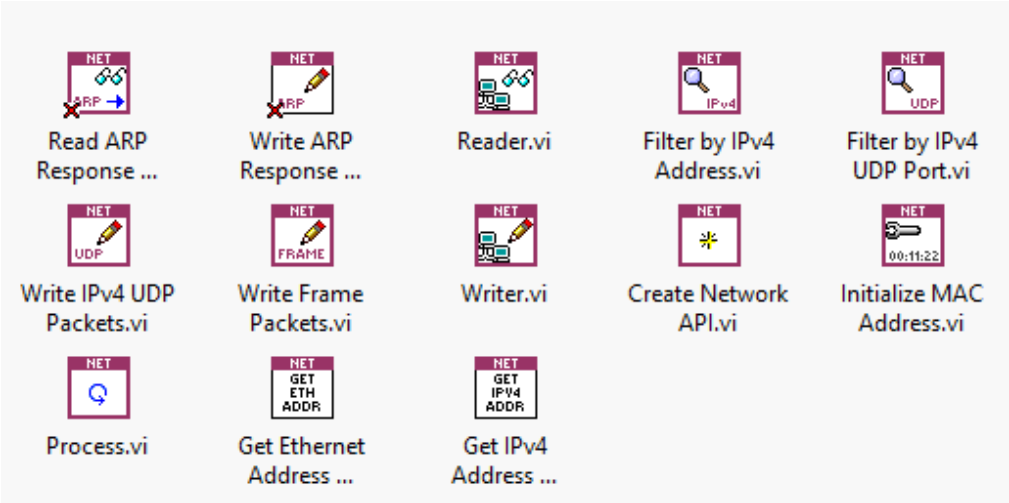
100GigE Interface

- The Xilinx CMAC IP includes the physical (PHY) and data link (MAC) layers.
- Ethernet frames are sent and received over a 512-bit AXI4-Stream interface
- The Xilinx CMAC IP will compute and append the FCS
- Hard IP for RS-FEC

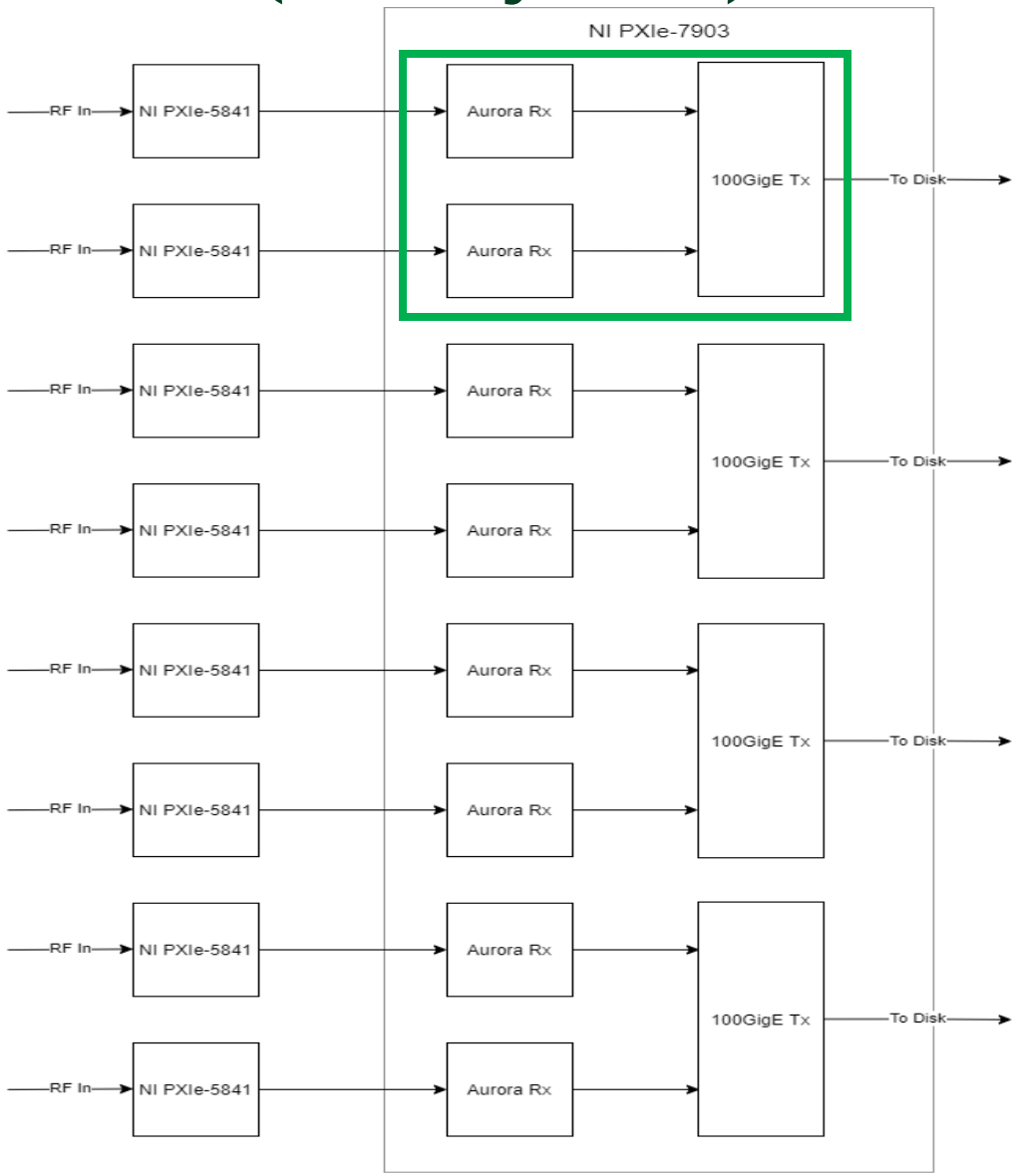


100GigE LabVIEW FPGA Support

- Network IDL expanded to support 100Gigabit Ethernet
- API for Writing UDP datagrams
- Filtering received packets by MAC address, IP address, UDP port
- Installed with FlexRIO Integrated IO

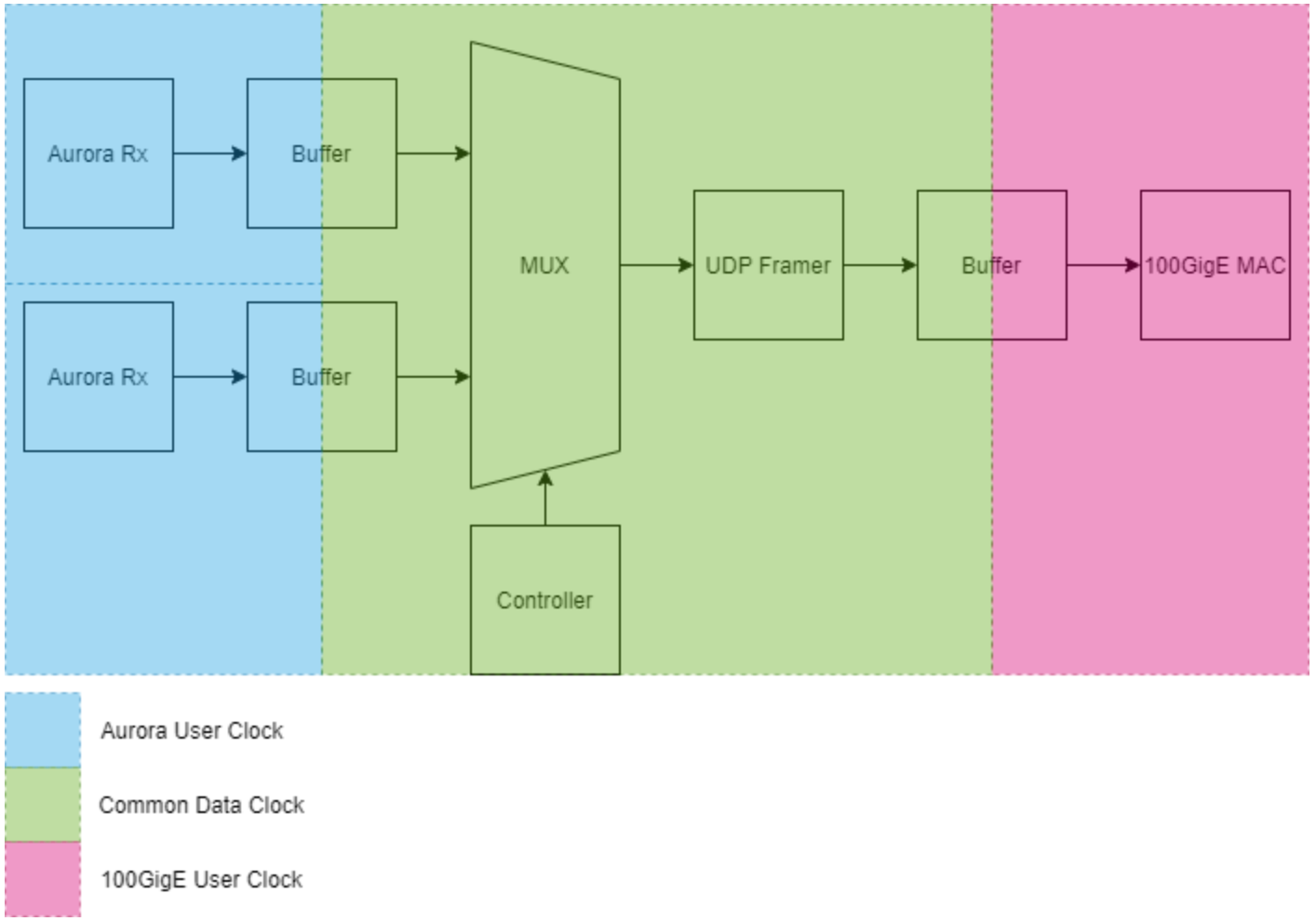


Case Study - Record (& Playback)



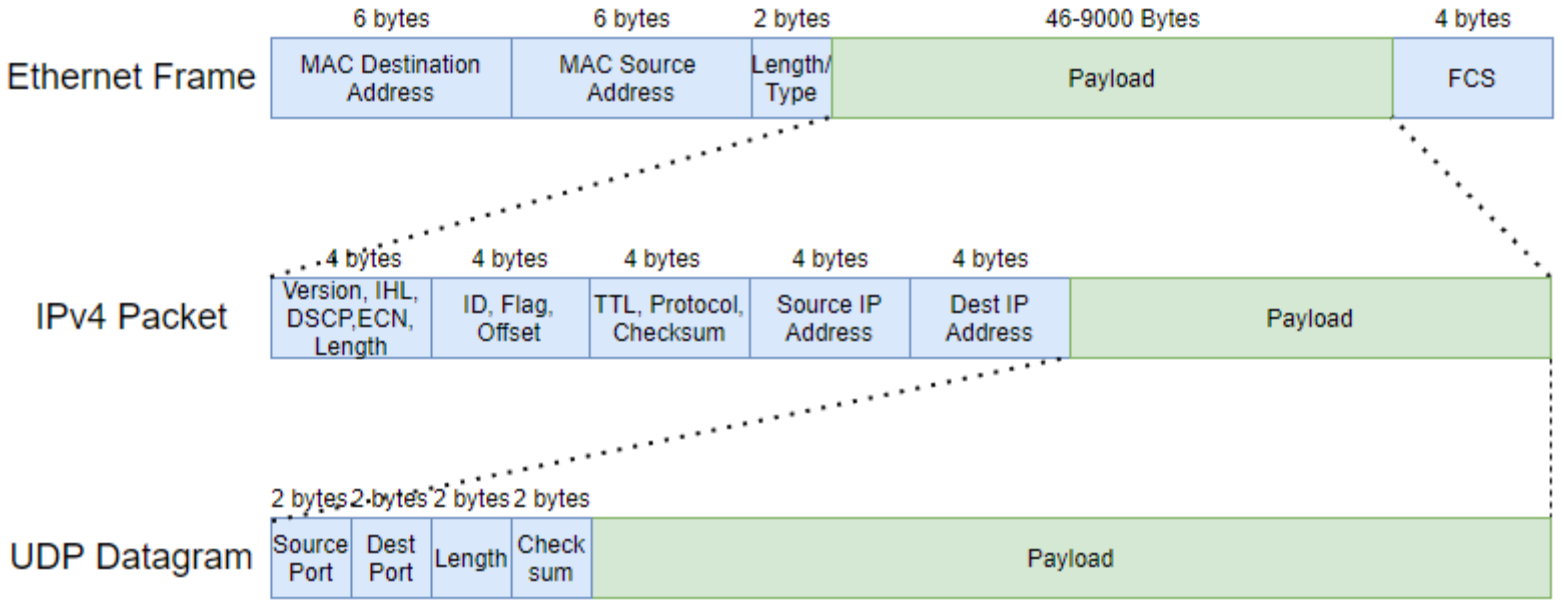
Aurora ->100GigE Subsystem

- The data received from each Aurora interface is on a unique Aurora User Clock
  - Data arrives at about 40gbps
- Data written to the CMACs is on the CMAC User Clock (~322 MHz)
- Minimize processing done at 322 MHz to alleviate timing pressure.



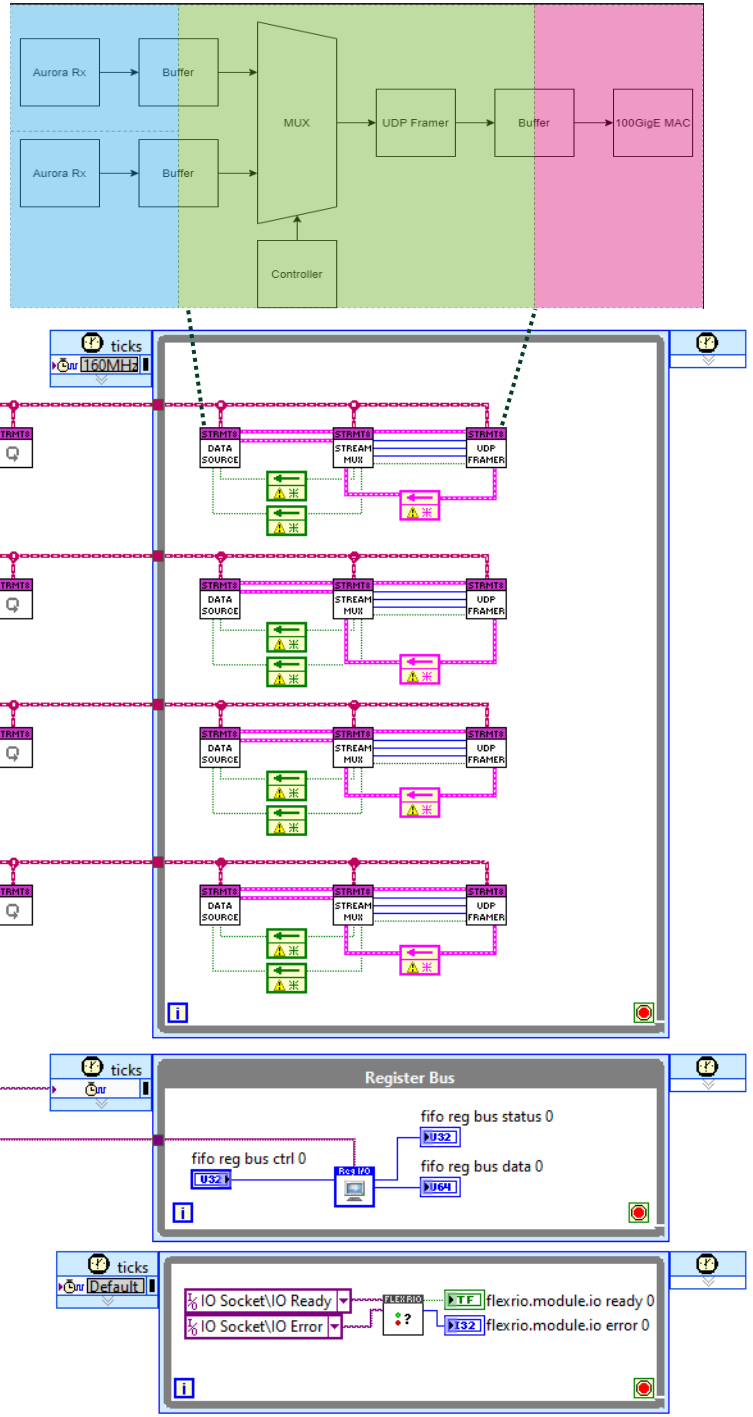
UDP over IPv4

- The parameters for the Ethernet, IPv4, and UDP headers are configured by the host. The MAC and IP addresses are static but the UDP source and destination ports for the UDP header toggle between two values for each packet.



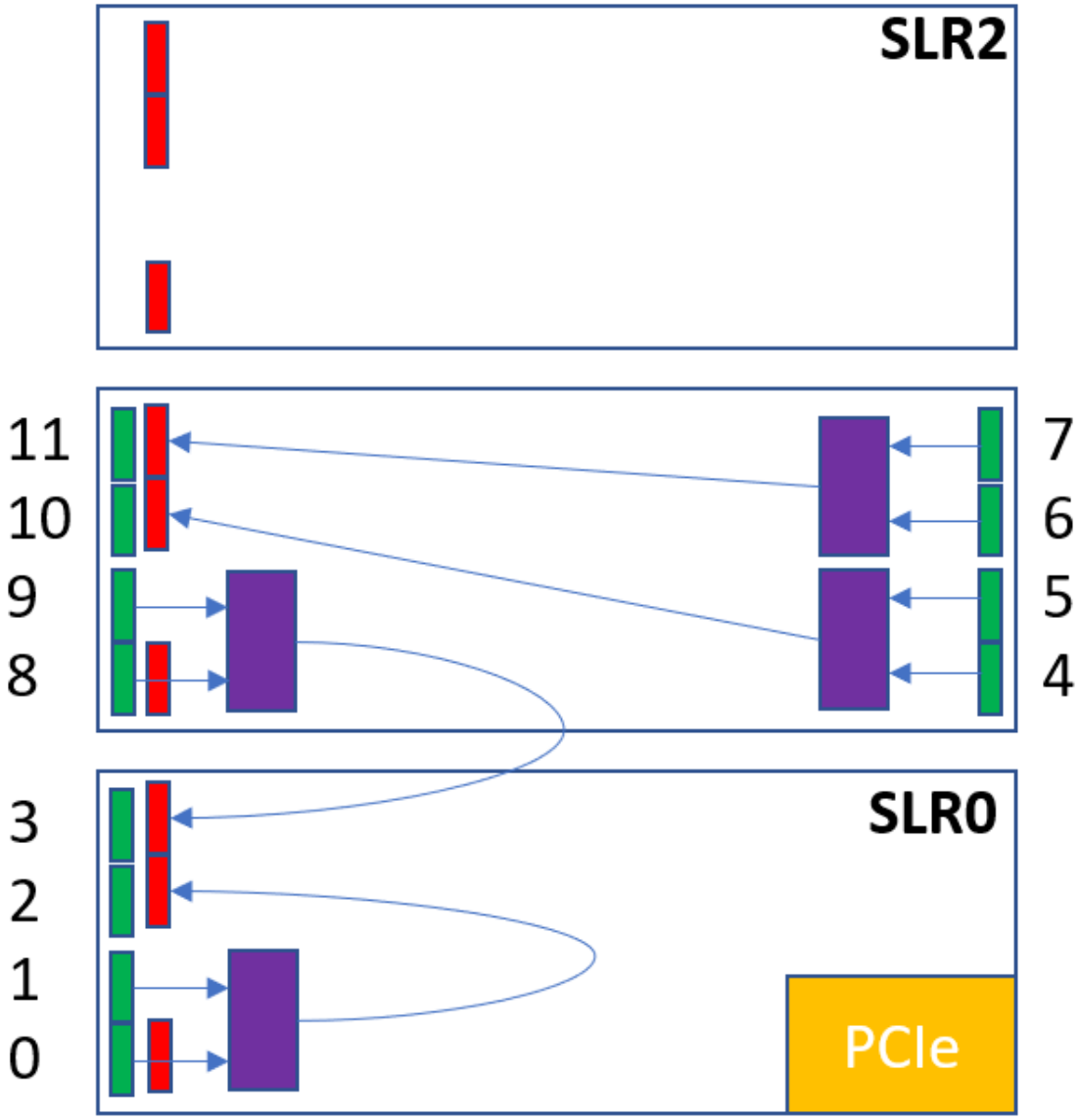
LabVIEW FPGA Implementation

- Modular Design
  - Four instantiations of the subsystem
- Instruction Framework used vs. front panel controls for portability and modularity
- ‘Process’ VI handles all parallel processes
  - Read data in the Aurora User Clock domain
  - Writing data in the 100GigE User Clock domain



Floor Planning - XCVU11P

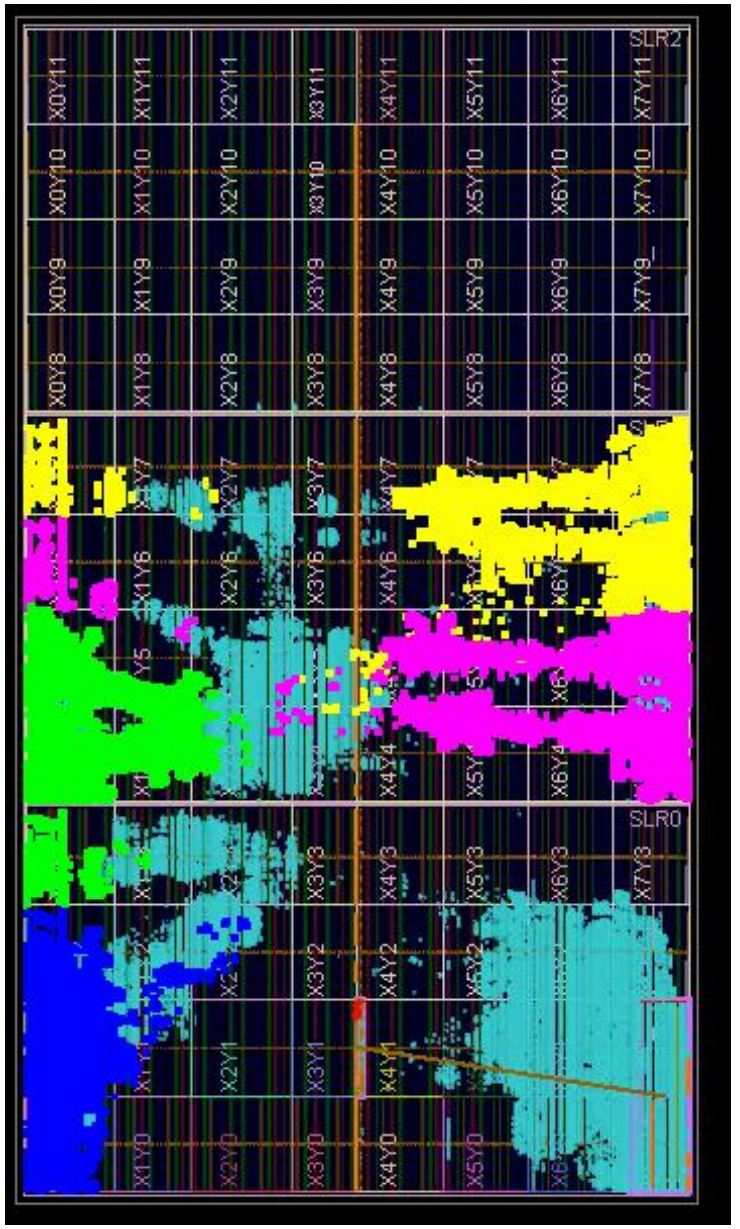
- Choose locations of Aurora Rx ports and CMACs to minimize congestion
- Record & Playback with 5841
  - Combine 2x5841 Aurora x4 links into 1x 100GigE links
  - If SLR1 gets congested, logic can be pushed to SLR2
- Upgrade to 5842 (2 GHz)
  - Same configuration except Aurora x8



Resource Utilization

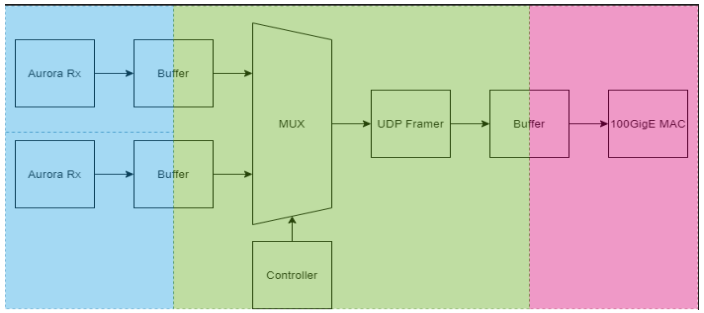
- CLIP IO highlighted
- 100% of DSP slices remaining
- 88% of LUTs and BRAM

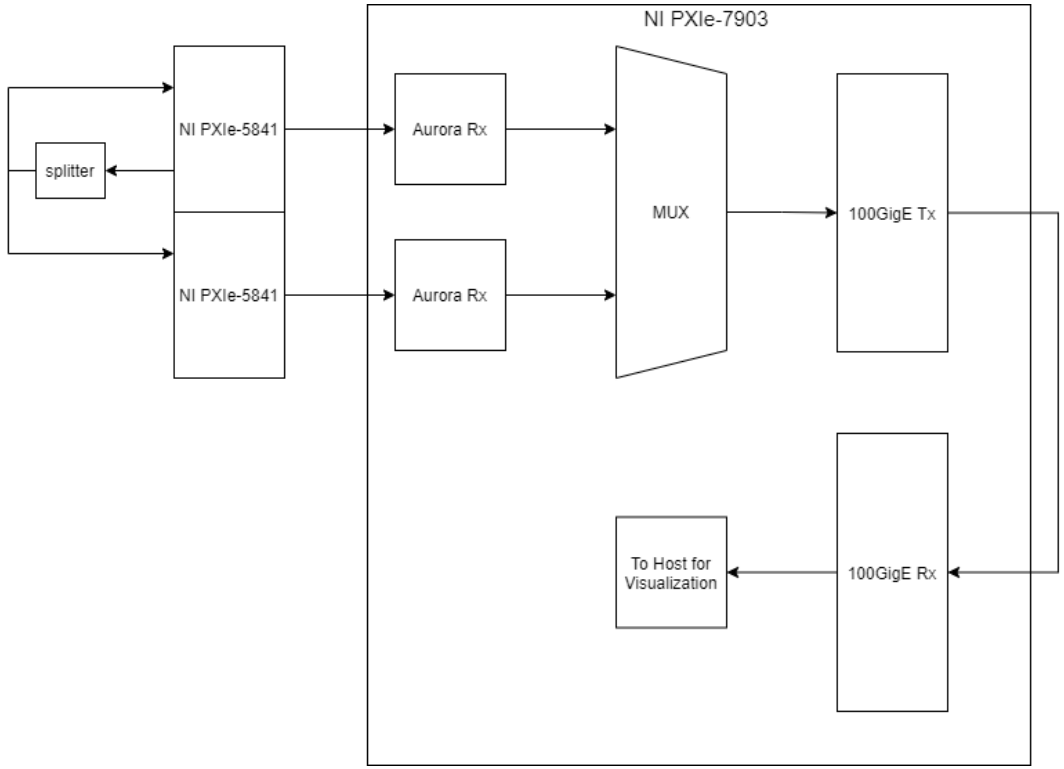
Resource	Utilization	Available	Utilization %
LUT	166528	1295864	12.85
LUTRAM	11773	593216	1.98
FF	234850	2592000	9.06
BRAM	252.50	2016	12.52
IO	430	567	75.84
GT	56	76	73.68
BUFG	58	1008	5.75
MMCM	2	12	16.67



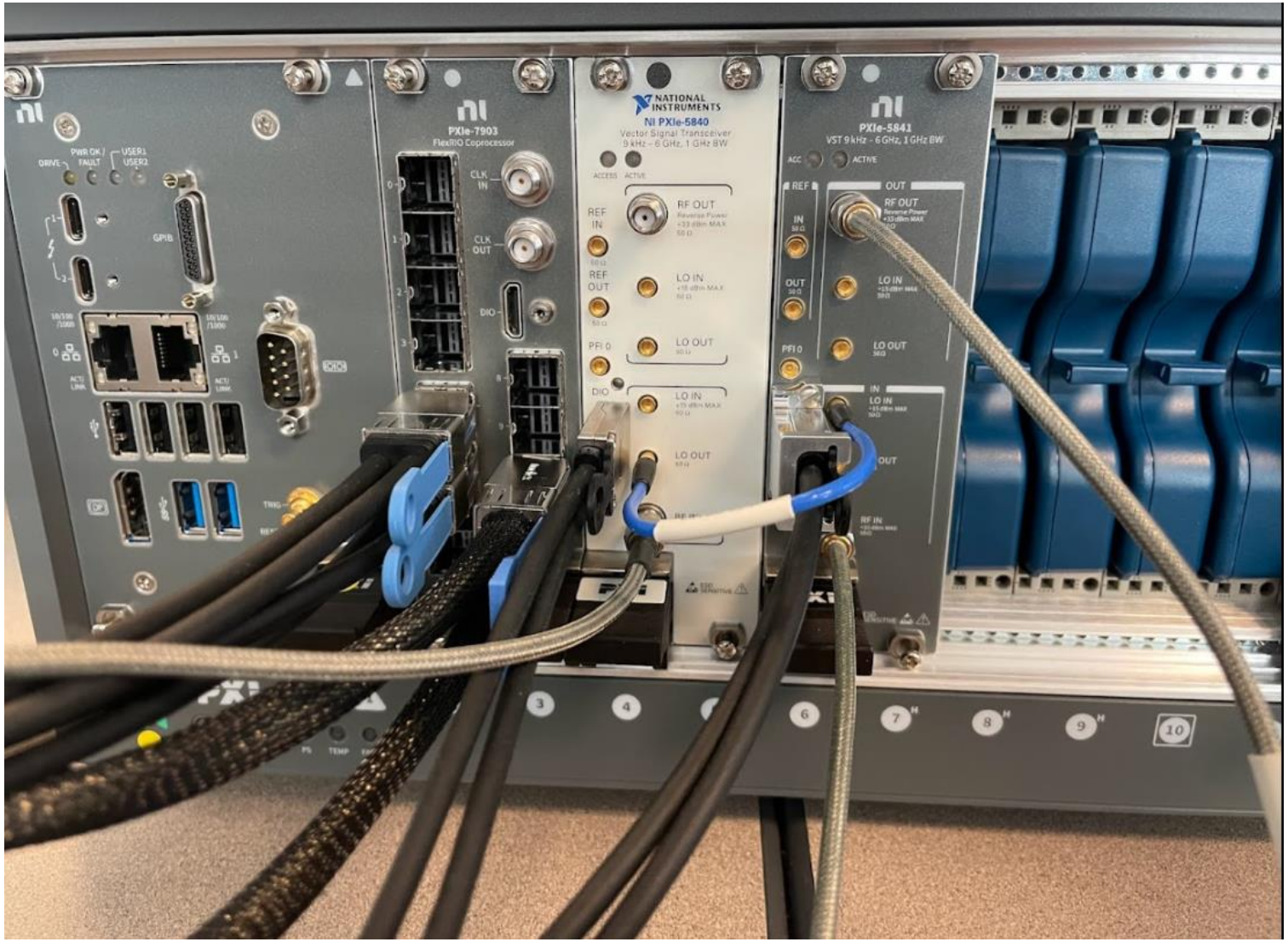
DEMO

- 2x5841s stream synchronized RF data to a NI PXIe-7903.
- IQ data is muxed into UDP packets with unique source/destination UDP ports
- 100GigE UDP is received on another PXIe-7903 100GigE port and demuxed based on the parsed UDP packet destination port.
- Snapshots of the data are taken and sent to the host for visualization





Demo


PXIe-7903
FlexRIO Coprocessor
NATIONAL INSTRUMENTS
NI PXIe-5840
Vector Signal Transceiver
9 kHz – 6 GHz, 1 GHz BW
PXIe-5841
VST 9 kHz – 6 GHz, 1 GHz BW
RF OUT
LO IN
LO OUT
REF IN
REF OUT
CLK IN
CLK OUT
DIO
GPIB
PFI 0

Summary

PXIe-7903

Features

- 12 MiniSAS zHD Connectors
- 28.2 Gbps Line Rate
- External Reference Clock Input/Output
- Xilinx Virtex UltraScale+ FPGA
- 20 GB of DRAM (10 GB per bank) w/ up to 25 GB/s (theoretical) write speed
- 8-port DIO terminal (mini-HDMI)
- PCI Express Gen 3x8

Release

- June 2023
- Delivery in Q3

Questions?

Image source: https://matrixestimating.com.au/faq/