

**W**  **L** 20 42758  **ME**  **AUST**  **N**



CONNECT



**CONNECTION**

**2023 AUSTIN**



# 5 Best Practices for Maximizing DC Measurement Performance

Shane Arthur



# Agenda

- Background and Intro
- DC Instrumentation and Measurement Fundamentals
- Best Practices

Calibration

Voltage Offsets

Voltage Drop

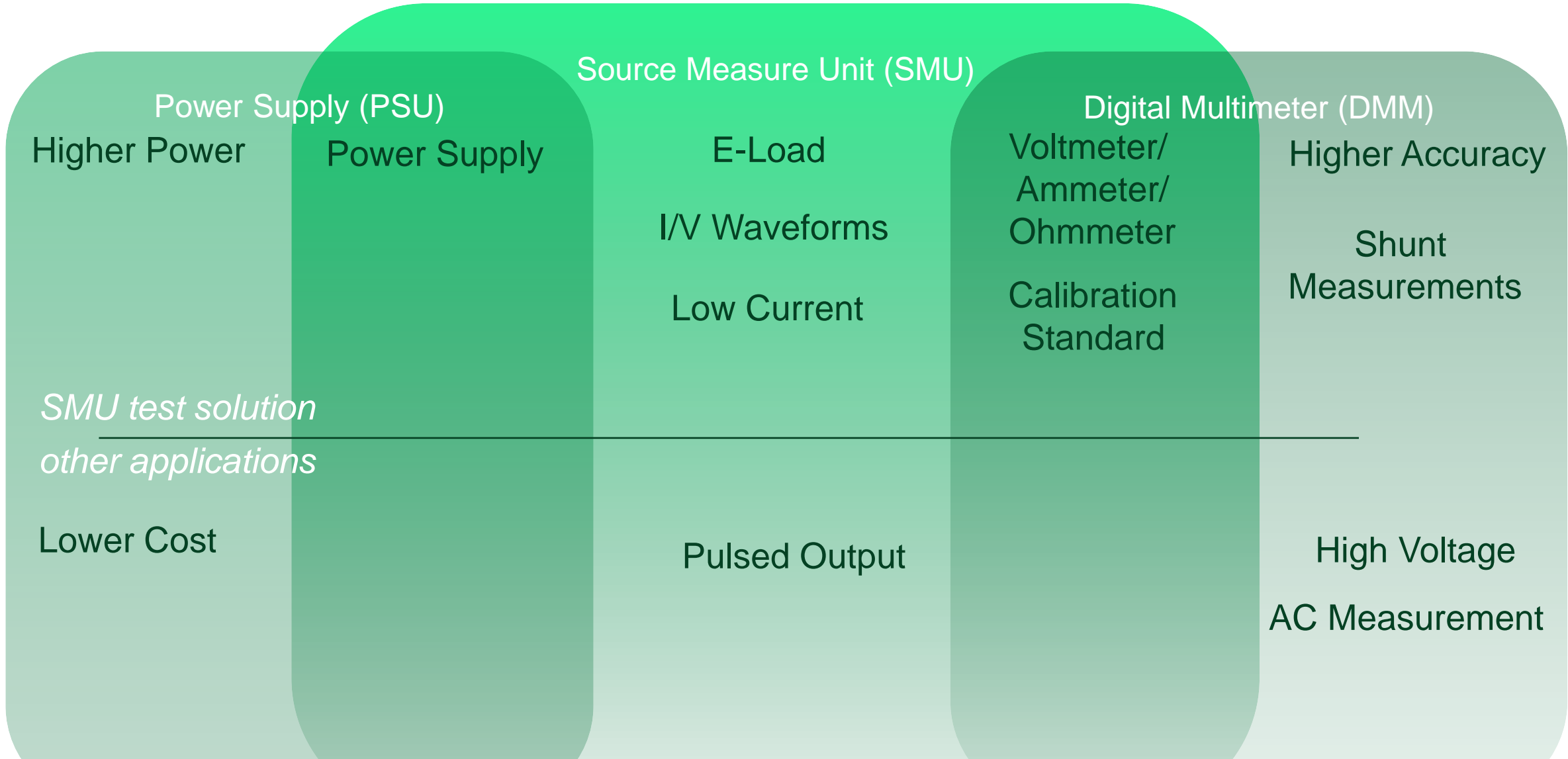
External Noise

Leakage Current

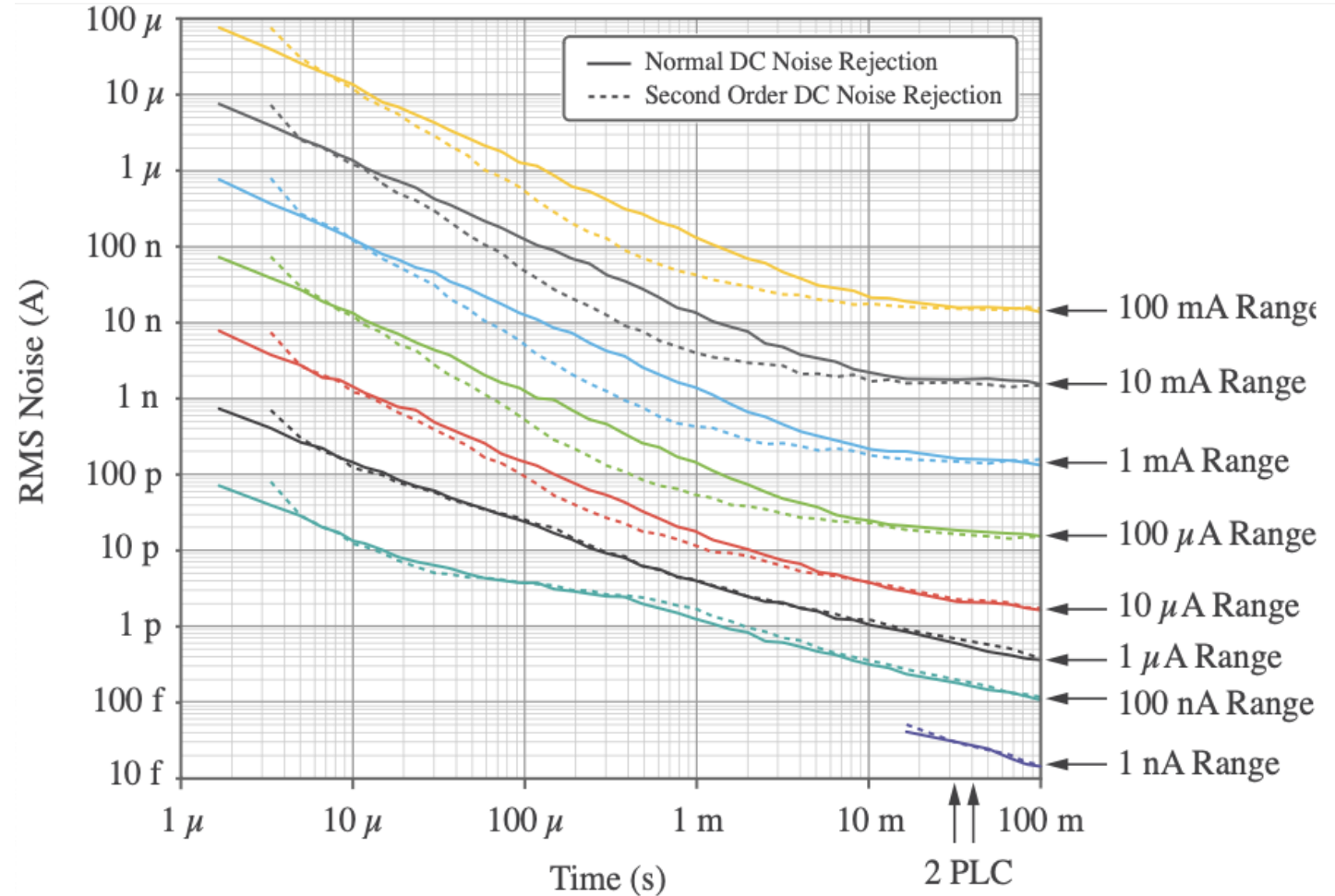
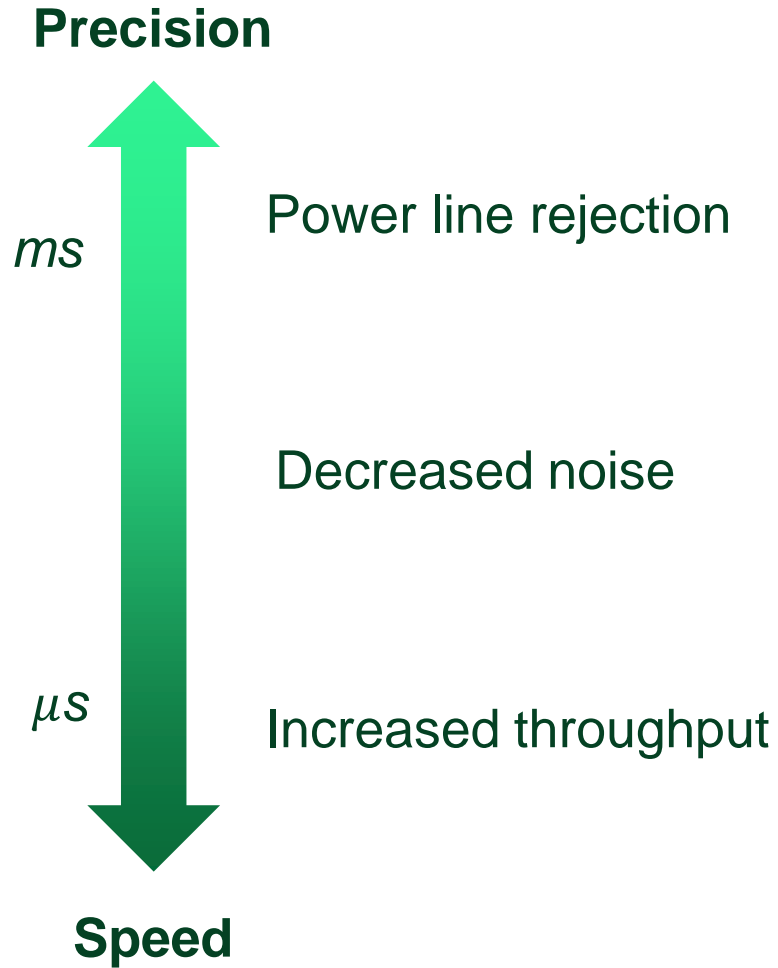
System-Level  
Error Sources



# DC Instrument Applications



# Optimizing Precision vs Speed



# Best Practice 1: Understand the Importance of Calibration







Understand the Importance of Calibration

# Calibration Types and Use Cases

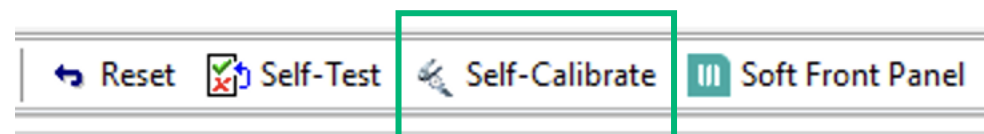
Two types of calibration work together to ensure devices meet specifications:

**External Calibration** (typically annually)

**Self-Calibration** (typically daily)



**Traceable Calibration Certificate**





# Externally Calibrate for Absolute Accuracy

Regularly calibrating instruments will ensure that they operate within published specifications

- Adjustment corrects for time drift of onboard references
- Specifications can only be guaranteed for specific time intervals
- Performance verified against traceable standards – back to fundamental units as defined by the International System of Units (SI)

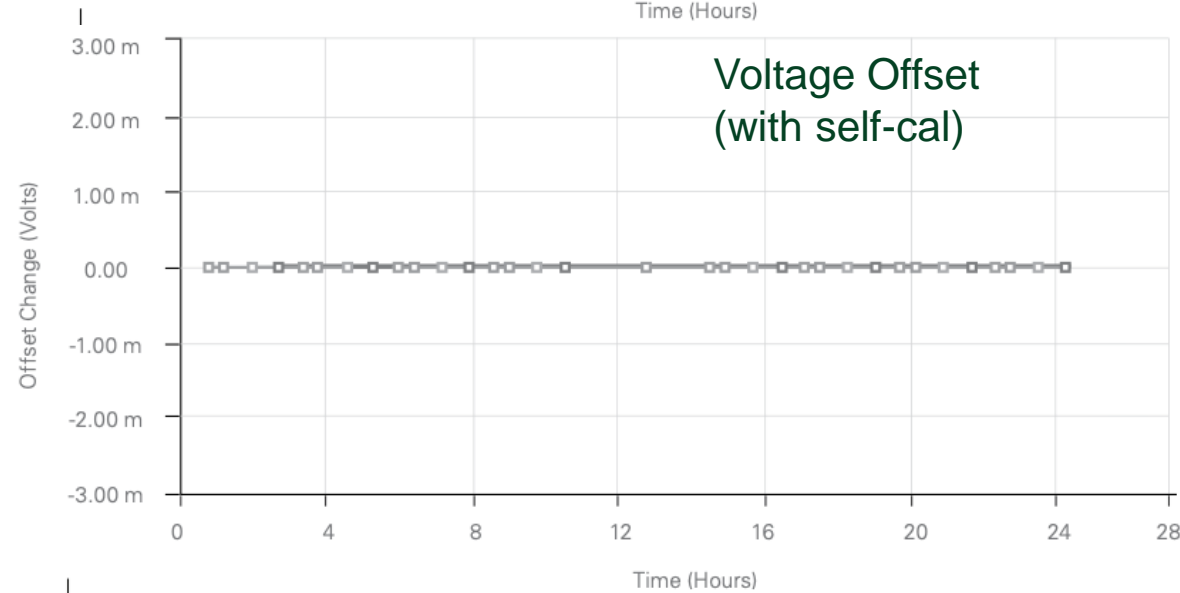
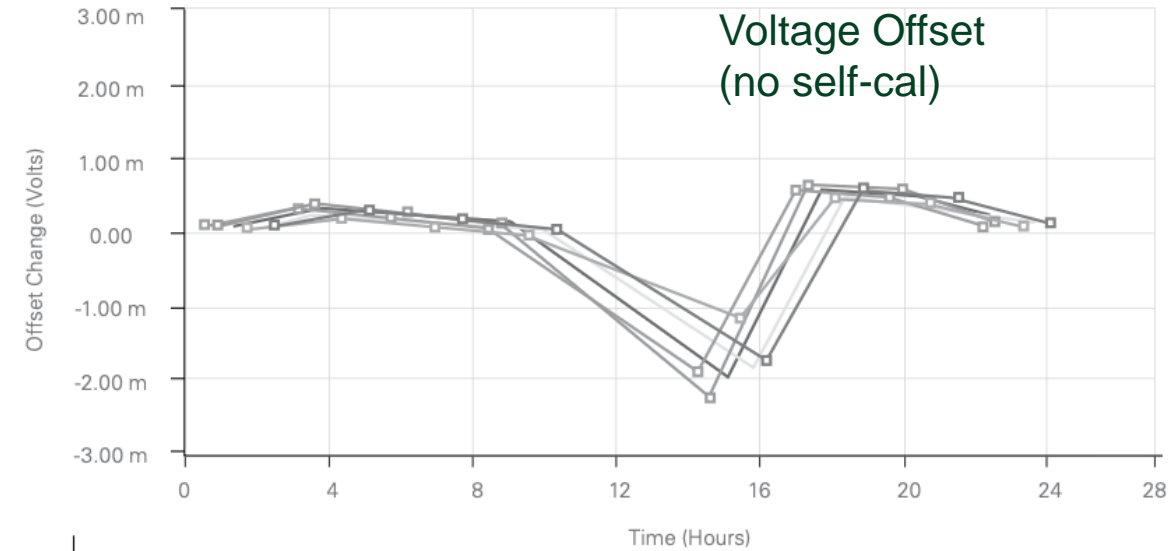
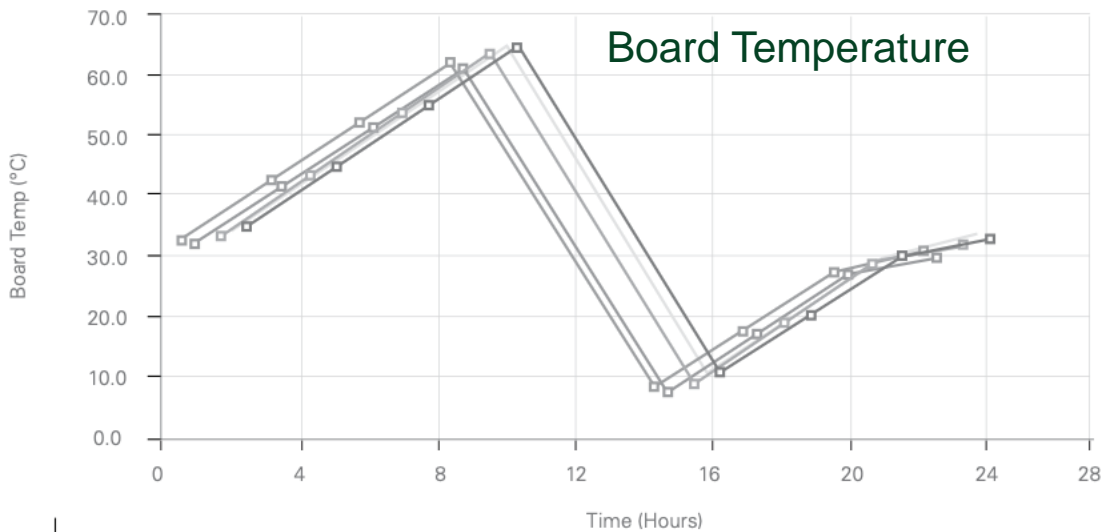
**Table 1.** DC Voltage  $\pm$  (ppm of reading + ppm of range)

Range	Input Resistance <sup>[1]</sup>	24 Hr <sup>[2]</sup> T <sub>selfcal</sub> $\pm 1^\circ\text{C}$	90 Day T <sub>selfcal</sub> $\pm 5^\circ\text{C}$	2 Year T <sub>selfcal</sub> $\pm 5^\circ\text{C}$
100 mV	10 M $\Omega$ $\pm$ 2%, >10 G $\Omega$	6 + 5	27 + 7	28 + 8
1 V		4.5 + 0.8	15 + 2.5	18 + 2.5
10 V		2 + 0.5	10.5 + 0.5	12 + 0.5



# Reduce Temperature Sensitivity with Self-Cal

Results show the effect of large temperature swings on device offset performance



# Best Practice 2: Minimize and Compensate for Voltage Offsets

# Sources of Offset Voltages

Unintentional thermocouples can introduce offsets due to

- Variations in temperature across a cable or mated connector pair
- Self-heating in current shunts or other high-power dissipation equipment
- Self-heating in relays due to coil power dissipation

Component	“Budgetary” Offset
Connector	1uV
Electromechanical Relay (non-latching)	20uV
Electromechanical Relay (latching)	2uV
Reed Relay (single pole)	50uV



# Experimental Connector Offset Setup

Tested offset voltage vs temperature gradient:

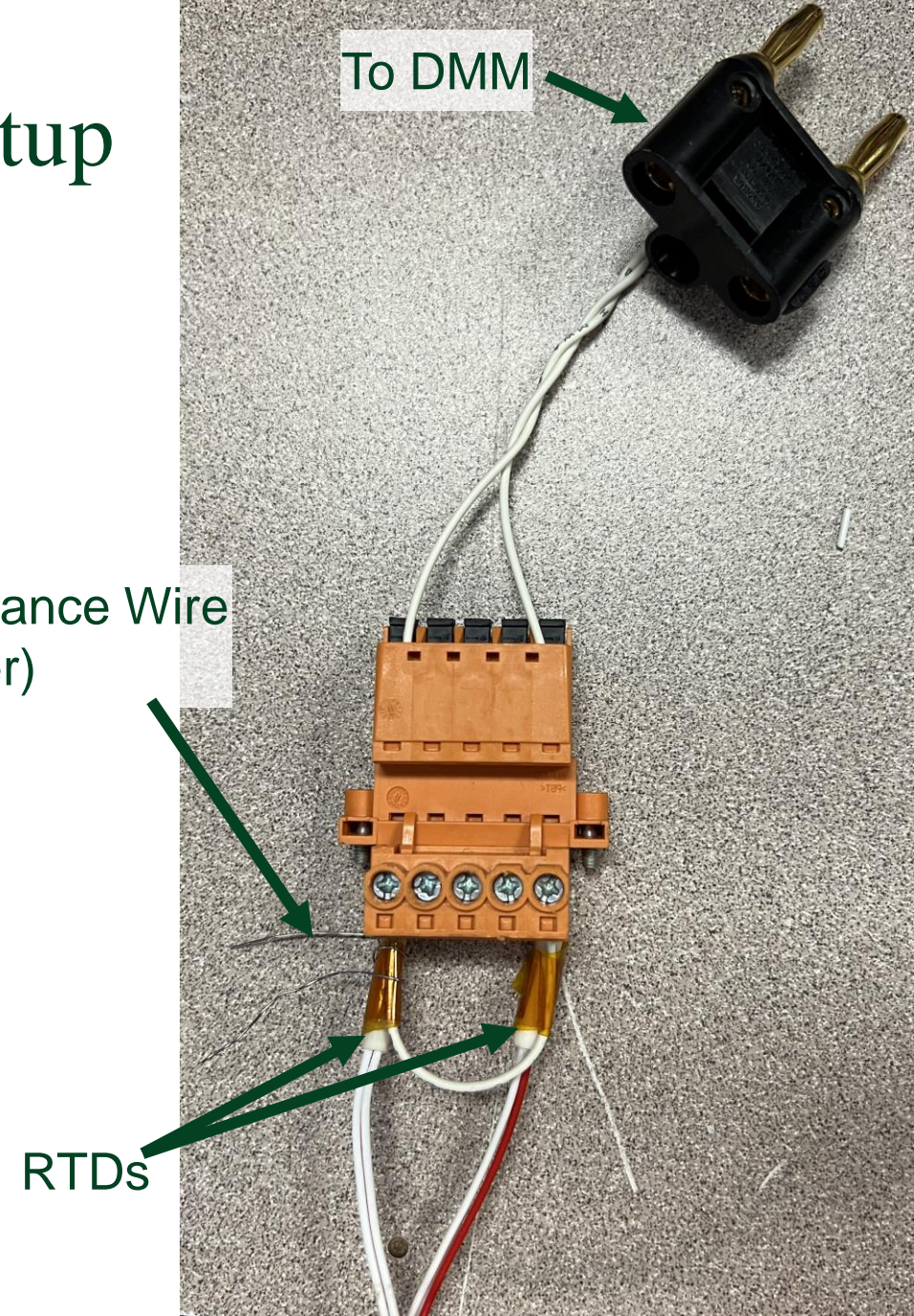
- Heated one side of a jumper wire
- Measured voltage of the short with DMM
- Measured temperature on both sides of the jumper



Resistance Wire  
(heater)

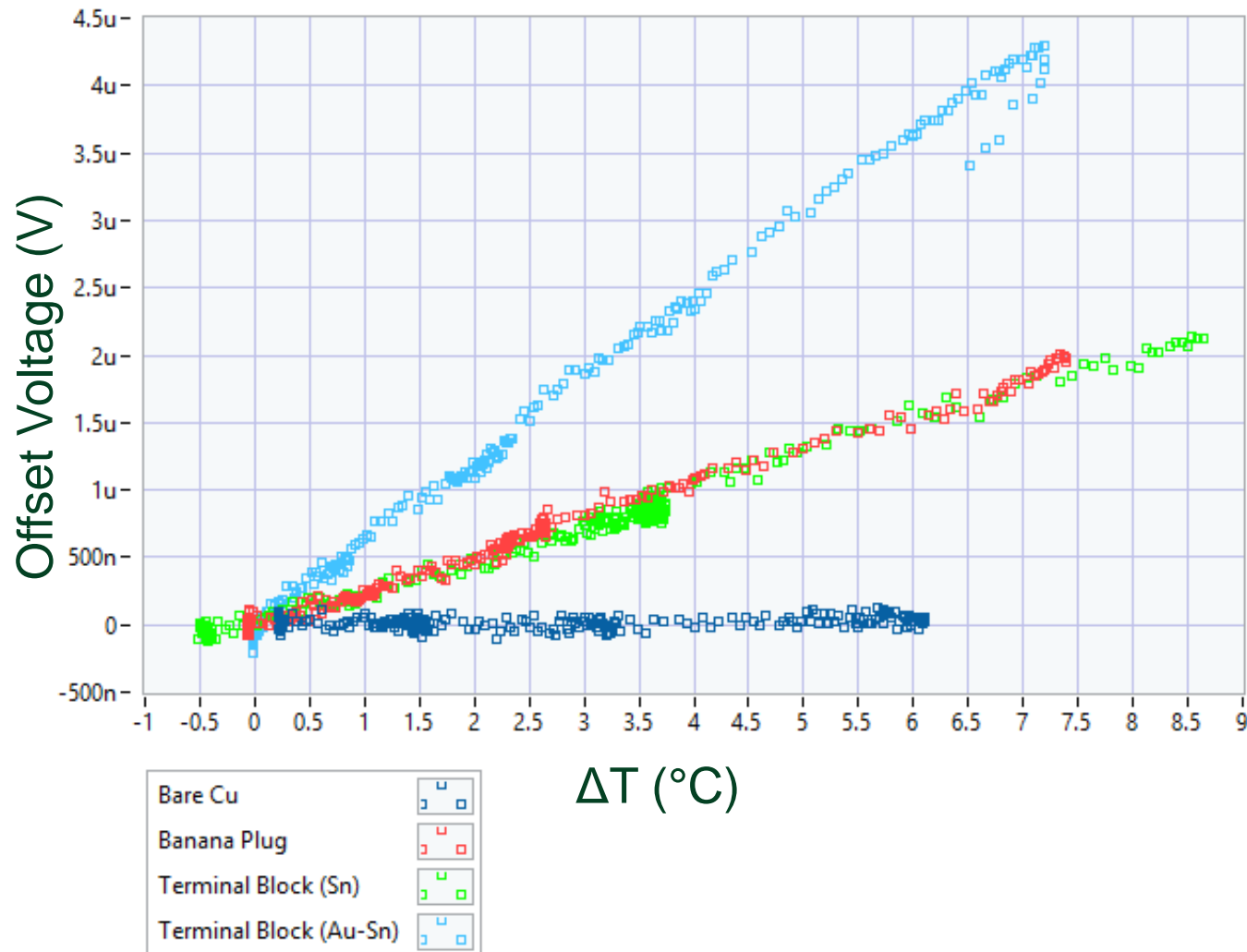
RTDs

To DMM





# Experimental Connector Offset Results



Copper connector showed nearly no temperature dependency

- Wire conductor is also copper

Banana plug and tin terminal block very similar

- Both are primarily brass + plating

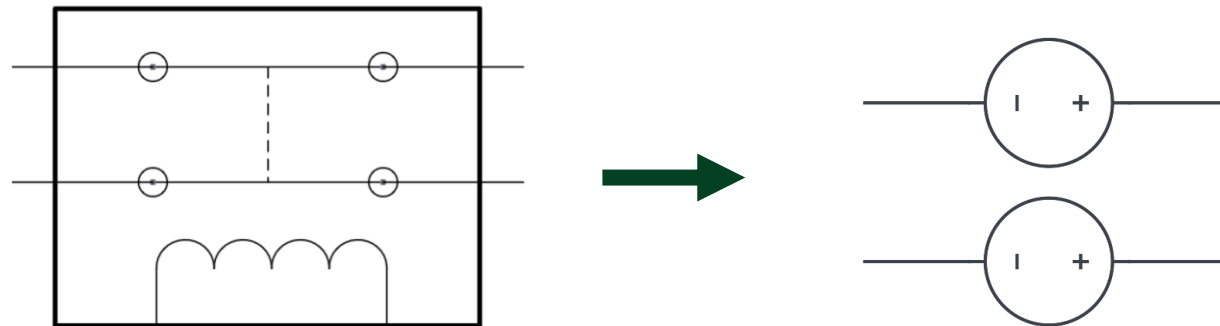
Gold-tin intermated pair much worse

- 600nV/ $^{\circ}\text{C}$  is still relatively small

# Balance Offsets for Differential Measurements

Symmetric offsets in a differential pair will cancel out

- Evaluate the specified offset voltage (thermal EMF) of switching in the measurement path (hint: look for a spec with  $\mu V$  units)
- Include the same number/type/orientation of relays and connections on each lead
- Model the measurement by replacing closed relays with voltage sources







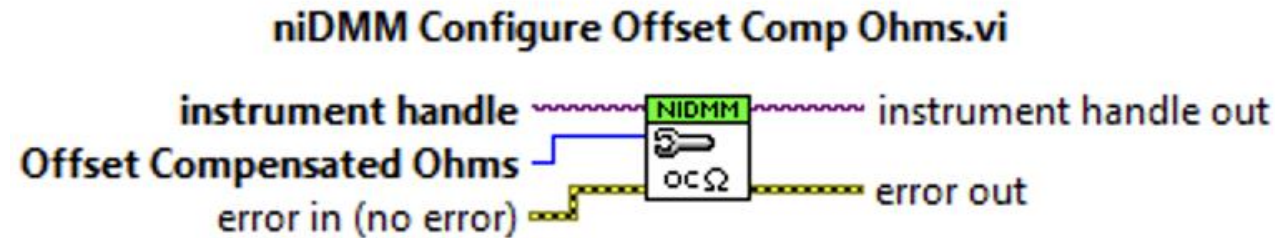
# Compensating for Voltage Offsets

Offsets that can't be physically removed can often be compensated for

A compensated measurement can be calculated from multiple measurements that include the offset

For DMM resistance measurements, compensation can be performed automatically

For SMU measurements, offset compensation can be performed in application code



# Compensating for Voltage Offsets

To determine the compensated measurement with an SMU, perform two measurements:

$V_{M1}$  is the measured voltage with the source turned on

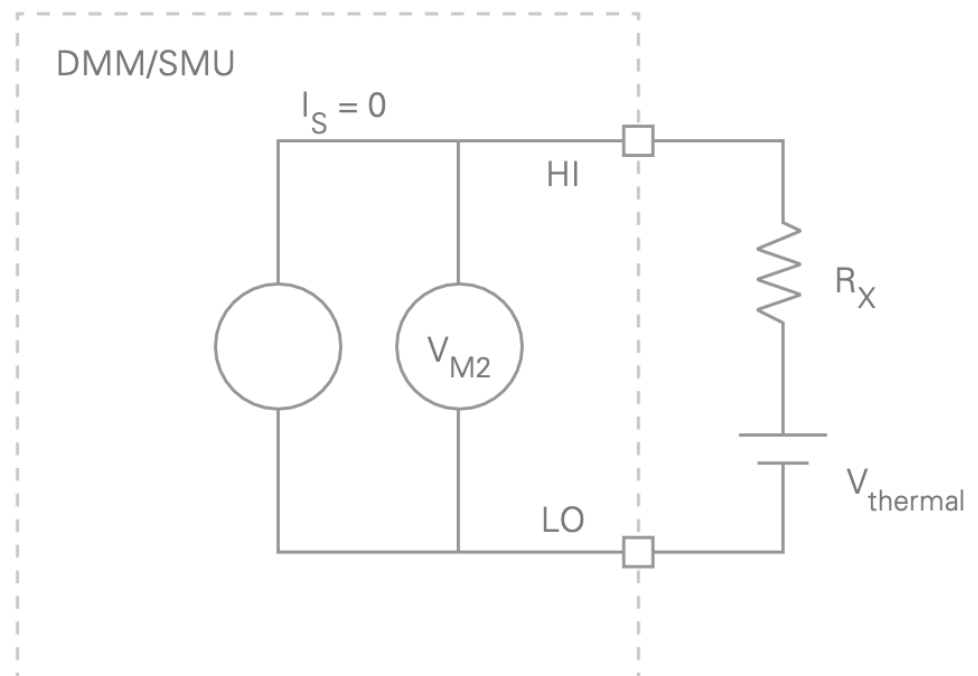
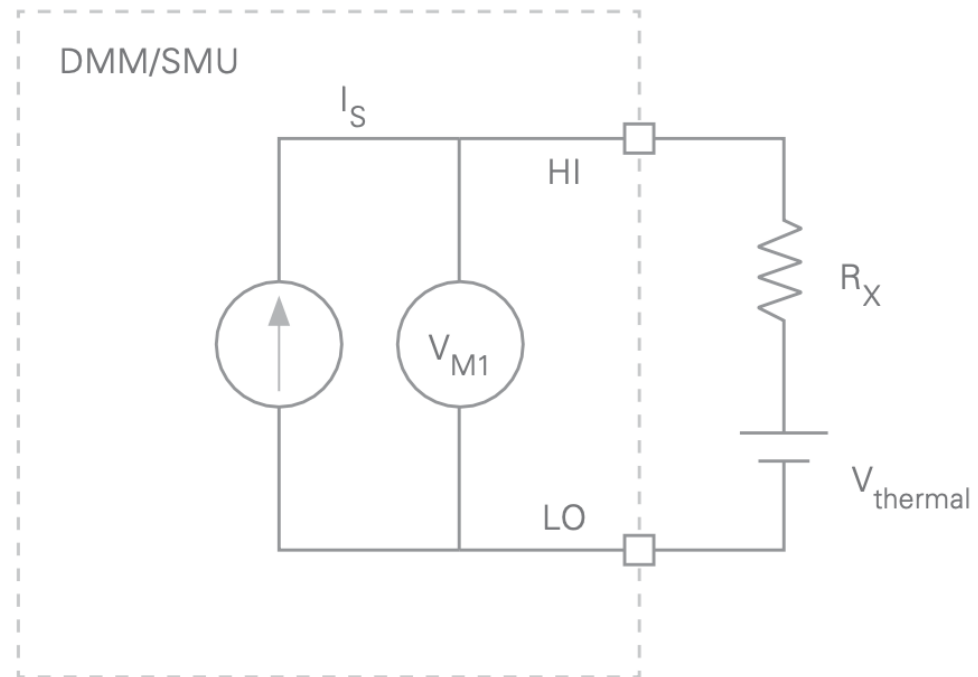
$$V_{M1} = I_S R_X + V_{\text{thermal}}$$

$V_{M2}$  is the measured voltage with the source turned off

$$V_{M2} = I_{\text{Soff}} R_X + V_{\text{thermal}} = V_{\text{thermal}}$$

The offset compensated voltage  $V_{OC}$  is then

$$V_{OC} = V_{M1} - V_{M2} = (I_S R_X + V_{\text{thermal}}) - V_{\text{thermal}} = I_S R_X$$



# Best Practice 3: Offset the Effects of Lead Resistance

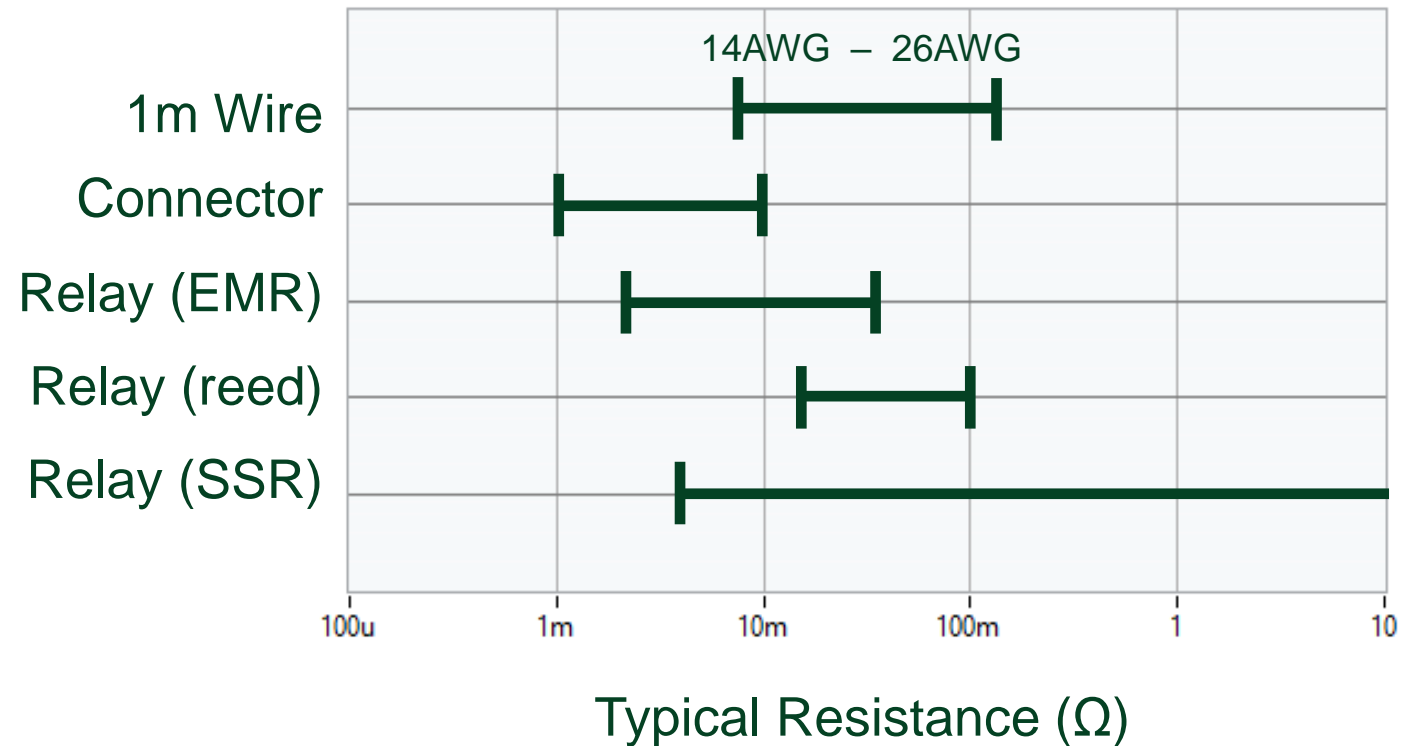




# Lead Resistance Impact on Measurements

Lead resistance introduces several potential issues:

- Voltage delivered to the DUT is lower than expected
- Resistance measurements will include error

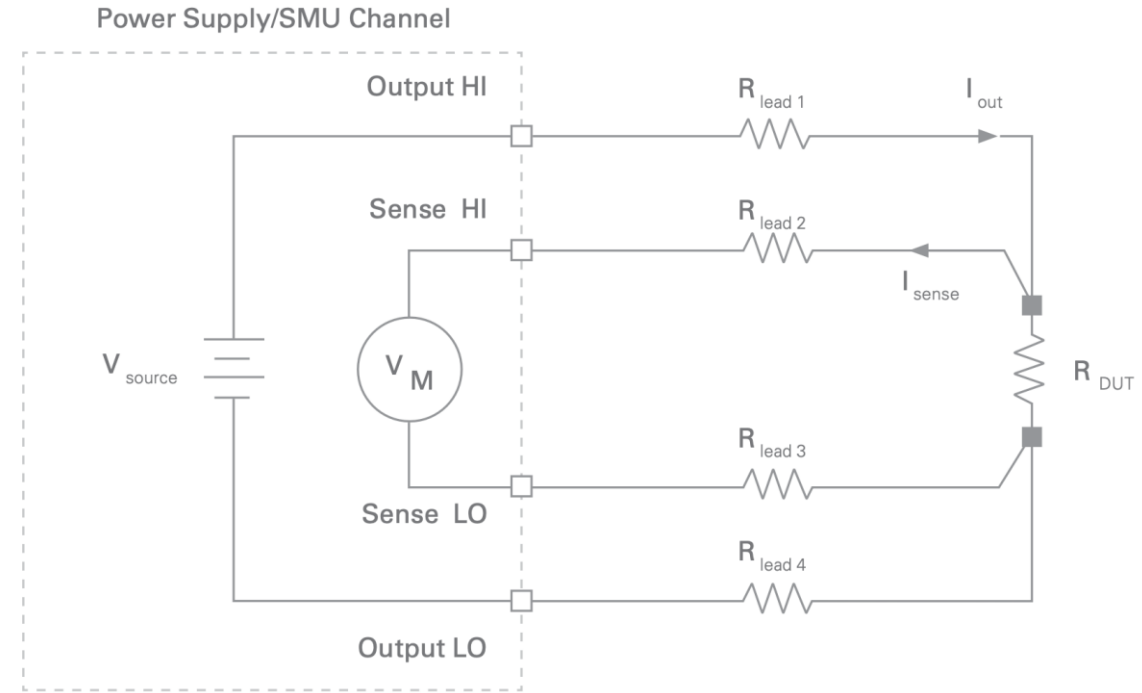


# Offset Effects with Remote Sense

Remote sense uses two pairs:

- Force/output: Supplies current
- Sense: Measures voltage

DMM 4-Wire resistance measurements operate the same way



## Local Sense

SMU controls the voltage between the output pins

$$V_{\text{source}} = V_{\text{HI}} - V_{\text{LO}}$$

The voltage at the DUT is determined by the voltage divider formed by  $R_{\text{DUT}}$  and the HI/LO lead resistances due to current flow

## Remote Sense

SMU controls the voltage between the sense lines

$$V_{\text{source}} = V_{\text{Sense HI}} - V_{\text{Sense LO}}$$

With sense lines connected at the DUT, the voltage setpoint is maintained at the DUT regardless of lead drop voltages



# Remote Sense Example

$$R_{DUT} = 10\Omega$$

$$R_{lead1} = R_{lead4} = 1\Omega \text{ (output/force)}$$

$$R_{lead2} = R_{lead3} = 10\Omega \text{ (sense)}$$

$$V_{source} = 1V$$

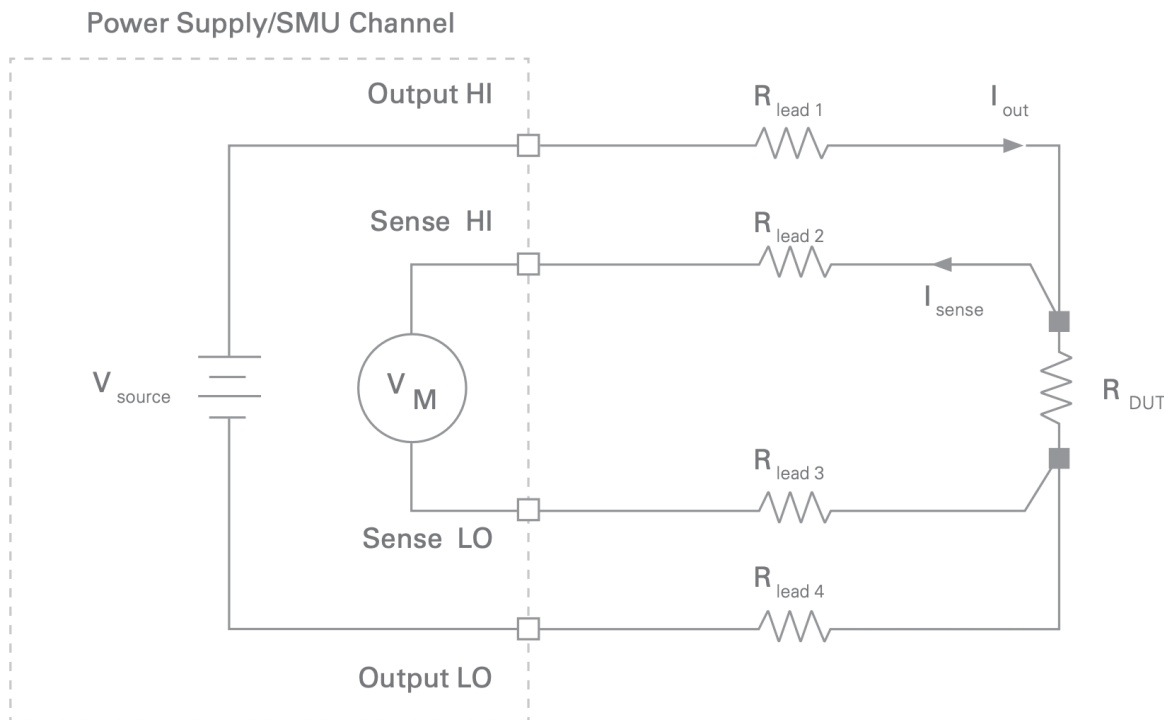
$$R_{force} = R_{DUT} + R_{lead1} + R_{lead4} = 12\Omega$$

## Local Sense

$$V_{DUT} = V_{Source} * \frac{R_{DUT}}{R_{Force}} = \mathbf{0.833V}$$

## Remote Sense

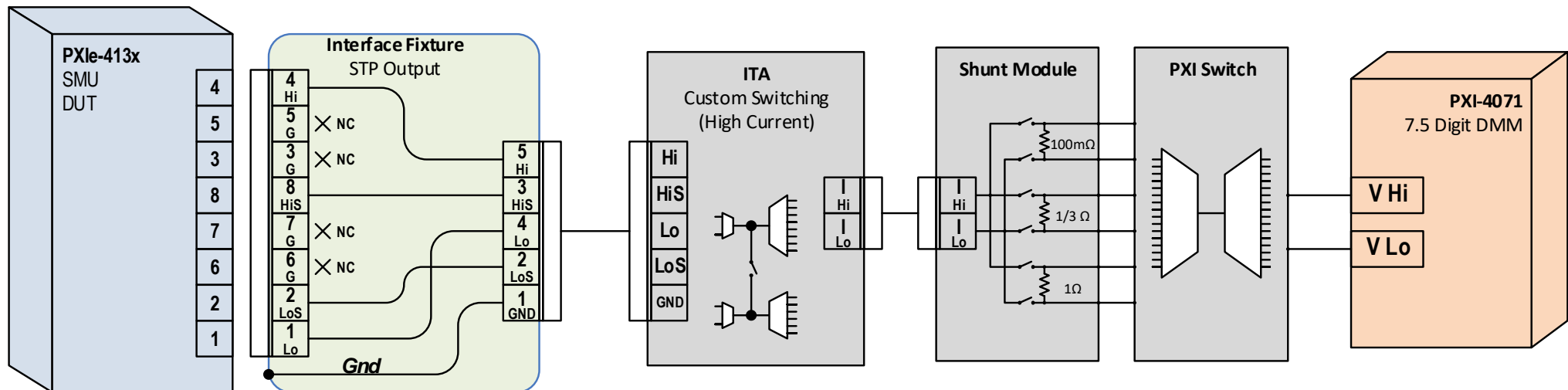
$$V_{DUT} = V_{Source} = \mathbf{1V}$$



# Practical Example of Lead Resistances

## NI Manufacturing SMU Current Verification with Low-Value Shunt

- When the 100mΩ current shunt is enabled, the DUT measures ~900mΩ
- The DMM, in 2W resistance mode, measures ~300mΩ (200mΩ lead + relay resistance)
- For current verification, the DUT voltage measurement is unimportant
- DMM input is high impedance and functions like sense lines, so the 200mΩ resistance does not affect the measurement

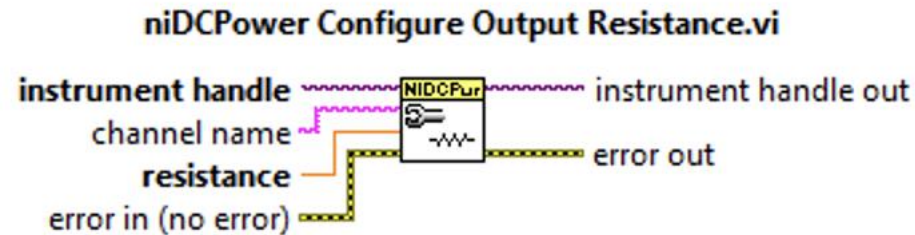




# Alternative Compensation for Lead Resistance

For applications where it is not possible to connect sense lines directly at the DUT, there are other options

- Remote sense can be used to correct for part of the measurement path
- Programmable output resistance
  - Measure path resistance using the SMU by shorting the output at the DUT,  $R_{\text{path}}$
  - Set output resistance to  $-R_{\text{path}}$

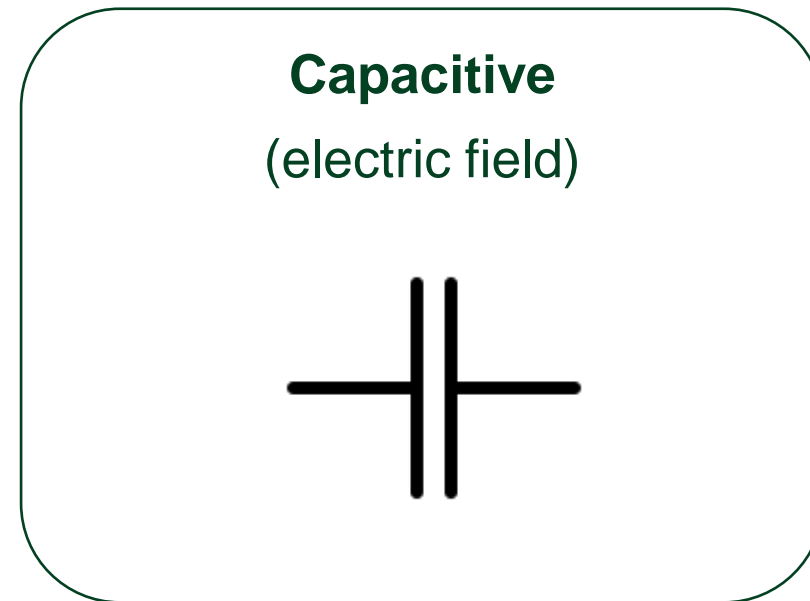
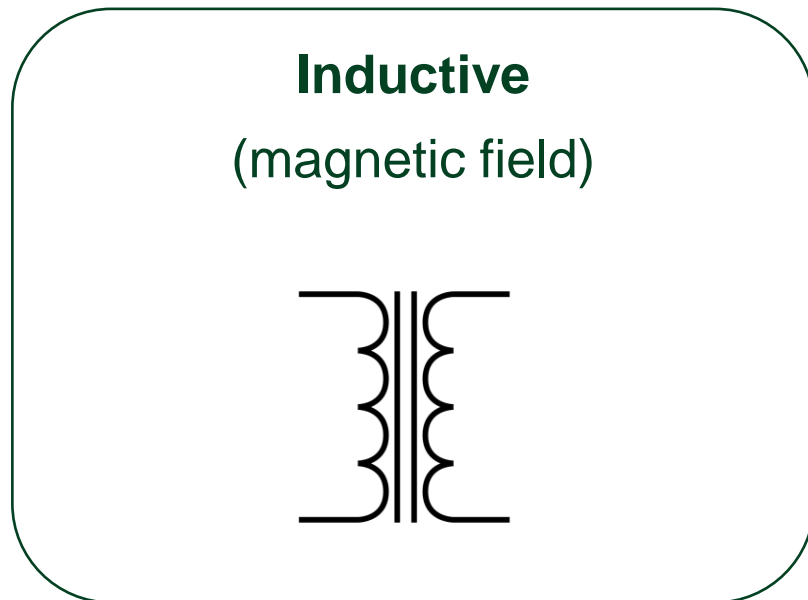




# Best Practice 4: Minimize External Noise



# External Noise Sources and Coupling



# Minimizing Inductively Coupled Noise

Inductively coupled noise often comes from

- Nearby cabling (or shields)
- Leakage flux from transformers, inductors, or motors

Reduce the loop area to minimize noise pickup:

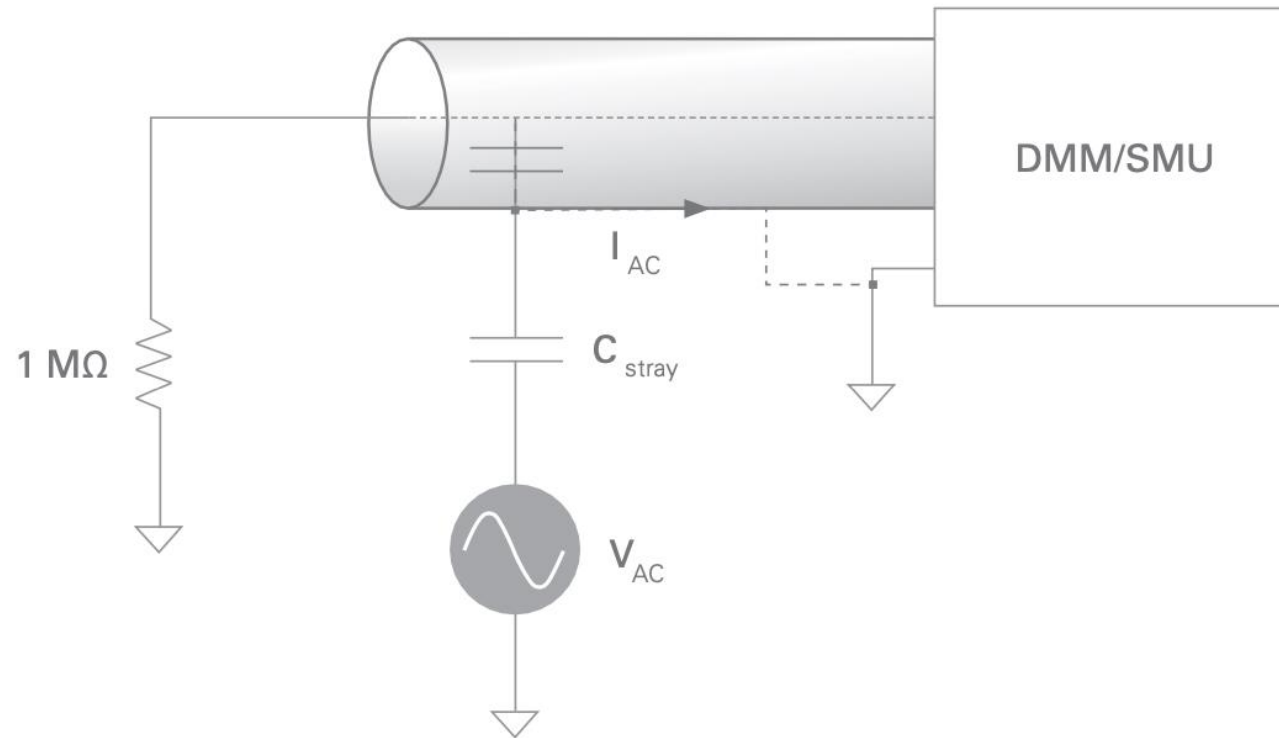
- Keep the conductors close together
- Twist the pair together





# Shielding for Capacitive Coupling

Shielding is a critical consideration for high-impedance measurements





# Implementing Effective Shielding

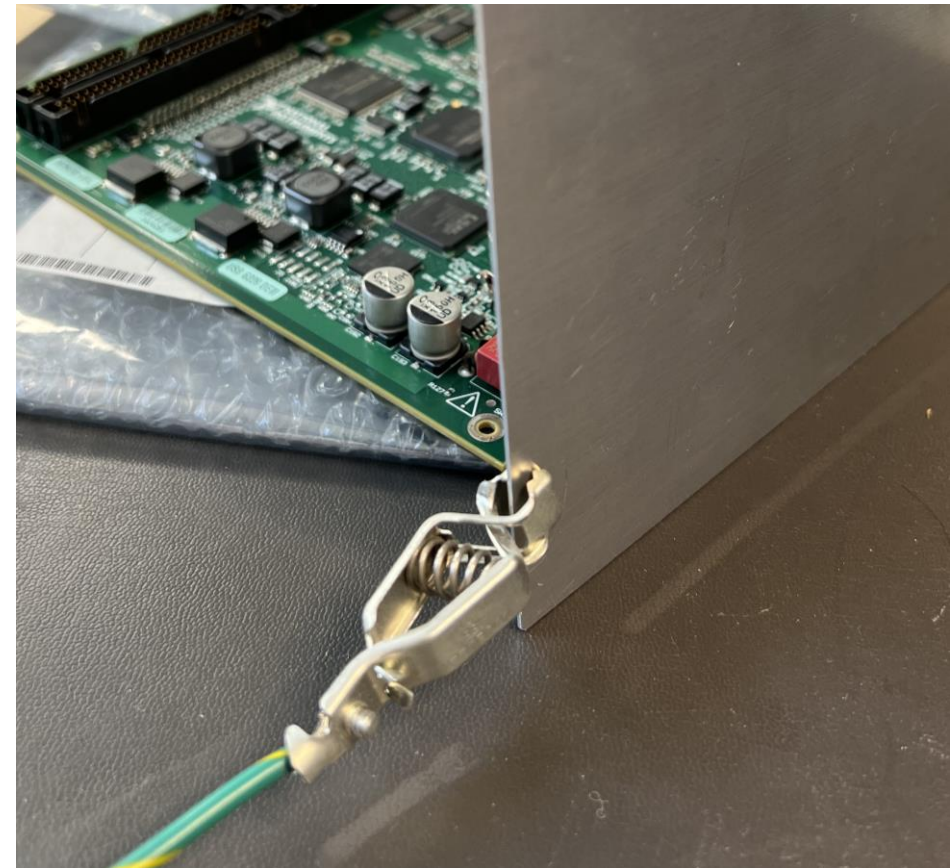
## Ideal

One continuous unbroken conductor around the *entire* measurement path

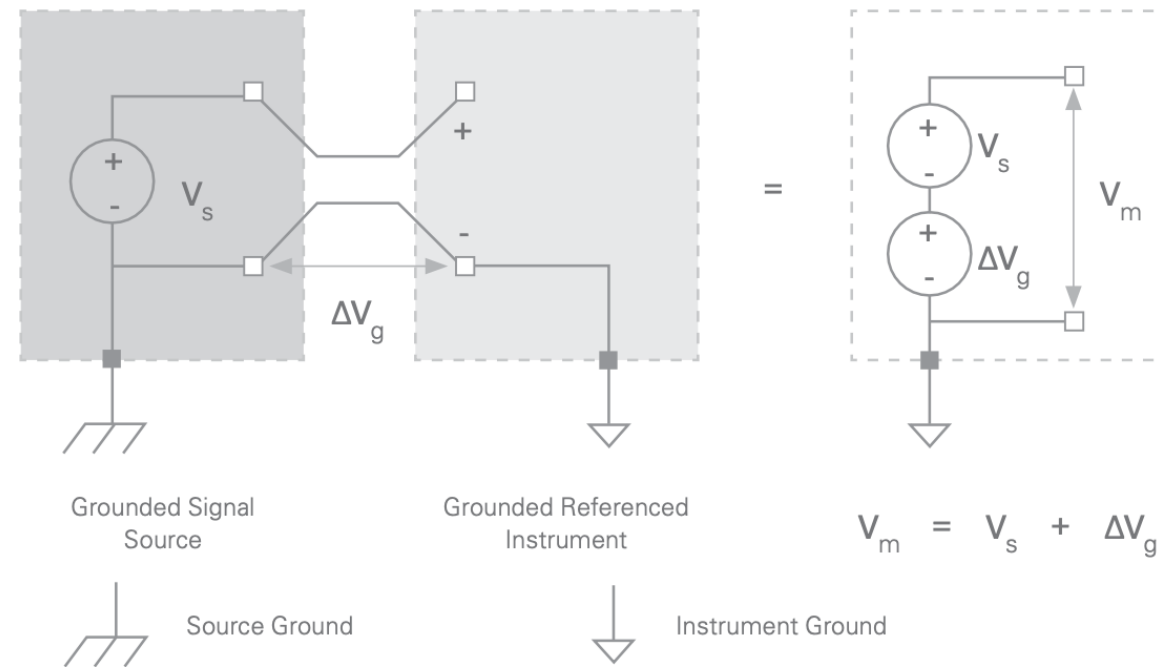


## More Practically

Targeted based on known/expected noise sources



# Avoiding Ground Loops



Ground loops can affect shielded differential measurements

- Shield currents can introduce noise
- Connecting shields at only one end eliminates the ground current





Minimize External Noise

# Practical Example of Shielding

## NI Manufacturing SMU Station

Station is fully shielded from external noise



# Best Practice 5: Guard Against Leakage Current

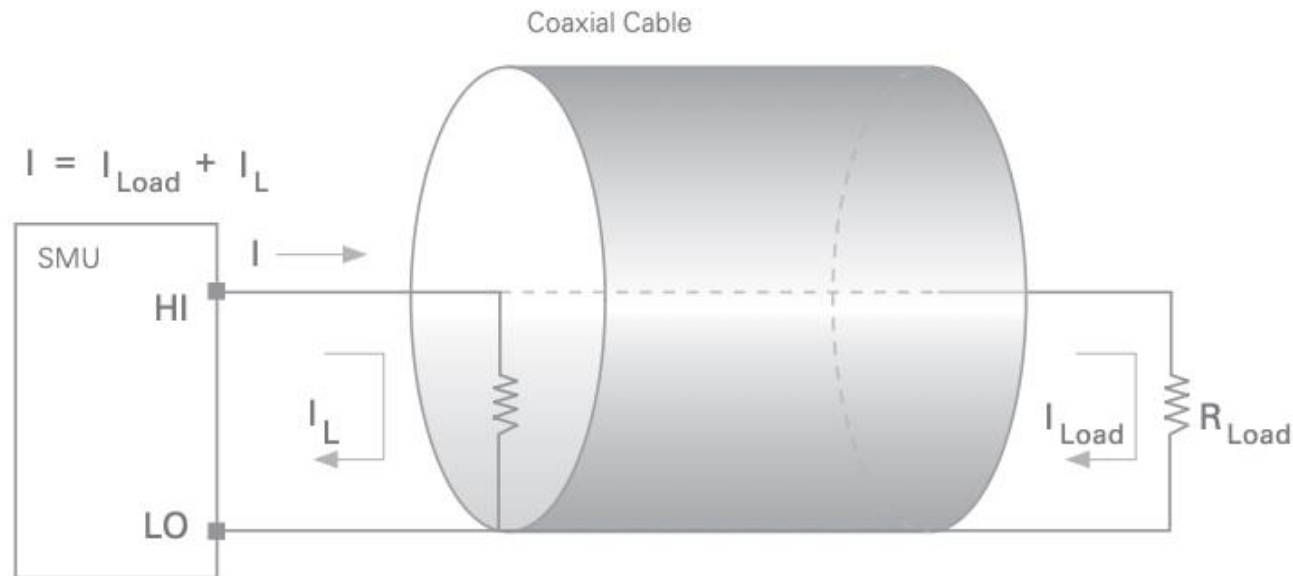




# Errors Introduced by Leakage Currents

Leakage currents can occur when there is a voltage difference across *any* finite resistance

- Cable dielectric, for example from signal to shield of a coax cable
- Open relay contacts
- Contamination, especially flux residue



Insulation resistance = 100GΩ  
Output voltage = 50V

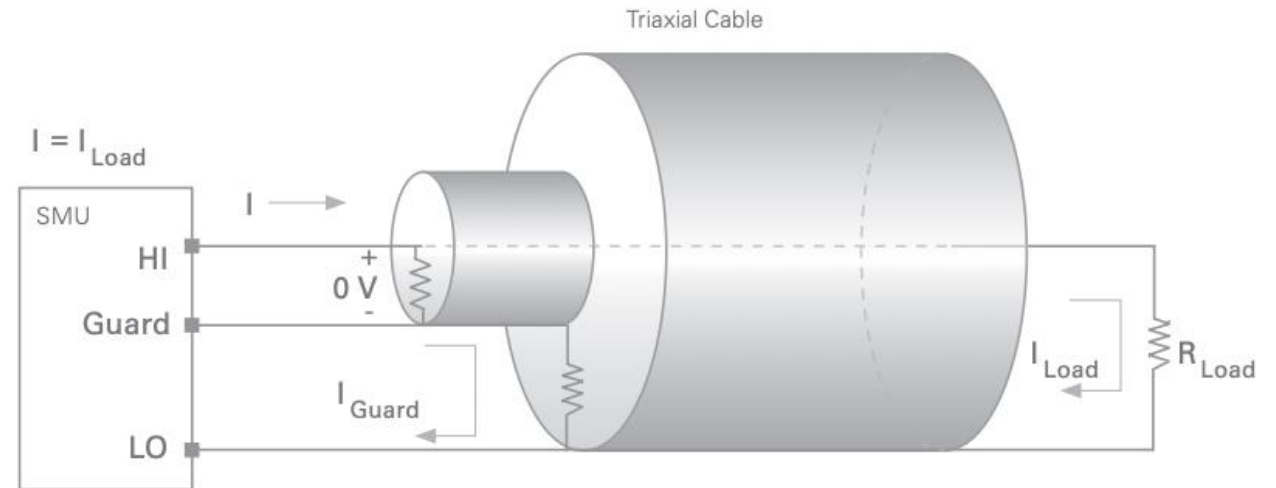
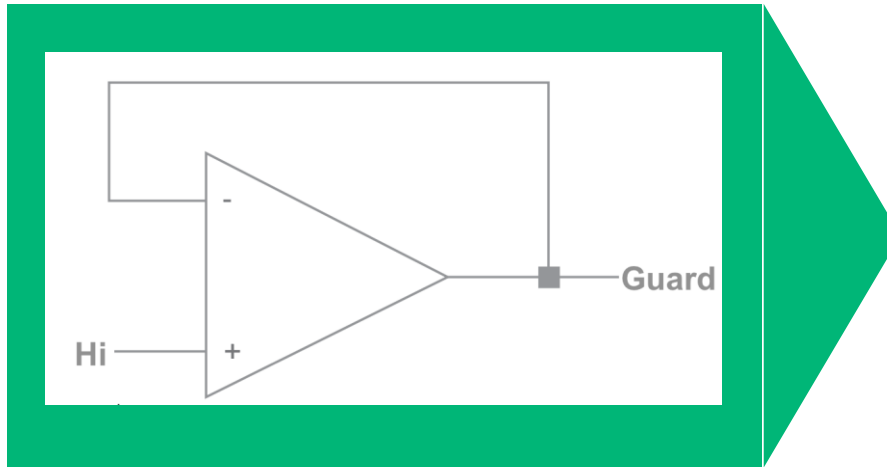
$$I_L = \frac{50 \text{ V}}{100 \text{ G}\Omega} = 0.5 \text{ nA}$$

# Guard Eliminates Leakages

Guard is a buffered signal at the same potential as Hi

By placing an additional shield around the signal that is driven to the same voltage, the voltage across the leaky insulation is reduced to 0V and no current flows

The configuration with three concentric conductors is a triaxial cable that is used heavily in low-current applications

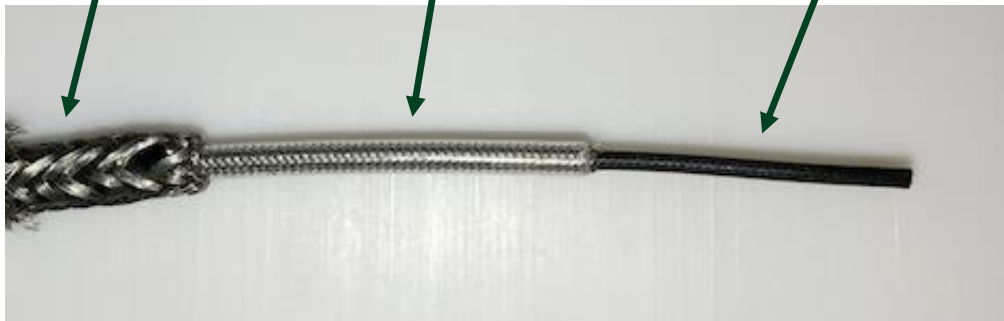


# Low Noise Cabling

Cabling used in low-current applications is often “low-noise”

- Normal cables generate charge when moved
- Low-noise cable has a semi-conductive layer
- This low-noise layer conducts noise to the guard shield
- Noise on HI is reduced several orders of magnitude

Outer Shield   Inner Shield   Low-Noise Layer



Center Conductor  
(after cleaning)





# Reducing Effective Parasitic Capacitance

Guarding also reduces the parasitic capacitance that must be charged by HI

Voltage across a capacitor changes at a rate  $\frac{dV}{dT} = \frac{i}{C}$

- SMU current limit and parasitic capacitance limit voltage slew rate
- 1 meter of coaxial cable has ~90pF of capacitance
- With a 1nA limit, voltage slew rate is limited to 11V/s
- Limitation can be avoided by charging the capacitance with guard



# Settling Time Example

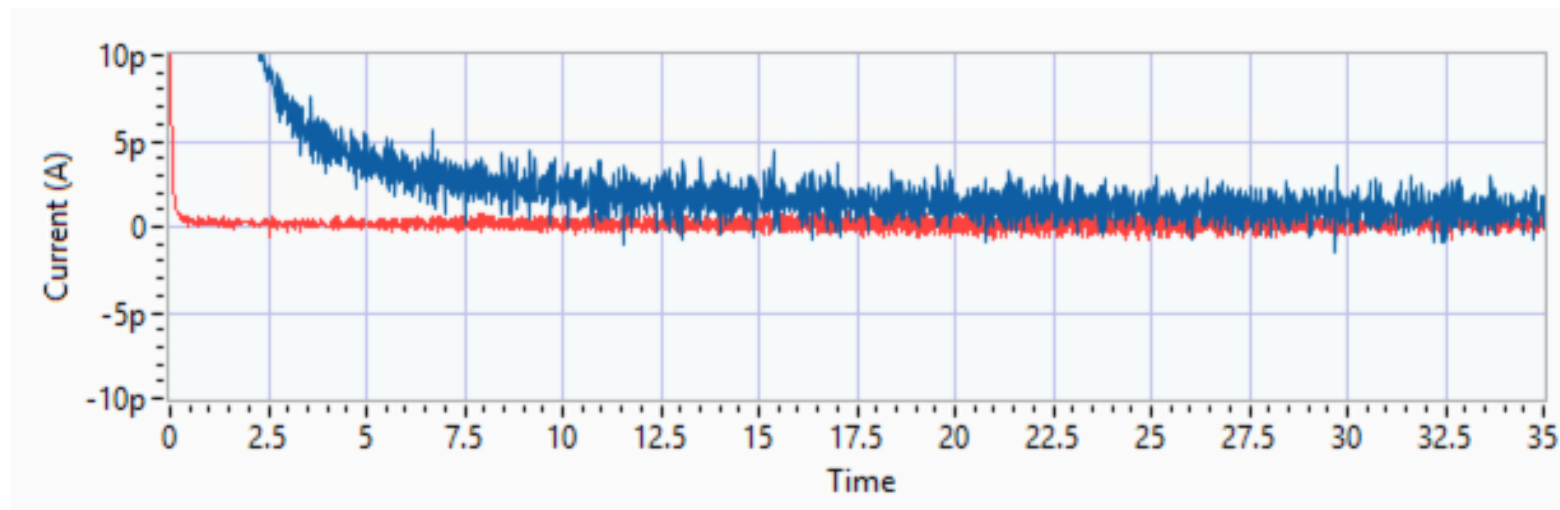
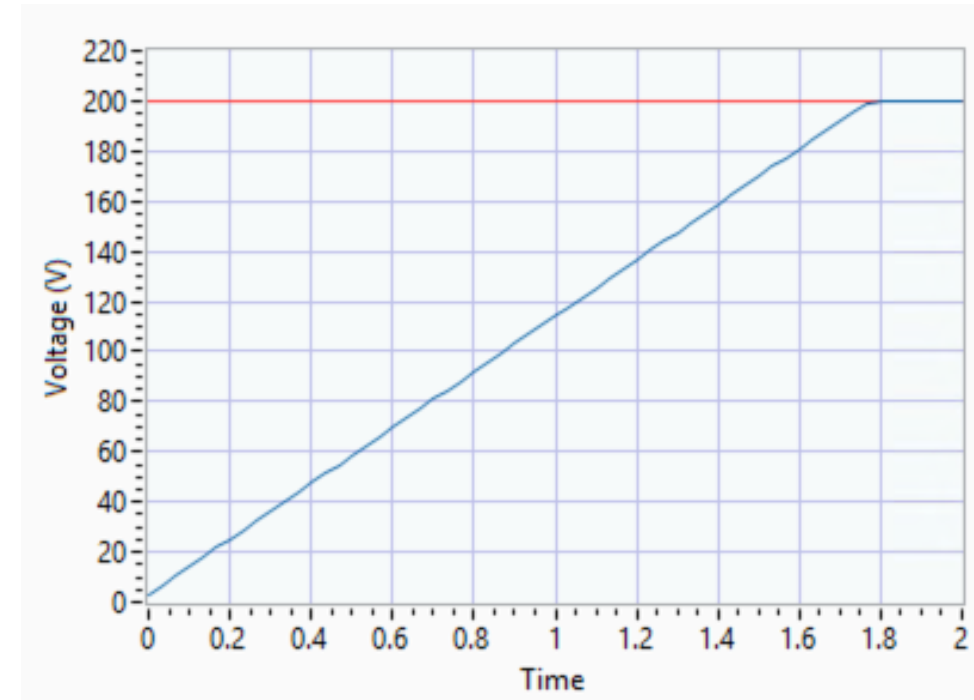
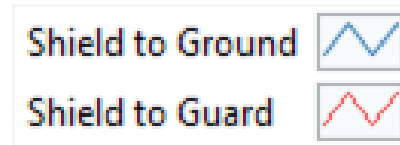
PXIe-4135 with 1m of coax cable, 200V step with 10nA limit

## Coax Shield to Ground

- Output reaches 200V in **1.8s**
- Current settles to **<2pA** in **30s**

## Coax Shield to Guard

- Output reaches 200V in **10ms**
- Current settles to **<1pA** in **200ms**

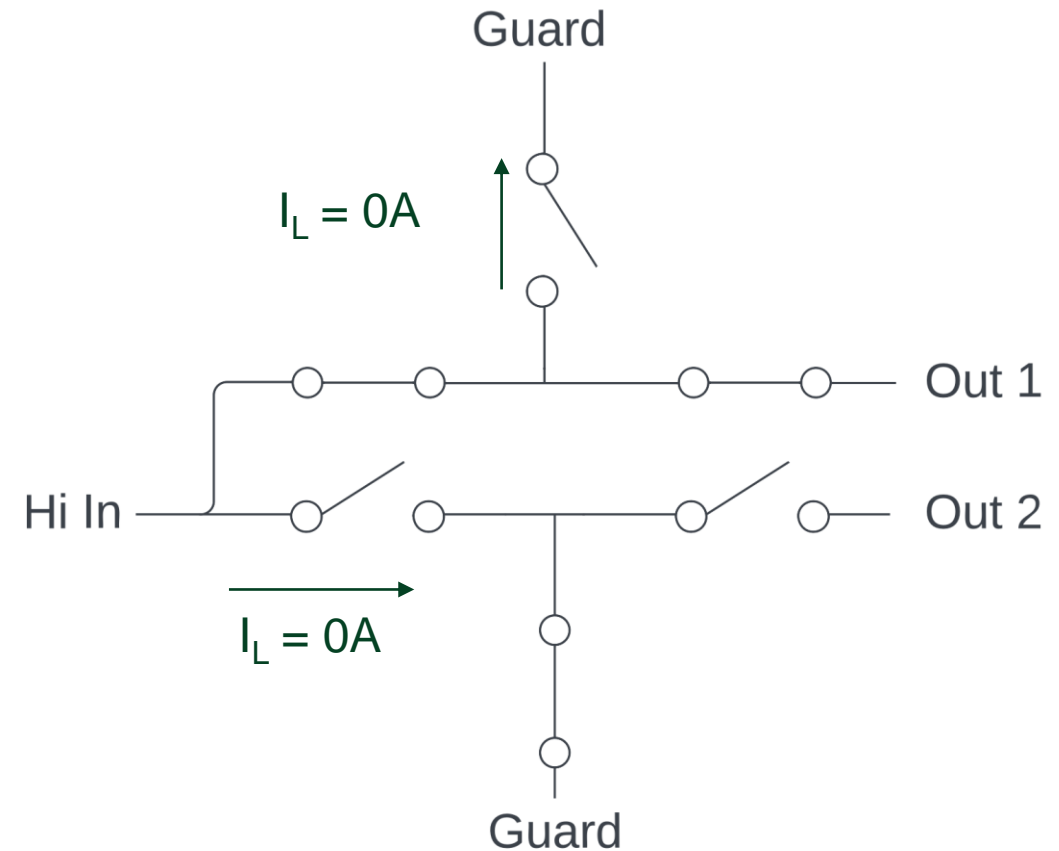


# Additional Optimizations Leveraging Guard

## Reducing Leakage in Switching

Relay leakage can be addressed with guard

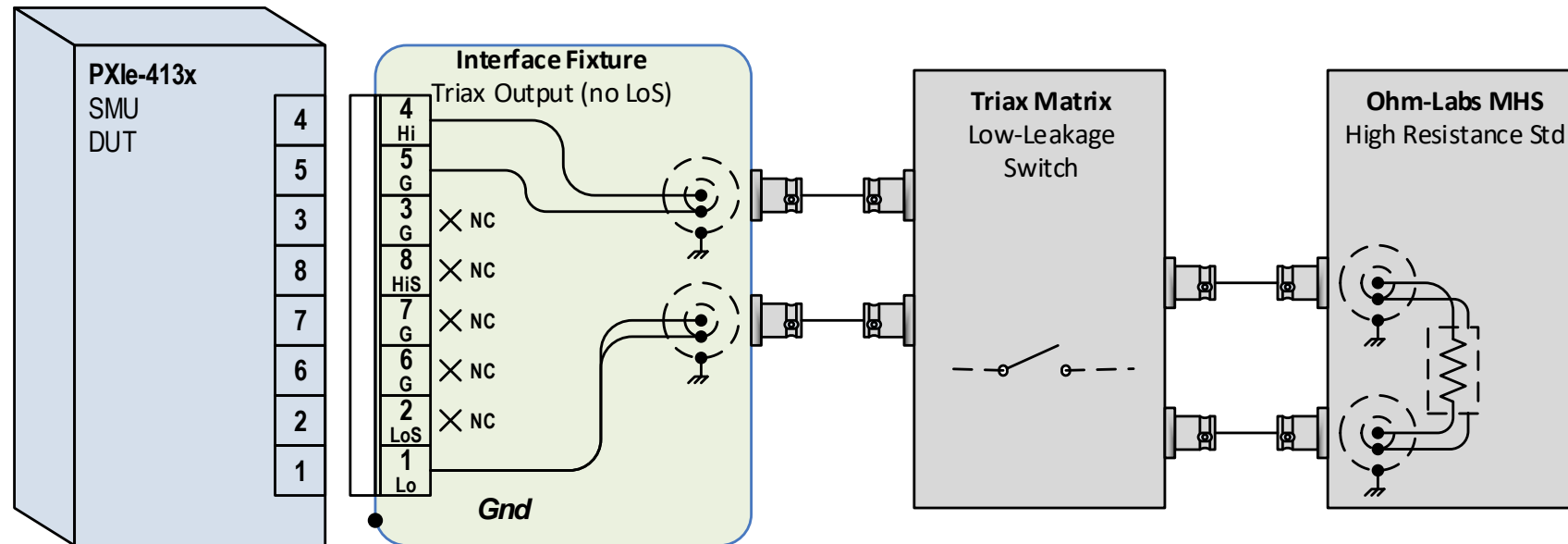
- A “guarded-T” topology adds a center node that can be connected to guard
- Example shows a 1:2 mux composed of two guarded-T sections
- Leakage is removed by guarding the center node



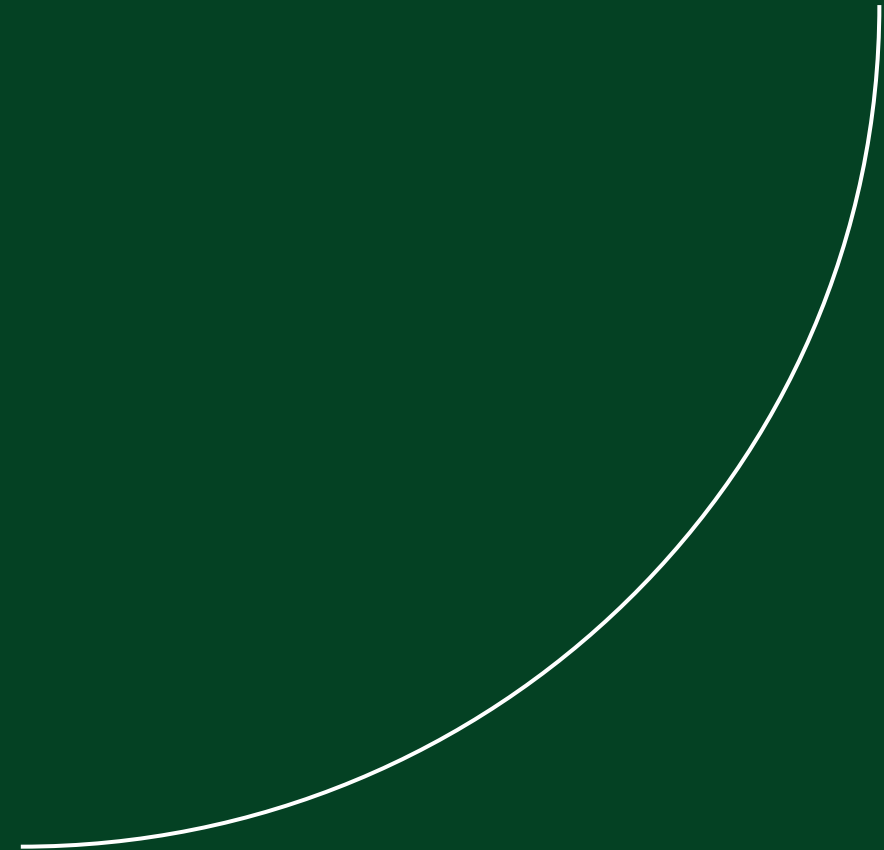
# Practical Example of Guard Application

## NI Manufacturing SMU Verification with High Resistance Standards

- Ohm-Labs MHS contains 7 fully-guarded standard resistors from 1MΩ to 1TΩ
- Entire path from DUT to standard is guarded triax, including switching
- With guard, 1GΩ measurement settles in **100ms** with **<1pA** leakage
- Without guard, settling time would be **>60s** with **100pA+** leakage



# Applying Best Practices





# Analyzing Measurement Errors

Model the circuit of your measurement with increasing detail to identify potential issues

- Start with sources and loads, then add representations for parasitic elements
- With a sufficiently detailed model, simple analysis (e.g. Ohm's law) often reveals potential issues

Component	Primary Parasitics	Additional Parasitics
Wires	$R_{\text{Wire}}$	$C_{\text{shield}}$ , $R_{\text{Insulation}}$ and $C_{\text{Stray}}$ to other conductors (maybe $I_{\text{fusing}}$ on a bad day)
Coax/triax cable	$R_{\text{wire}}$ and $C_{\text{shield}}$	$R_{\text{insulation}}$ , $I_{\text{triboelectric}}$ , $R_{\text{leakage}}$ due to contamination
Relay (closed)	$R_{\text{Contact}}$	$V_{\text{Thermal}}$ , $R_{\text{leakage}}$ and $C_{\text{Stray}}$ to coil
Relay (open)	$R_{\text{Insulation}}$ and $C_{\text{Open}}$	$R_{\text{leakage}}$ and $C_{\text{Stray}}$ to coil
Connector	$R_{\text{Contact}}$	$R_{\text{leakage}}$ and $C_{\text{Stray}}$ to other conductors
PCB	$R_{\text{Trace}}$	$C_{\text{stray}}$ , $R_{\text{leakage}}$ due to contamination

# Summary and Application Considerations

For low-impedance or voltage-sensitive applications:

- Use remote sense to address lead drop voltages
- Apply design best practices to minimize voltage offsets, or compensate for them

For high-impedance or low-current applications:

- Shield cables and other sensitive part of the measurement path
- Use guard to reduce the impact of leakage currents and parasitic capacitance

For all, especially precision, applications:

- Perform external calibration and self-calibration regularly to ensure instrument performance
- Model the full measurement path to anticipate and account for all sources of error

---

# Questions?

A decorative white curved line is positioned in the bottom right quadrant of the slide, starting from the bottom edge and curving upwards and to the right.

# Resources

5 Best Practices for Maximizing DC Measurement Performance (white paper)

<https://www.ni.com/en/solutions/semiconductor/making-dc-measurements.html>

Thermal EMF and Offset Voltage

[https://www.ni.com/docs/en-US/bundle/ni-switch/page/switch/thermal\\_voltages.html](https://www.ni.com/docs/en-US/bundle/ni-switch/page/switch/thermal_voltages.html)

Offset Compensated Ohms

[https://www.ni.com/docs/en-US/bundle/ni-dmm/page/offset-compensated-ohms\\_1.html](https://www.ni.com/docs/en-US/bundle/ni-dmm/page/offset-compensated-ohms_1.html)