



More Motors? No Problem. Future-Proofing Your Test Systems In An Evolving Electrification Landscape



BRANDON BRICE NI



ALAN SOLTIS OPAL-RT



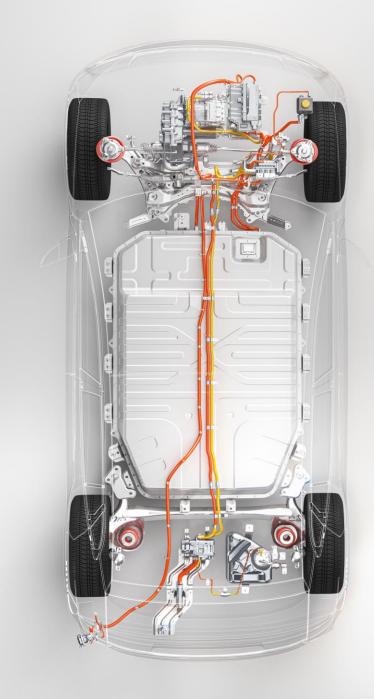
EV HIL Overview and Challenges

## Unique Challenges of EV HIL

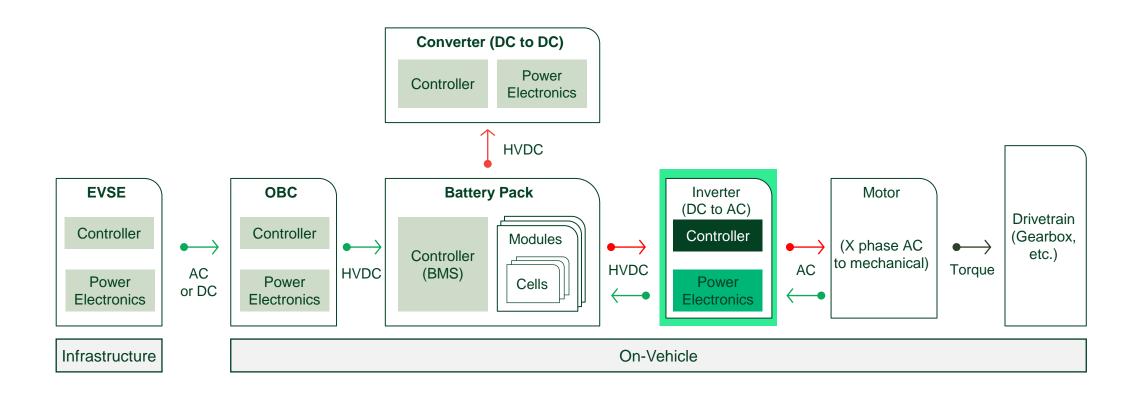
Near impossible to achieve complete automated test coverage with conventional dynamometers and road testing

Fast dynamic response of power electronics inverters and motors makes conventional HIL Test systems unsuitable for EV HIL

Power electronics simulation should be at least 100x faster than inverter switching frequency to achieve 2% accuracy 10kHz switching frequency = 1MHz simulation



### **EV** Traction Inverter



Control Tuning	Fault Handling
I/O Validation	Parameter Variation
Control Performance Analysis	Control Stability Analysis
State Machines	Thermal Management
Performance Mapping	Sensor Failure
DUT Bring-Up	Safe Operating Regions

EV HIL Overview and Challenges

## Testing Enabled Through HIL

Validate ECU performance over a wide range of parameter variations to achieve full test coverage

Verify ECU functionality in range of conditions, including extreme environments not easily created or replicated in the real world

Map test cases to requirements to ensure complete test coverage

Perform regression tests with ease to quickly validate design iterations

### Top Priorities for NI Inverter Test System



Minimize the time and complexity for the test engineer

- When mapping the test and DUT needs to the required hardware
- Configuring the IO and signal paths in the tester
- Getting initial DUT communication working for "Hello World" (fault free DUT-tester setup)
- Getting models integrated into the tester toolchain



Improve model performance and integration with The MathWorks Simulink<sup>™</sup> tools

NI SOLUTION

### Inverter Test System

Signal-Level Traction Inverter Validation

HIL Real-Time Powertrain Simulation

1, 2, or 4 DUT Configurations

Integrated Model Workflow

Signal Banked Mass Interconnect

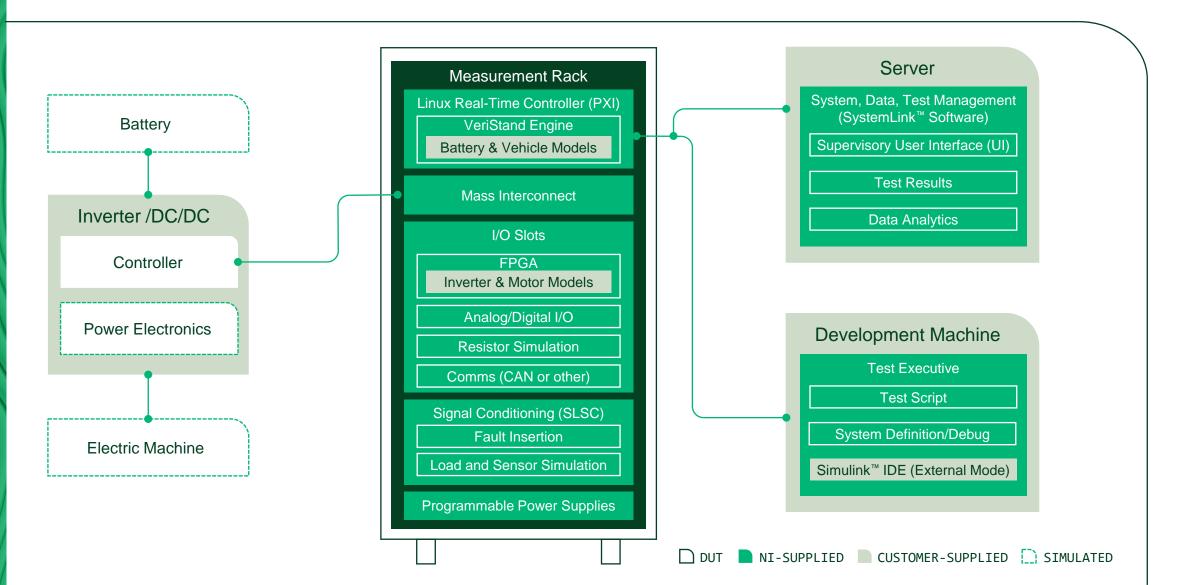
Faster Deployment and Procurement



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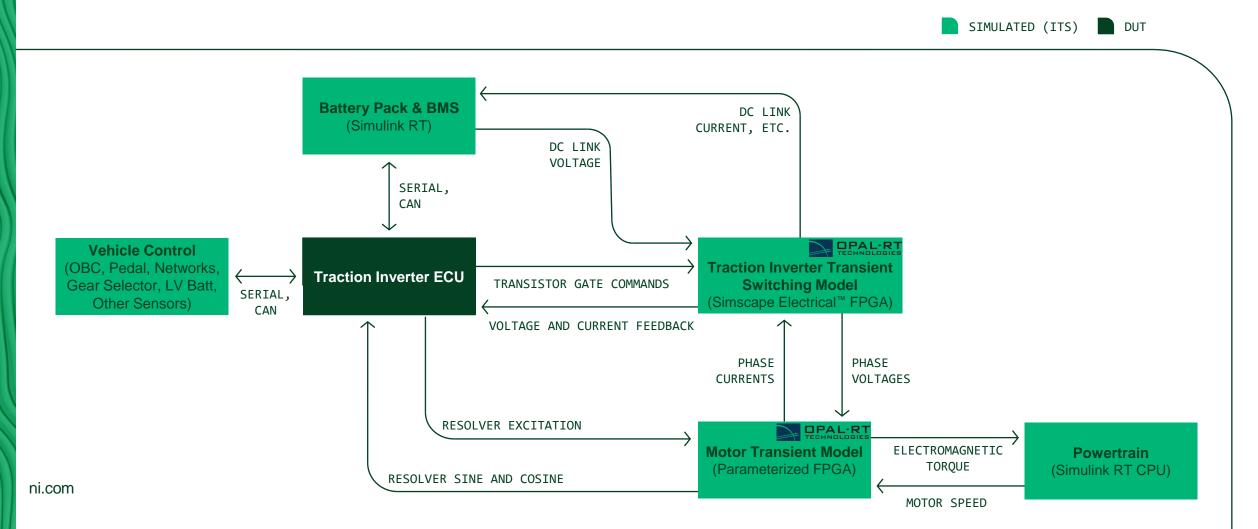
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### NI Inverter Test System Diagram



### NI ITS Traction Inverter HIL Test

### Real-Time EV Powertrain Simulation



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ITS Architecture & Advantages

### NI VeriStand

### **Embedded Test Software Functionality**

**RT Stimulus Generation** Hardware I/O Alarming **Deterministic Model Execution** MATLAB<sup>®</sup> and Simulink<sup>®</sup> Support Mapping and System Visualization Multi-chassis Synchronization **Closed-Loop Control** Data Logging **Test Automation** Calculated Channels User Account Management Multi-chassis Data Sharing Scaling and Calibration



# NI & Opal-RT Partnership

# Partnership built on several areas of collaboration:

- 1. NI VeriStand Power Electronics Add-On
  - Traction Motor Drive (Signal-Level & Power-Level)
  - Charging/OBC (AC/DC)
  - Battery Management Systems test (CMDE)
- 2. Systems Integration for NI
  - NI system integrator specialized in HIL
- 3. SLSC Module Design and Fabrication

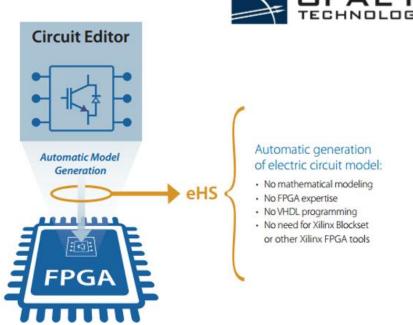


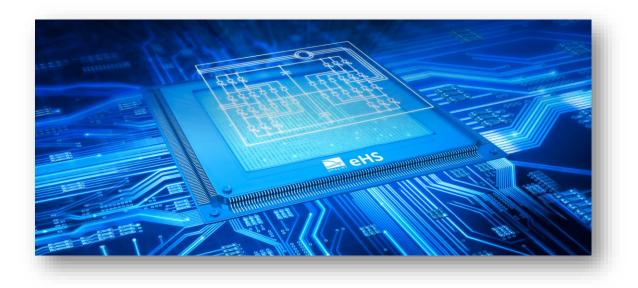




### **OPAL-RT's Power Electronics Add-On** is the **fastest** and **most flexible** FPGA-based electrical real-time solver

- Integrated into NI VeriStand
- Low I/O latency closed-loop including firing signals
- Enables coupling of more than 144 switches without artificial delays
- 200+ kHz support for PWM switching frequencies
- Sample time of electrical system solved by eHS ranges from 100ns to 2.5us





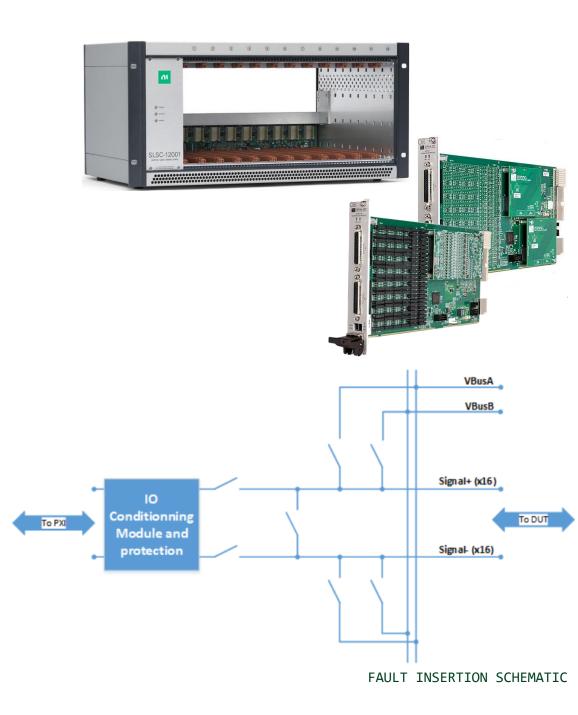
### Fault Insertion

SLSC – Switch, Load, and Signal Conditioning

### Available Faults (per channel):

- Open
- Short
  - Signal Pair
  - VBus
  - GND

Description	Fault Ins.
32 DIO: 5V to 33V	Ν
32 DO, High Speed	Y
16 DI   16 DO, High Speed	Y
16 AO: ± 20V	Y
8AI: ± 10 or 30V   8 AO: ± 20V	Y
32 Passthrough	Y
16 Resistor Sim.: $10\Omega$ to $10k\Omega$	Ν
	32 DIO: 5V to 33V 32 DO, High Speed 16 DI   16 DO, High Speed 16 AO: ± 20V 8AI: ± 10 or 30V   8 AO: ± 20V 32 Passthrough



Number of modules depends on config – refer to  $\underline{\text{ITS Signal List}}$  for more details



### **Overview Motor & Drives Simulation**

#### **Complete motor library**



Permanent Magnet Synchronous Machines (IPM, BLDC, SPM)



Induction Machines (DFIG, DFIM, SC)



Switched Reluctance Machines (SRM)

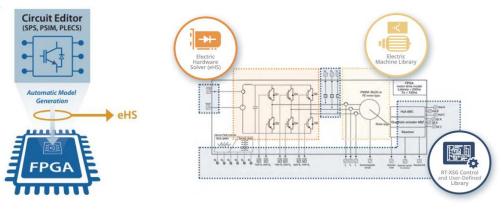
#### **High Performance**

- Down to 100 ns time step
- Up to 144 switches per FPGA no decoupling
- Up to 400 kHz switching frequency

### **Efficient Workflow**

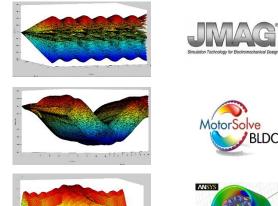
- Scenario Feature (automate up to hundreds of scenarios)
- Flexible modelling environment
  - SimScape Power Systems, Simulink

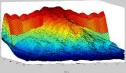
#### **FPGA Simulation solver**



#### Import of spatial harmonic tables (FEA)

• Torque, Flux & Inductance Table



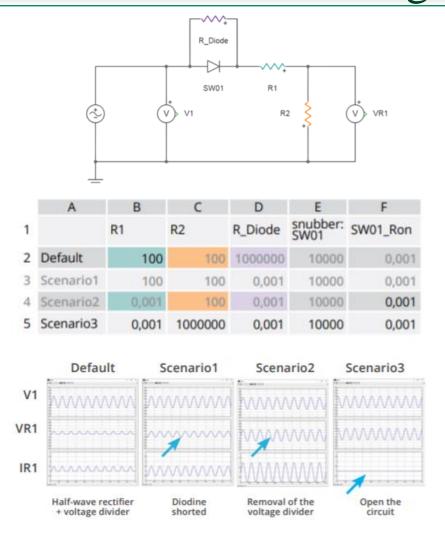




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### Scenarios & Faulting



- Create hundreds of testcases and fault scenarios on the circuit/machine natively in the add-on
- Automate scenarios using python, TestStand, ECU-Test, etc.

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File	Dual PMSM VDQ Local Control  Targets  Guide Controller  For Hardware  Custom Devices  For Custom Devices  For Custom Devices  For Custom Nodel 1  For Control Model 1  For Calculated Channels  For Stimulus  For Stimulus  For Calculated Channels  For Stimulus  For Stimulus  For Calculated Channels  For Calculated Channels  For Calculated Channels  For Calculated Channels  For Stimulus  For Calculated Channels  For Calculated Channe	Model         Name         Circuit Model 1         Description         Configure the circuit that will be simulated on the FPGA, including the Timestep and Scenarios.         Circuit Model File Path         C:\Users\Public\Docu\Dual PMSM VDQ Local Control\Circuit Model\PMSM_eH5_UB.mdl         Timestep (s)       Form Factor         0       eHSx64	Reload
	u <sup>2</sup> g Data Sharing Network ≌3 System Initialization	Scenario Configuration Scenarios File Path C:\Users\Administrator\Desktop\example.xls Use Scenarios?	N
* 0		Model Information       Minimum Timestep (s)     Number of Scenarios Used     Maximum Number of Scenarios       0     0     0	Refresh



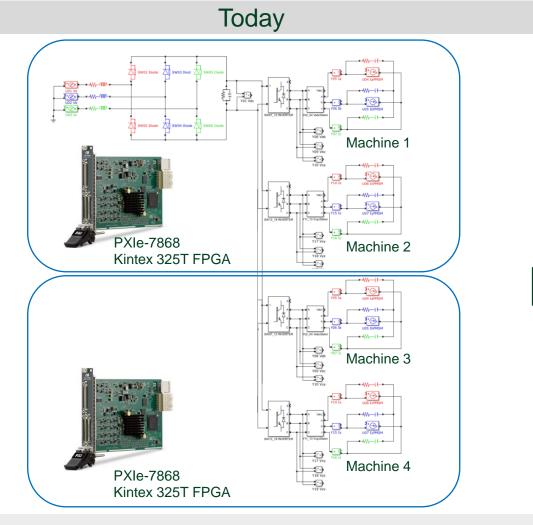
# Demo Video

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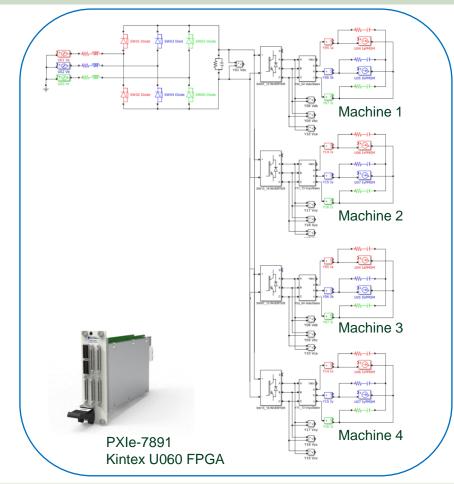
ITS Roadmap - H2 2023

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### New PXIe-7891 – Quad-motor support on single FPGA



With Kintex UltraScale FPGA



- Can deploy the entire model onto one FPGA (<1hr)</li>
- No latency between machines
- Split a model into two parts and validate them (>10hr)
- Expect communication latency between FPGA (300 ~ 700 nsec)

### Continuous Innovation on Electric Motor Models

#### IM ENHANCEMENTS



Induction Machines are widely used as industrial drives because they are selfstarting, reliable and economical.

#### PMSM (BLDC)



Permanent Magnet Synchronous Machines are known for its power density (power per unit of size/weight), and its higher speed capacity. EESM



BMW electrically excited synchronous moto

Electrically Excited Synchronous Machines are becoming an alternative to PMSM because of no rare-earth materials and high starting torque

- IM: Audi e-Tron SUV, Mercedes-Benz EQC, Tesla Model S, 3, X and Y on front axles and VW Group MEB cars on front axles.
- **PMSM**: Most popular for EV today, Hyundai Ioniq 5, Kia EV6, Tesla Model S, 3, X and Y on the rear axles. VW Group MEB cars on the rear axles, Jaguar i-pace, Audi e-tron GT, and Porsche Taycan, just to name a few.
- **EESM**: BMW iX3, iX, and i4; Renault Megane E-TECH and SMART EQ.



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## **ITS Benefits for EV HIL**



Model Integration



Advanced Compute



I/O Breadth



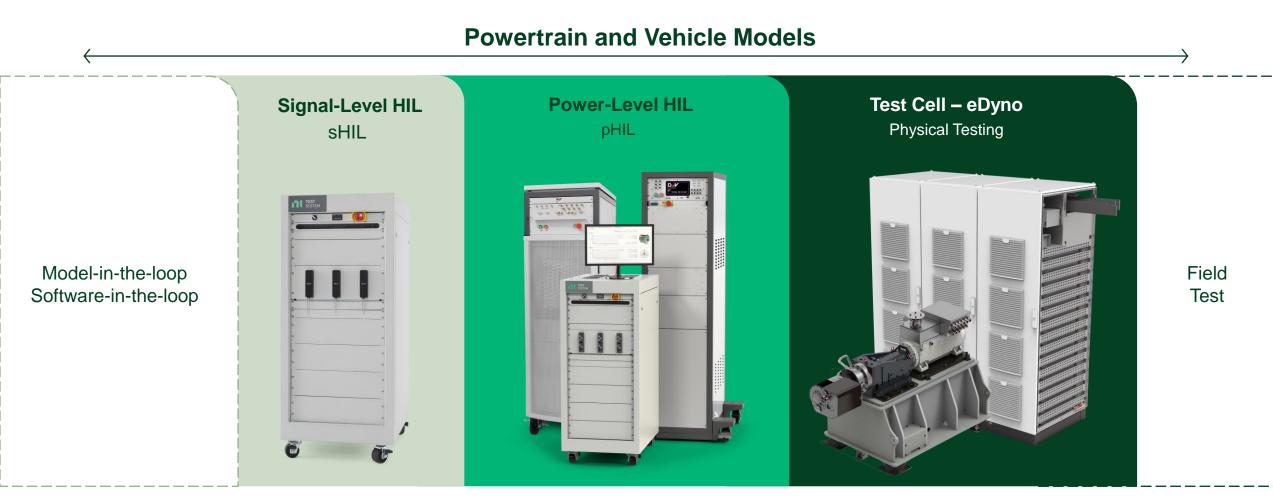
Customizability



Integration

## NI Offerings Along the Inverter Design Lifecycle

Reduce Development Time and Improve Engineering Efficiency Through Model Reuse



# Give us your feedback! Quick 2 Question Survey

In the mobile app, click into the session you would like to provide feedback for



10:15 AM Multichannel RF Data Recording 11:15 AM and Analysis

Meeting Room 19A

 Aerospace & Defense • Technical Session

10:15 AM Optimizing Validation Processes: 11:15 AM Building Complex Test Systems with Distributed I/O

- Meeting Room 19B
- Aerospace & Defense Technical Session

10:15 AM Panel: Continuous Integration (Cl/ 11:15 AM CD)—Don't Leave Home without It

- Meeting Room 12A
- Programming Essentials
   Technical Session

10:15 AM Using Python and TestStand to 11:15 AM Boost Your Test Development

Ballroom G

 Product & Technology • Technical Session

10:15 AM What Does Left Shifting Test 11:15 AM Mean in the NI Ecosystem?

Meeting Room 18A
 Transportation - Technical Session

#### **〈** Tue May 23

#### 🛨 Add to Schedule 🛛 🛗 iCal 🛛 👤 Check In

Optimizing Validation Processes: Building Complex Test Systems with Distributed I/O

#### Tue May 23 10:15 AM - 11:15 AM

Map Meeting Room 19B
 Aerospace & Defense • Technical Session

#### [] Surveys

#### Take Session Survey

In this session, learn to improve efficiency and reduce non-recurring engineering costs in validation labs by connecting multiple distributed line-replaceable unit (LRU) test systems. Also learn how to abstract LRUs and construct complex test systems faster and more efficiently using existing distributed I/O and edge computation technology.

# Click "Take the Session Survey"

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