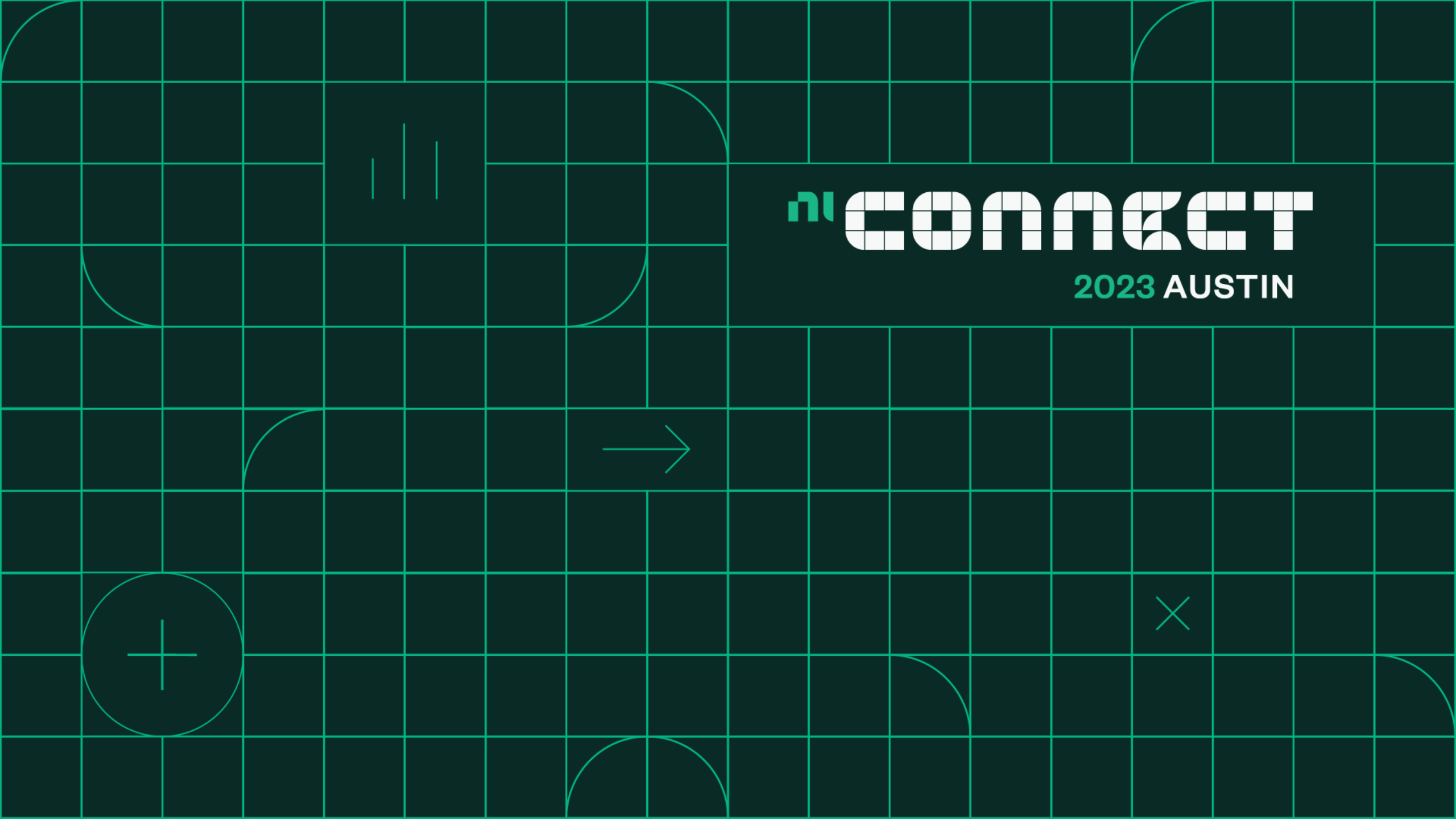
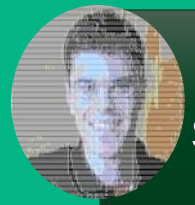

CONNECT
2023 AUSTIN

Optimizing Validation Processes:

Building Complex Test Systems with Distributed I/O

Jason Kreienheder
Principal Application Engineer



Matt Jacobson
Senior Application Engineer

Sintu Punnoose
Senior Application Engineer

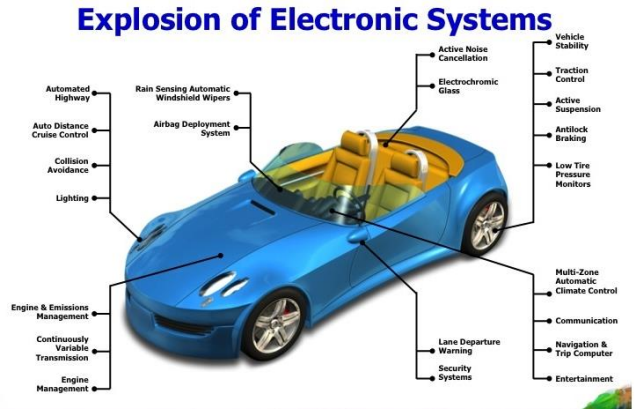
Agenda

- History of Distributed Systems
- Reasons for Distributing Systems
- Hardware Options for Distributed Systems
- Challenges of a Distributed System

History of Distributed Systems

History of Distributed Systems

It was around the year **1978**, when General Motors introduced the first ever electronics system in an automobile. And the rest as they say is history.



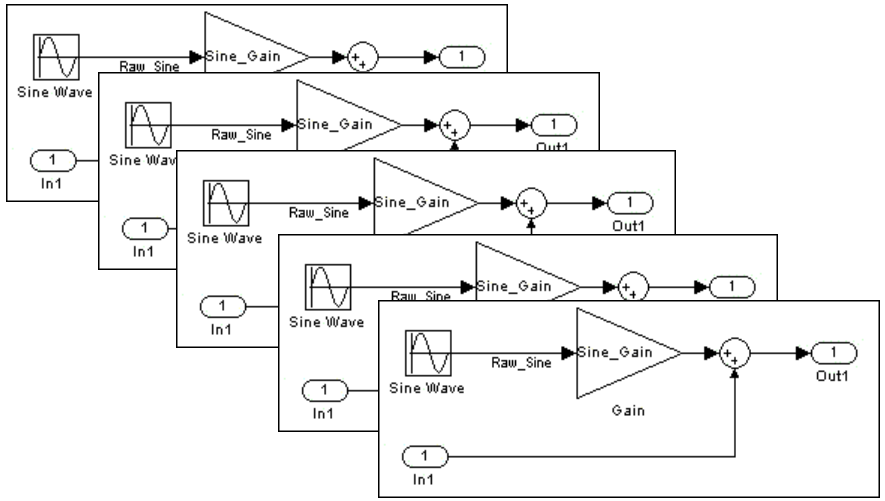
H009 (also called MacAir H009), introduced by McDonnell in **1967**, was one of the first avionics data buses. It is a dual redundant bus controlled by a Central Control Complex (CCC), with up to 16 Peripheral Units (PUs), synchronously communicating using a 1MHz clock. H009 was used in early F-15 fighter jets, but due its noise sensitivity and other reliability issues was replaced by MIL-STD-1553.

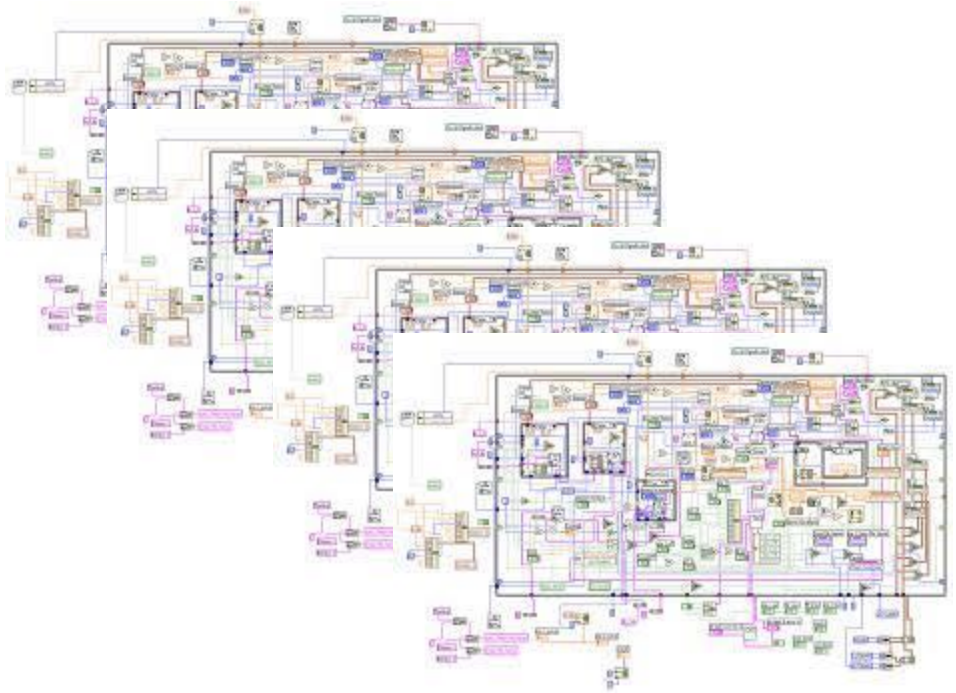
https://www.embitel.com/blog/embedded-blog/automotive-control-units-development-innovations-mechanical-to-electronics
https://en.wikipedia.org/wiki/MIL-STD-1553

Reasons for Distributing Systems

Reasons for Distributing Systems

Distributed Processing



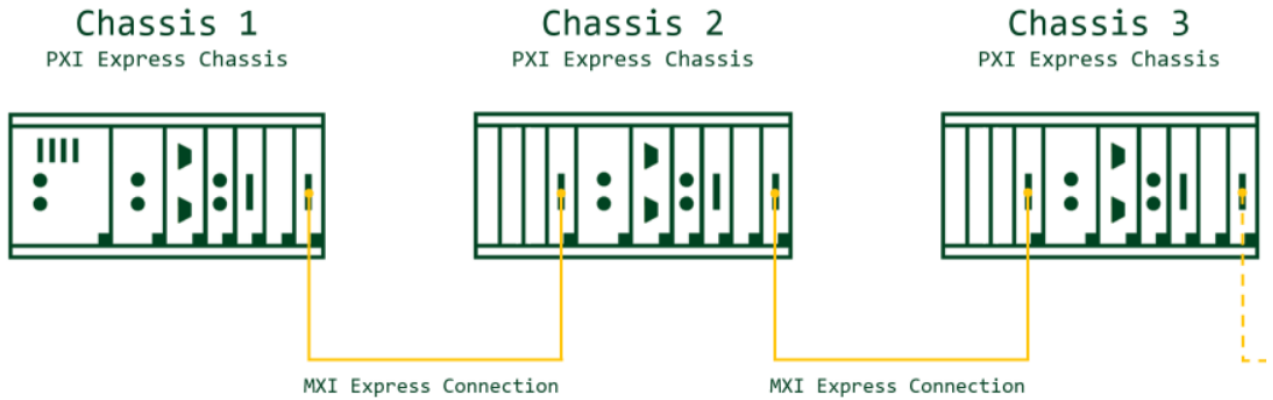


Reasons for Distributing Systems

Reduced Wiring

Reasons for Distributing Systems

MXI Expansion



1. PXIe Chassis Front Connections

- Sufficient processing power on a single controller
- A need for more slots of a certain type i.e. PXI, PXIe
- I/O segregation based on rack layout and wiring considerations

Hardware Options for Distributed Systems

MXI Express

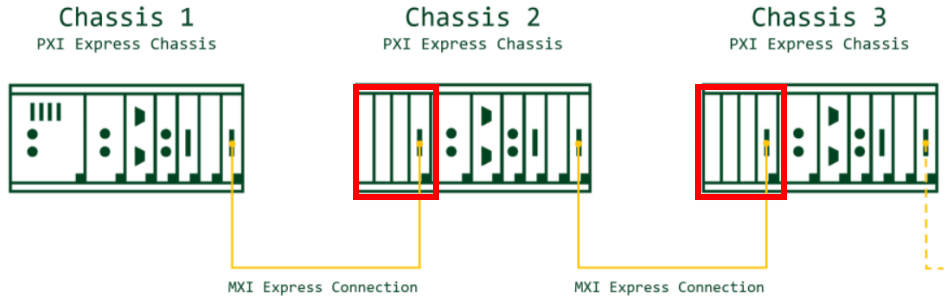
CompactRIO

CompactDAQ

EtherCAT

MXI Expansion

PXI Remote Control Module Options



1. PXIe Chassis Front Connections

PXIe-8360

PXIe, x1, MXI-Express Interface, PXI Remote Control Module

FROM $ 1,435.00

Bandwidth: <192 MB/s
Topology: 1:1
Distance: 7m

PXIe-8399

PXIe, Gen 3, x16, 2-Port PXI Remote Control Module

FROM $ 4,699.00

PXIe-8398

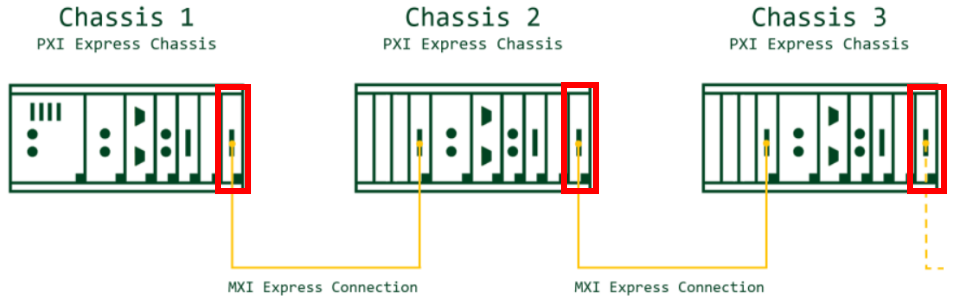
PXIe, Gen 3, x16 PXI Remote Control Module

FROM $ 3,046.00

Bandwidth: <13.7 GB/s
Topologies: 1:1, Star & Daisy Chain
Distance: < 200m

MXI Expansion

PXI Bus Extension Module Options



1. PXIe Chassis Front Connections

PXIe-8364

PXIe, x1, MXI-Express Daisy-Chain Copper Interface, PXI Bus Extension Module

FROM $ 1,733.00

Bandwidth: Low/Fixed 192 MB/s
Topology: 1:1
Distance: 7m

PXIe-8394

PXIe, x8, Gen 3 MXI-Express Daisy-Chain Interface, PXI Bus Extension Module

FROM $ 3,722.00

Bandwidth: High/Flexible 13.7 GB/s
Topologies: 1:1, Star & Daisy Chain
Distance: 200m

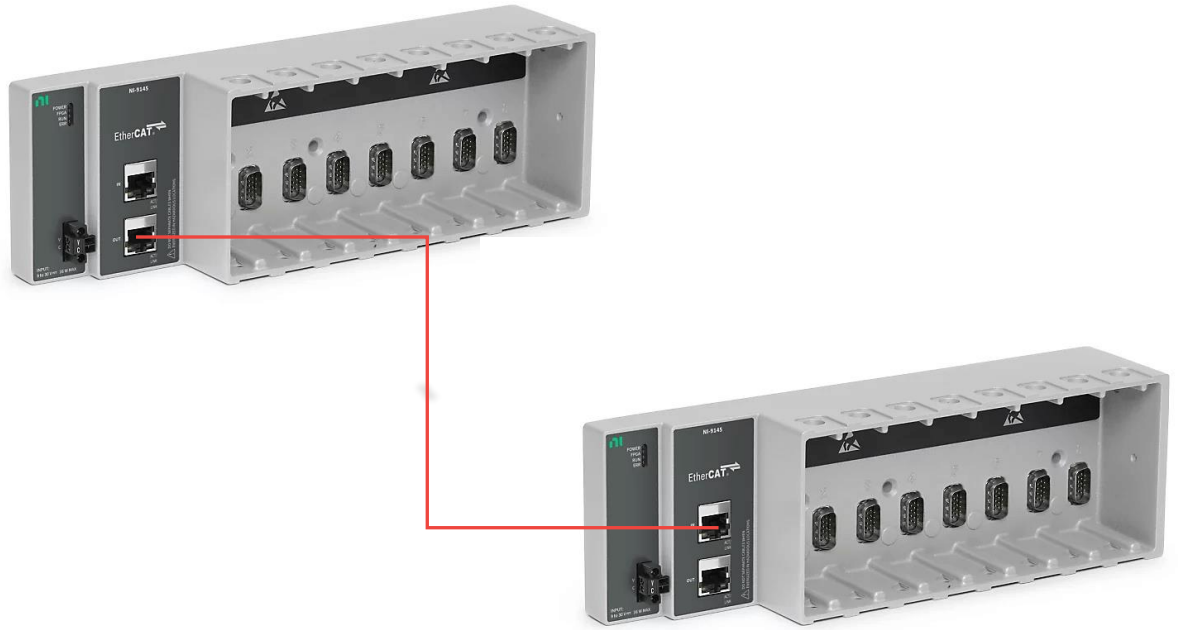
CompactDAQ

- USB or Ethernet connectivity
- Slot count options 1,4,8 and 14
- Monitoring only
- TSN Enabled on Ethernet

Experience Lounge Demo: 2,000 - Channel Structural Test System

EtherCAT

- Chassis are daisy chained from the RT controller standard networking cables
- Control and Monitoring
- Users can utilize the 9145 chassis in either Scan Mode or leverage the backplane FPGA to implement custom logic in FPGA mode.
- Requires NI Scan Engine



Experience Lounge Demo: Coordinated Control for Dynamic Actuator Test

CompactRIO

- NI is trending away from MXI on cRIO
- Fewer options for data sharing between controllers
- Not a typical in distributed systems other than an EtherCAT master

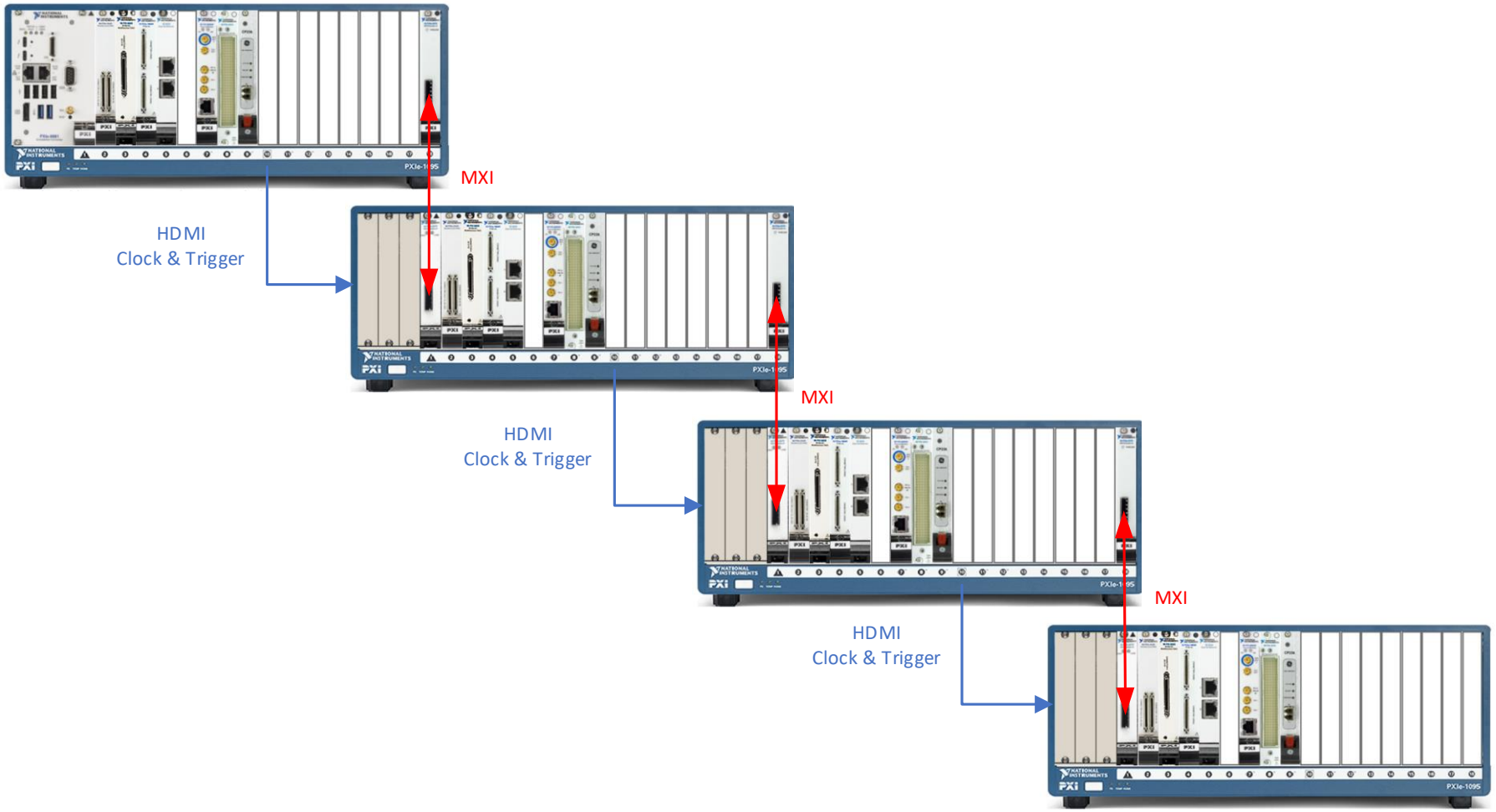
Technology	Physical Distance Between Nodes	Accuracy[1]	Global Traceable Time?	Cabling	Timestamp?	Recommended Hardware	Synchronized Subsystem
Signal-Based[5]	<100 m	Varies (Refer to the manual)	No	Varies	No	NI-9469, trigger, or NI-9402	FPGA, and NI-DAQmx/DSA[3]
IEEE 1588 with hardware support (IEEE 802.1AS or default profile)	Within subnet	<1 µs	Optional	Standard Ethernet	Yes	Built-in Ethernet port on TSN enabled cRIO controllers	System Clock, FPGA, and NI-DAQmx/ DSA[4]
IEEE 1588 with software support (default profile)	Within subnet	1 ms	Optional	Standard Ethernet	Yes	Built-in Ethernet port on all Linux RT cRIO controllers	System Clock
SNTP[5]	Global (access to NTP server)	10's of ms	Yes[2]	Standard Ethernet	Yes	Built-in Ethernet port on all Linux RT cRIO controllers	System Clock
GPS[5]	Global	100 ns	Yes	N/A	Yes	NI-9467	FPGA
IRIG-B[5]	Varies	100 ns	Optional	Varies	Yes	NI-9402	FPGA

Challenges with a Distributed System

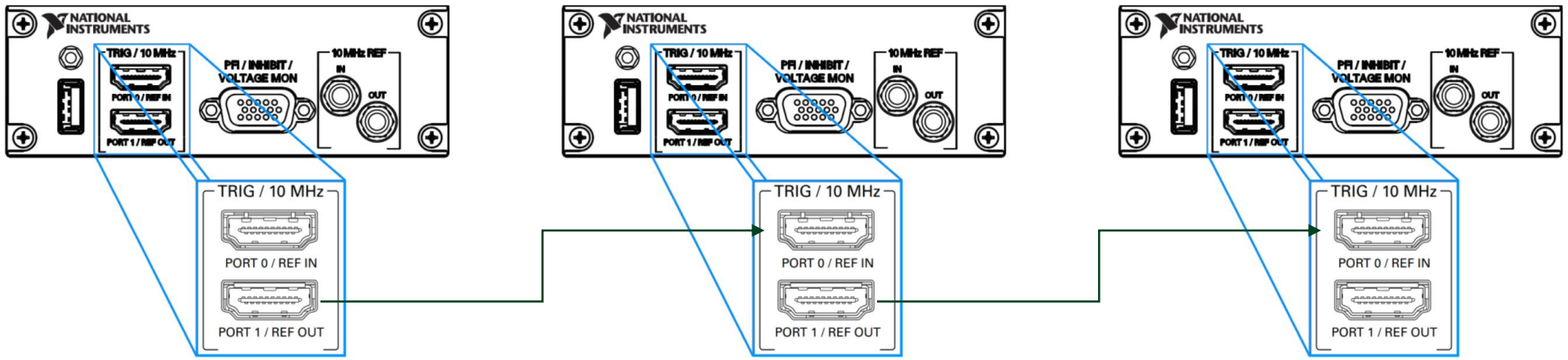
Synchronization

MXI Expansion

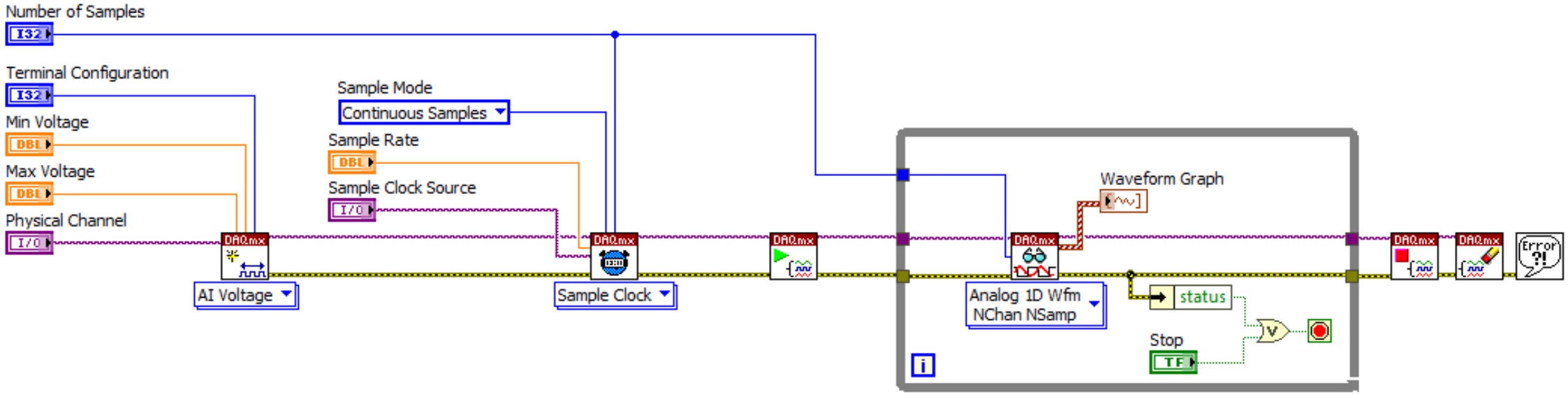
Hardware Configuration Overview



Signal-Based Synchronization

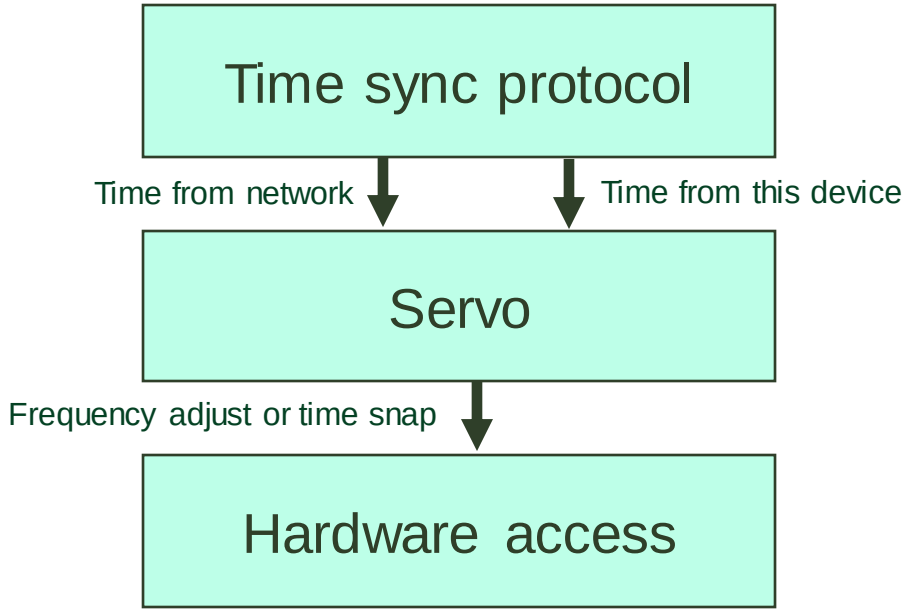


Signal-Based Synchronization



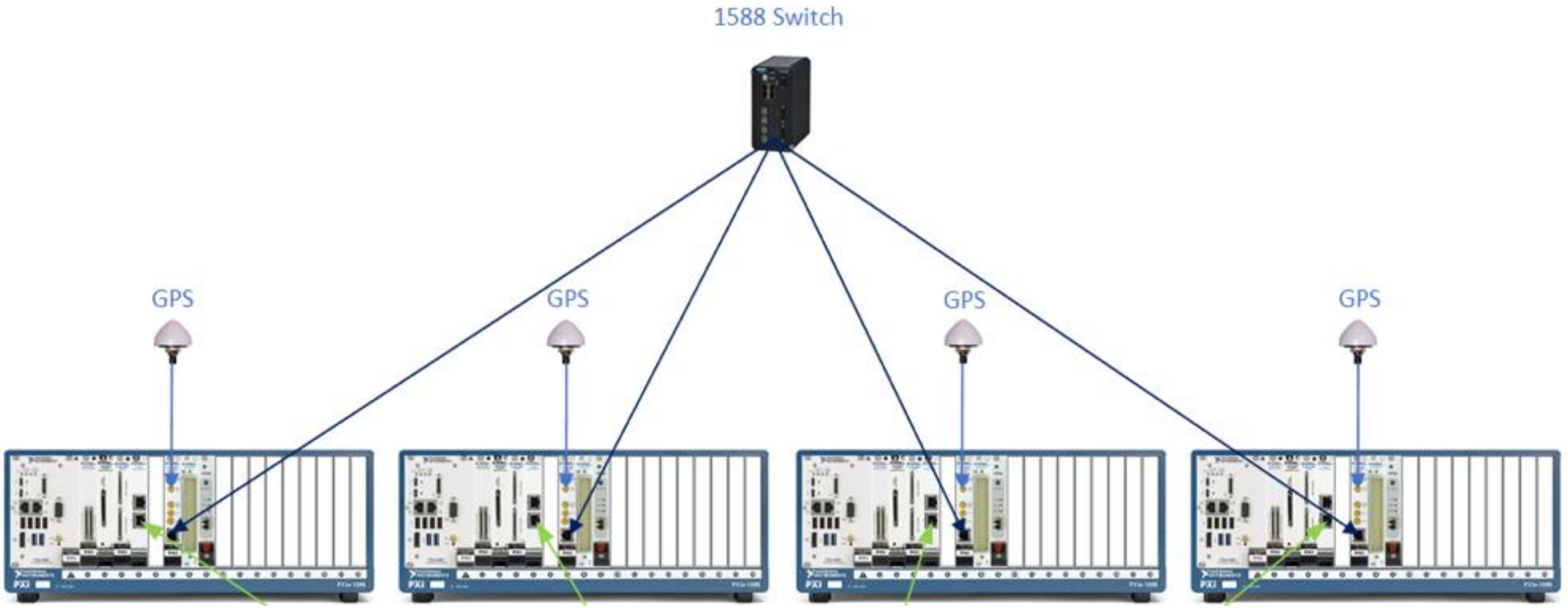
Time-Based Synchronization

- Time sync protocol
  - 1588, 802.1AS, GPS
  - AKA “Time Reference”
- Servo
  - Control the rate of time change in response to time correction information
  - Decides when to “snap” time
- Hardware access
  - Hardware-specific code adjust a hardware clock
  - AKA “Time Keeper”



Many different implementations of all these components, but the same idea

Time-Based Synchronization



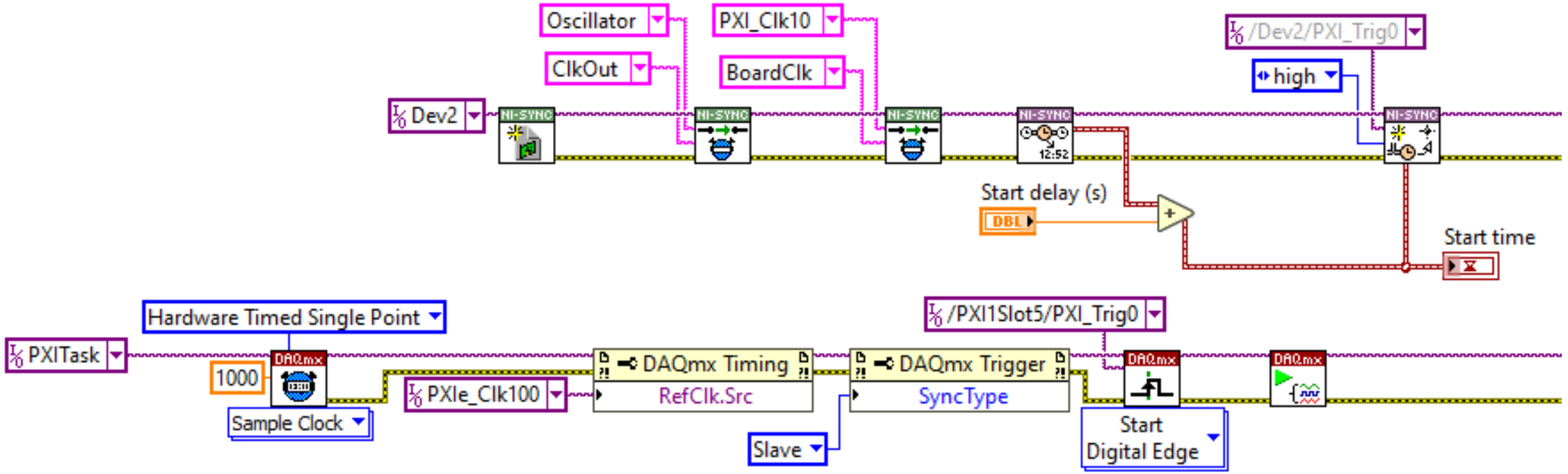
Translating Time Protocols

- May have requirement to synchronize to protocol (e.g. GPS) and have NI device which cannot directly synchronize to that protocol (e.g. cDAQ)
- Many indoor devices which must be synchronized to GPS
- Devices in system from multiple distributors which synchronize to different time protocols

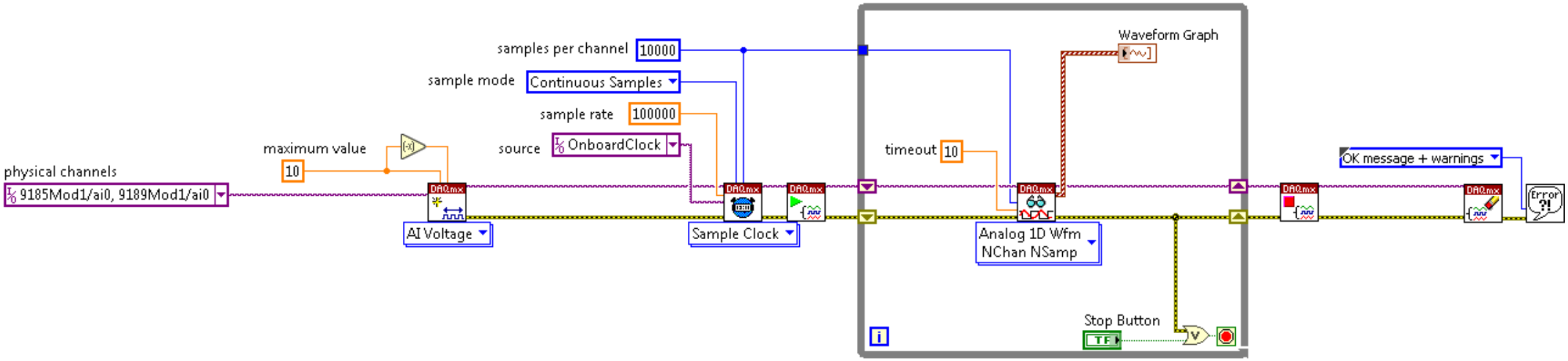
Time-Based Synchronization - PXI

- 6683H module synchronizes onboard oscillator to time reference (1588, GPS, etc.)
- 10MHz clock is routed through front of 6683H to 10MHz clock input of PXIe chassis
- All tasks reference PXIe backplane clock
- Either 6683H generates start trigger at specified time or start trigger is timed by 6683H

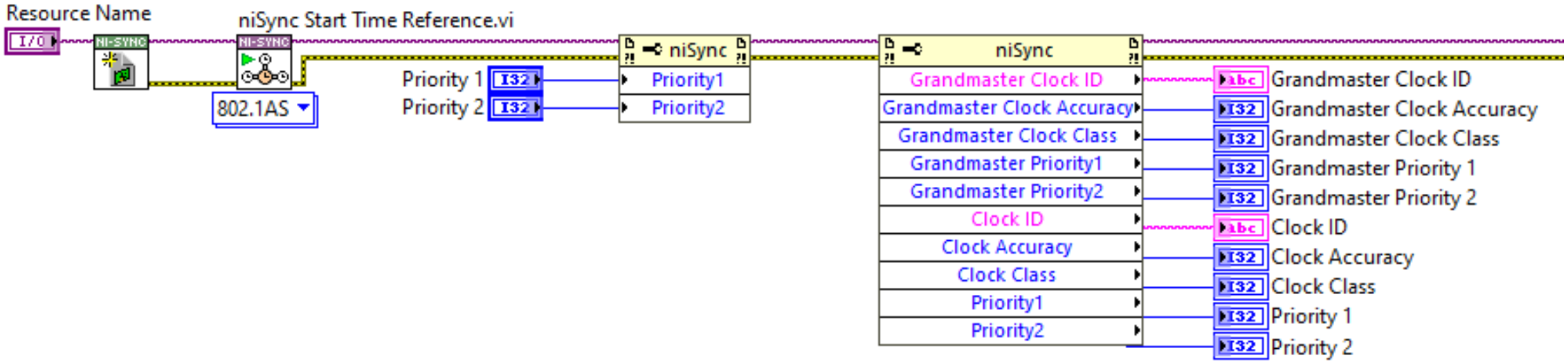
Time-Based Synchronization – PXIe DAQmx



Time-Based Synchronization – cDAQ/cRIO DAQmx



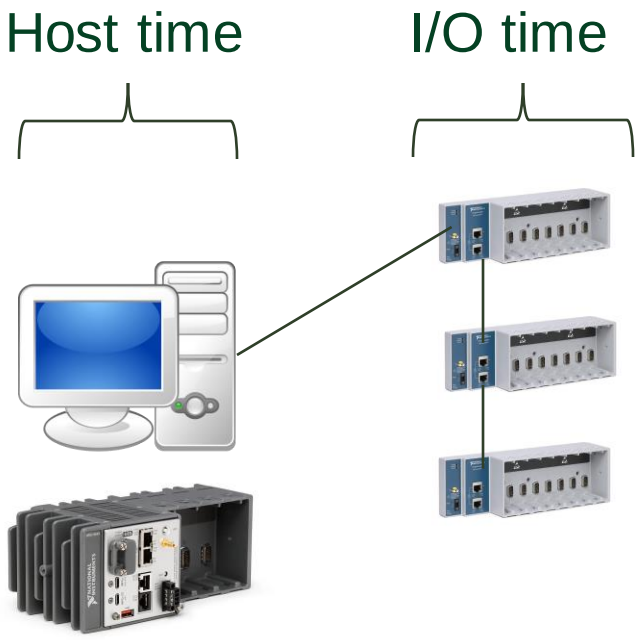
Time-Based Synchronization – cDAQ/cRIO DAQmx



Timescales

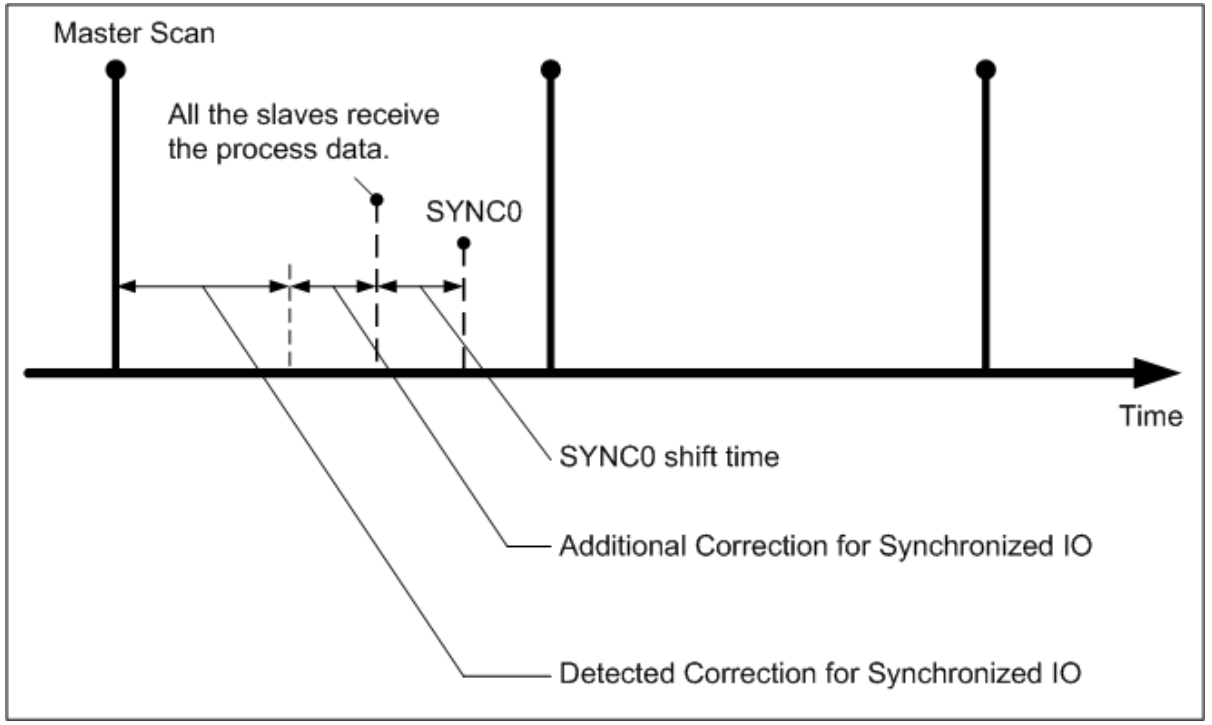
The platform has two conceptual timescales:

- I/O time
  - determined by NI hardware configuration and other network devices
- Host time
  - Determined by OS configuration
  - Usually same time as a wall clock



EtherCAT Synchronization

1. Master sends broadcast to all slaves
2. Slaves latch value of internal clock when message is received
3. Master reads all latched values to calculate delay
4. Calculated delay offsets are sent to slaves



Challenges with a Distributed System

Data Communications

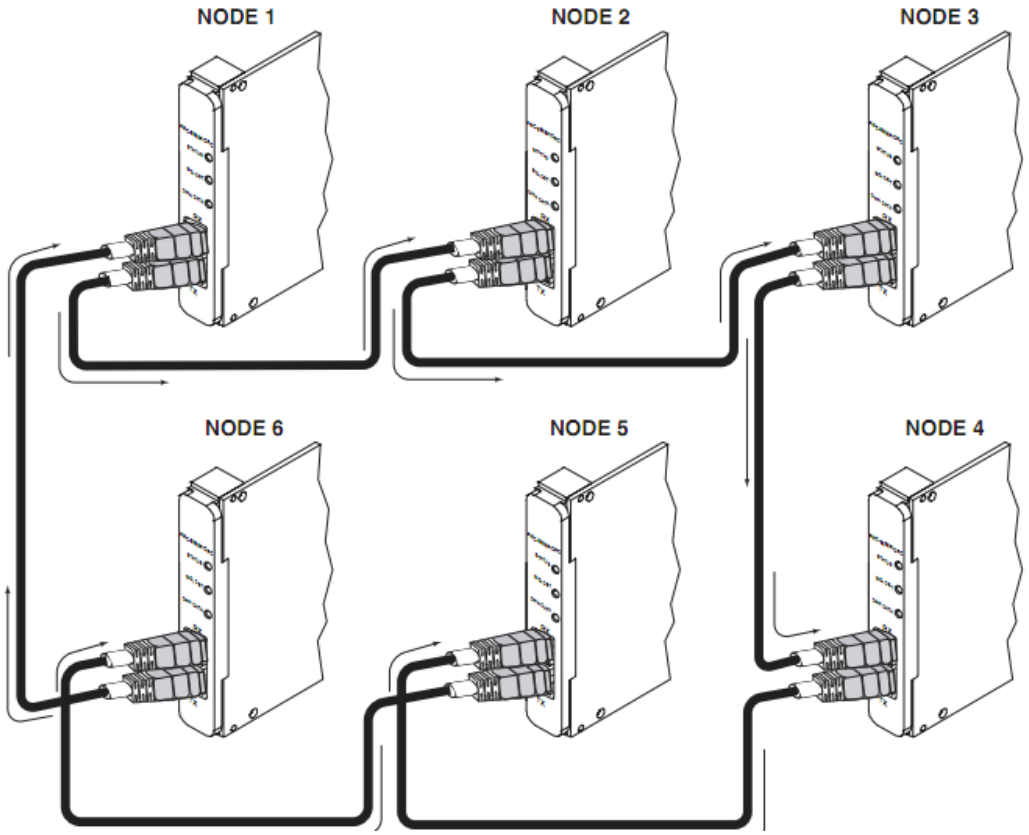
Data Communications

Parameters to check for Data Communication for Distributed Systems

- Latency
- Throughput
- Quality of Service
- Connection Topology

Reflective Memory Network

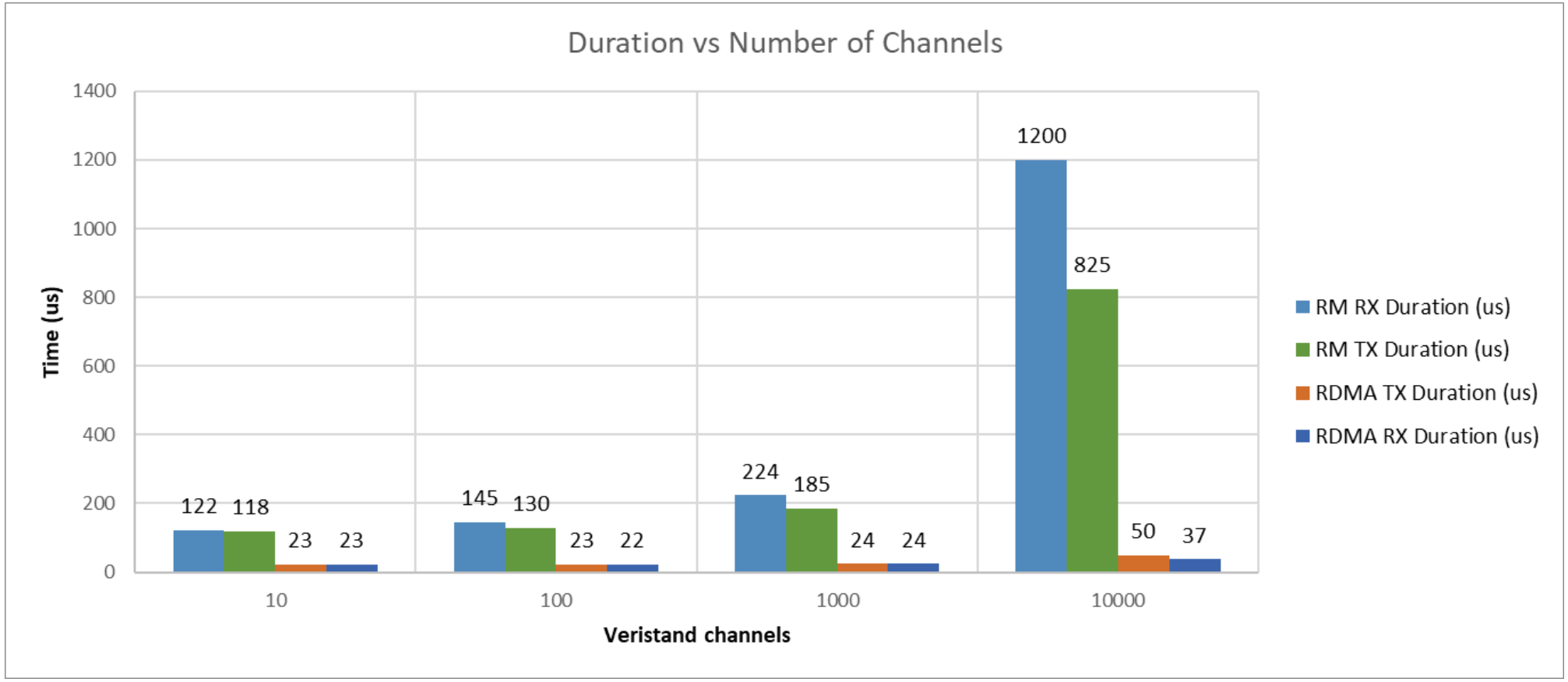
- Reflective Memory node card provides a
  - high-speed,
  - low latency,
  - deterministic interface
- Allows data to be shared between up to 256 independent systems (nodes) at rates up to **170 Mbyte/s.**
- Each Reflective Memory board may be configured with 128 MB or 256 MB of onboard SDRAM.
- The local SDRAM provides fast Read access times to stored data.
- Writes are stored in local SDRAM and broadcast over a high-speed fiber-optic data path to other Reflective Memory nodes.
- The transfer of data between nodes is software transparent.



RDMA Semantics

- High-performance 25-Gigabit remote direct memory access (RDMA) interface for PXI Express.
- Includes two 25-Gigabit Ethernet SFP28 ports in a single-slot PXI Express module and supports RDMA
- Similarities to TCP:
  - Listen, Accept, Connect, Close
  - One listener can accept connections from multiple connectors (each is independent stream)
  - Multiple simultaneous connections allowed
- Differences:
  - Directionality of stream set at connection time (send or receive)
  - Explicit configuration step to setup buffer size and number of overlapped operations

Reflective Memory vs RMDA in VeriStand



Basic Performance of RDMA

- Streaming bandwidth limited only by:
  - PCIe bandwidth
  - Link speed
- Latency very low
  - Dominated by interrupt/event through OS (when used)

Standard event/interrupt mode

```
[     10032] [ INFO] One-way latency:
[     10032] [ INFO]   -- min     : 14.547 us
[     10032] [ INFO]   -- mean    : 18.5482 us
[     10032] [ INFO]   -- max     : 29.374 us
[     10032] [ INFO]   -- std. dev: 2.79786
```

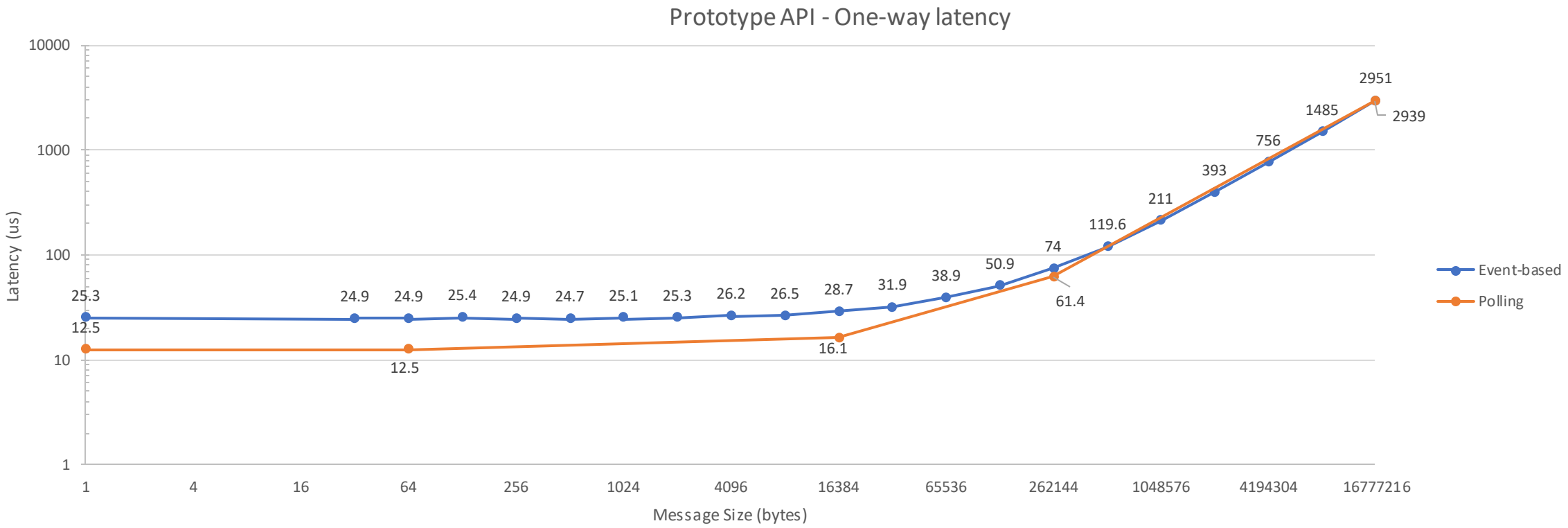
Polling mode

```
[     10174] [ INFO] One-way latency:
[     10174] [ INFO]   -- min     : 4.374 us
[     10174] [ INFO]   -- mean    : 5.63605 us
[     10174] [ INFO]   -- max     : 7.28 us
[     10174] [ INFO]   -- std. dev: 0.91291
```

Notes:
- PXIe-8880
- Standard RT kernel (not no_hz)
- C API
- Background CPU/disk load

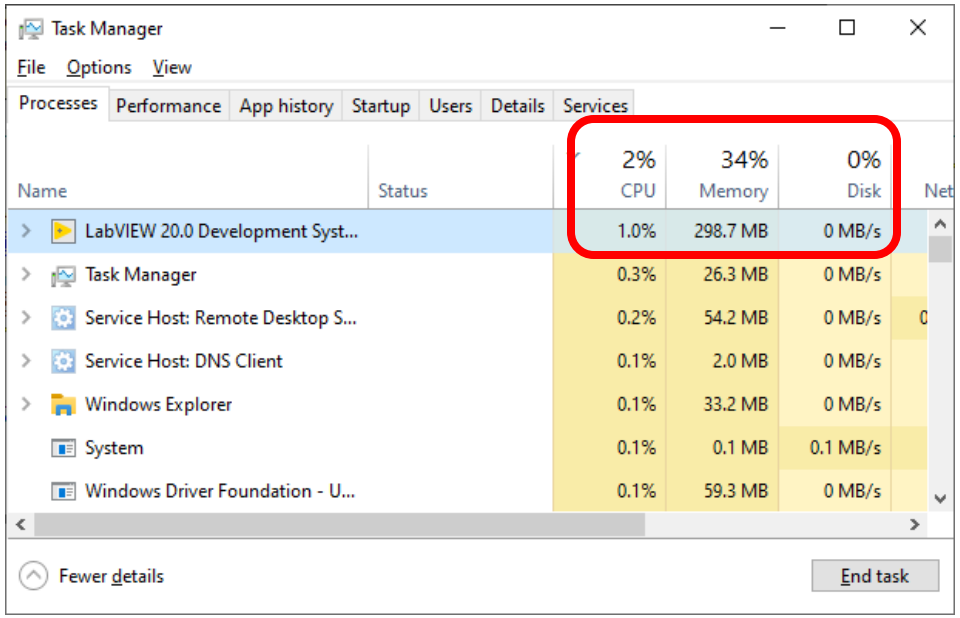
RDMA Latency Benchmarking

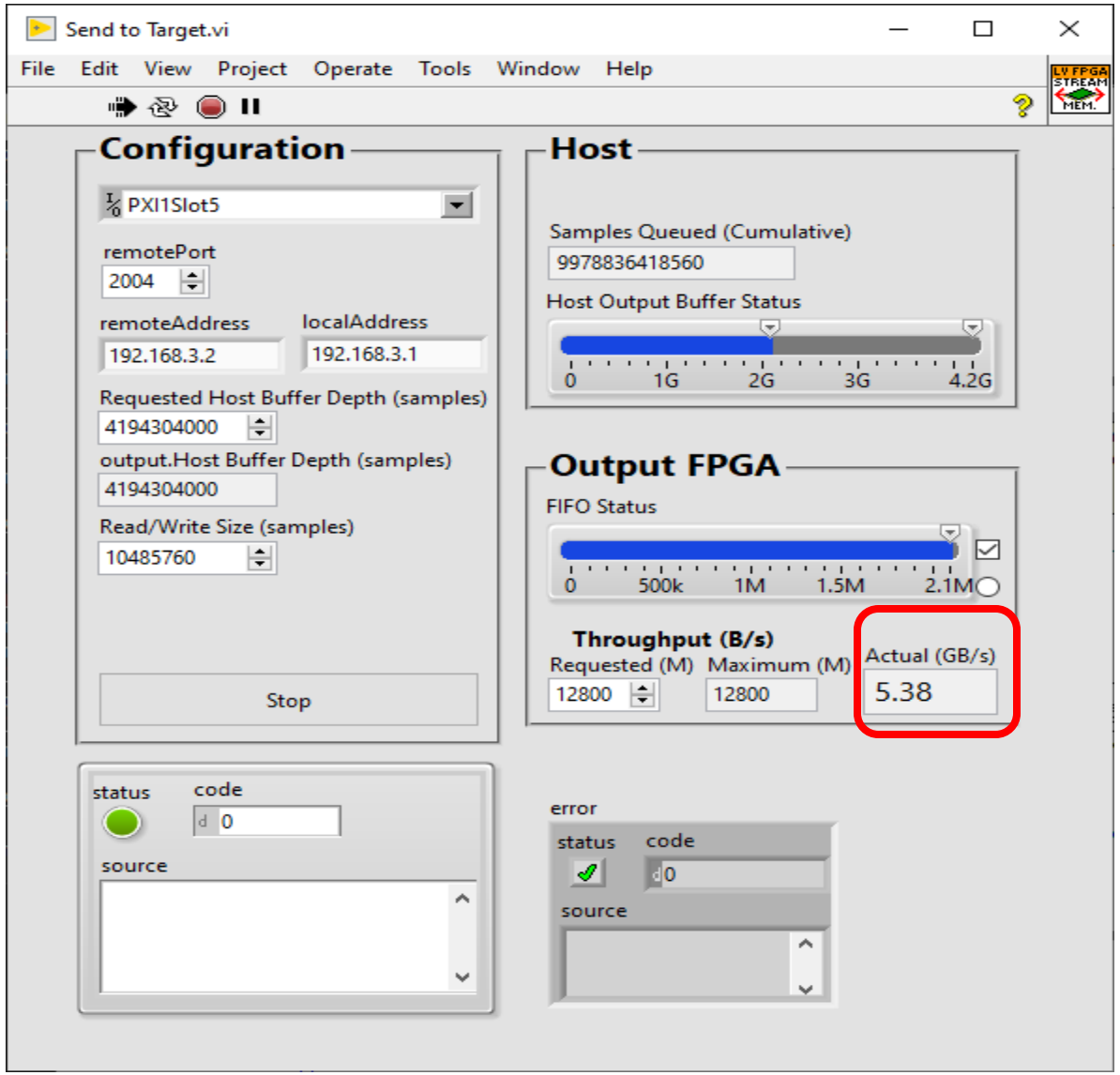
- Intel published Linux benchmarks show 4-6us for small messages on 100GbE link
- Benchmarked using LabVIEW (Mellanox 50GbE)



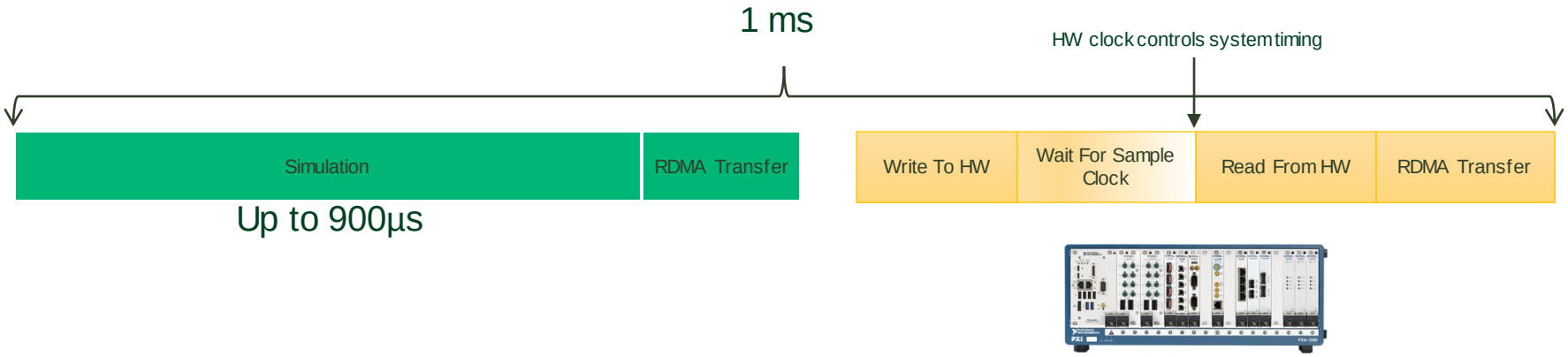
Zero-copy Transfers to NI devices

Saturating 50GbE link and sending to FlexRIO



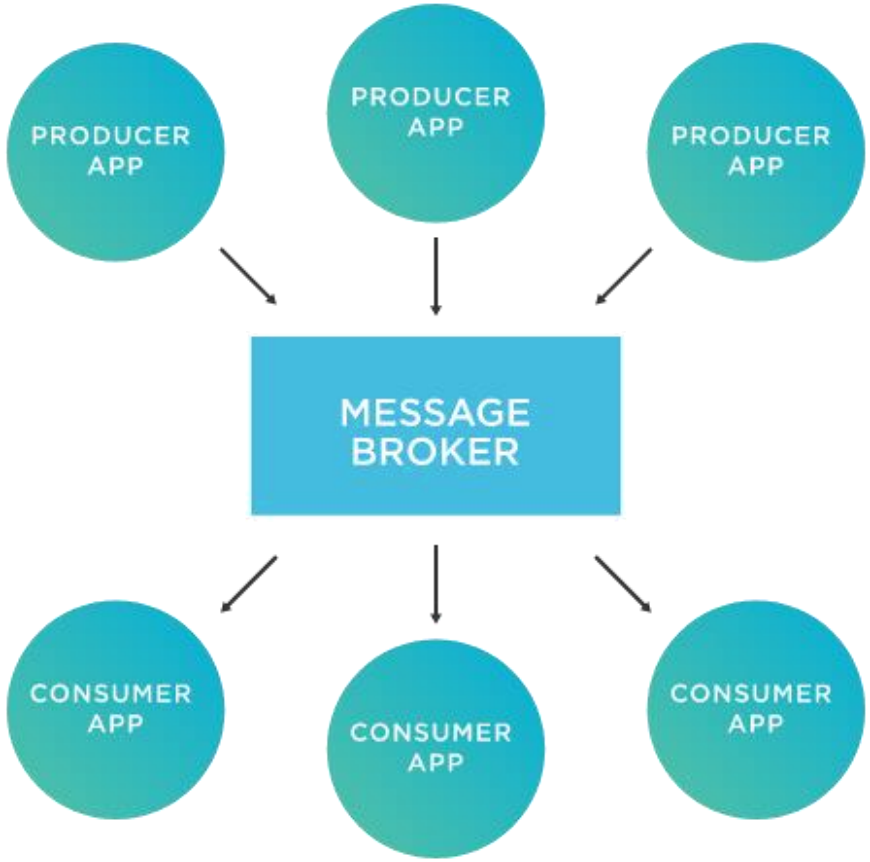


Data Transfer Block Diagram

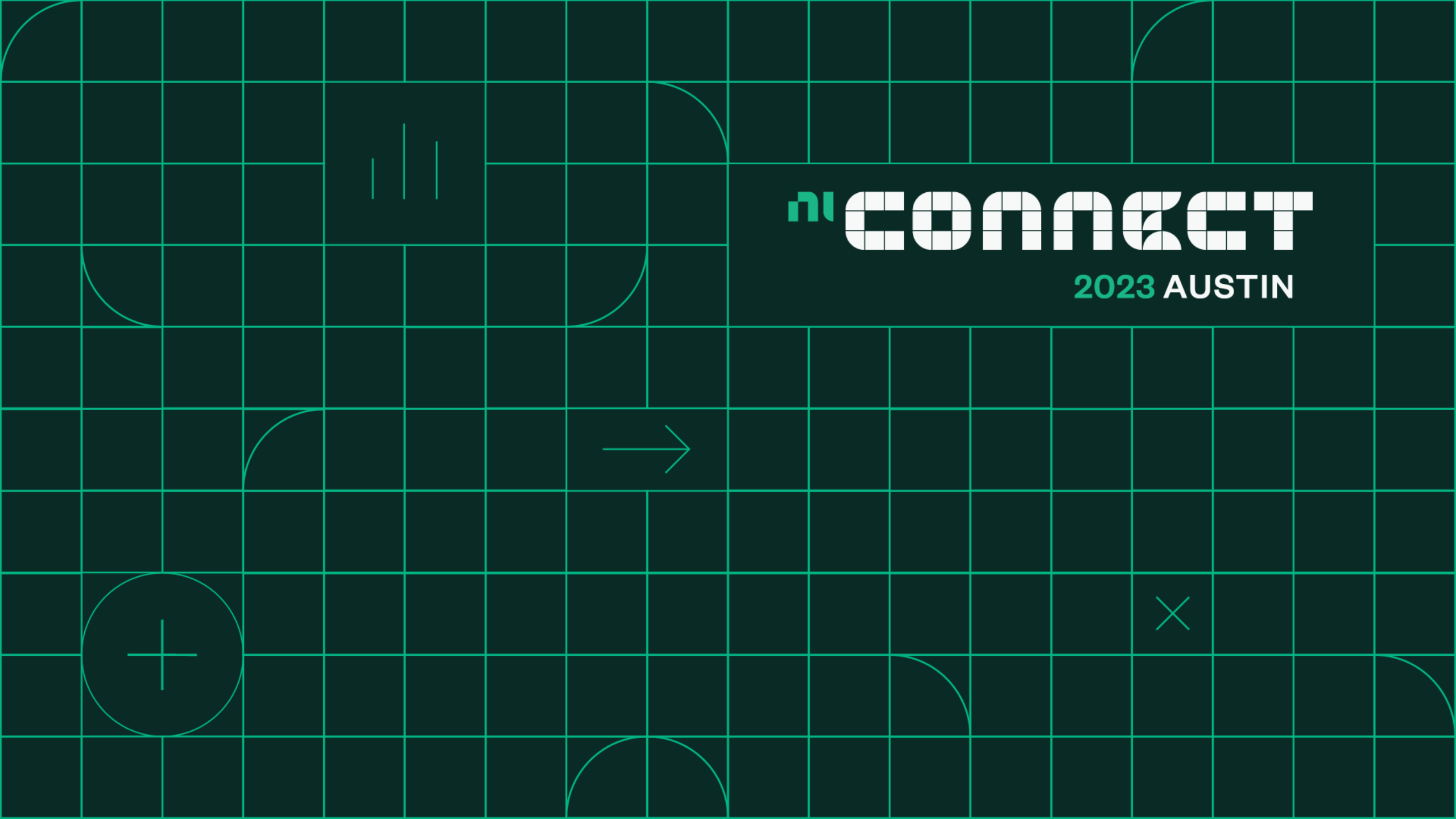


Publish Subscribe Protocols

- MQTT
- DDS
- NI Shared Variables
- OPC UA
- RabbitMQ
- And Many, Many More...



Rocket Testing: A Case Study in Distributed Control Architectures Meeting Room 19A 11:45 - 12:45 on Wednesday, May 24


CONNECT
2023 AUSTIN