Covering the Full Radar Test Spectrum

From Digital to Analog and Component to Systems

Haydn Nelson Business Development Manager

Pang Vadysirisack Field Applications Engineer



Phases of Radar Design Test & Evaluation

Modeling & Simulation Integration Lab Open Air Range Operational Mission Digitally Simulated System Digital & RF Hardware **Controlled Engagement** Active Engagement in the Loop Testing Scenarios (ll $\widehat{\mathcal{A}}$ ក្ពុំ (nn) ^tXt FD

Covering the Full Radar Test Spectrum

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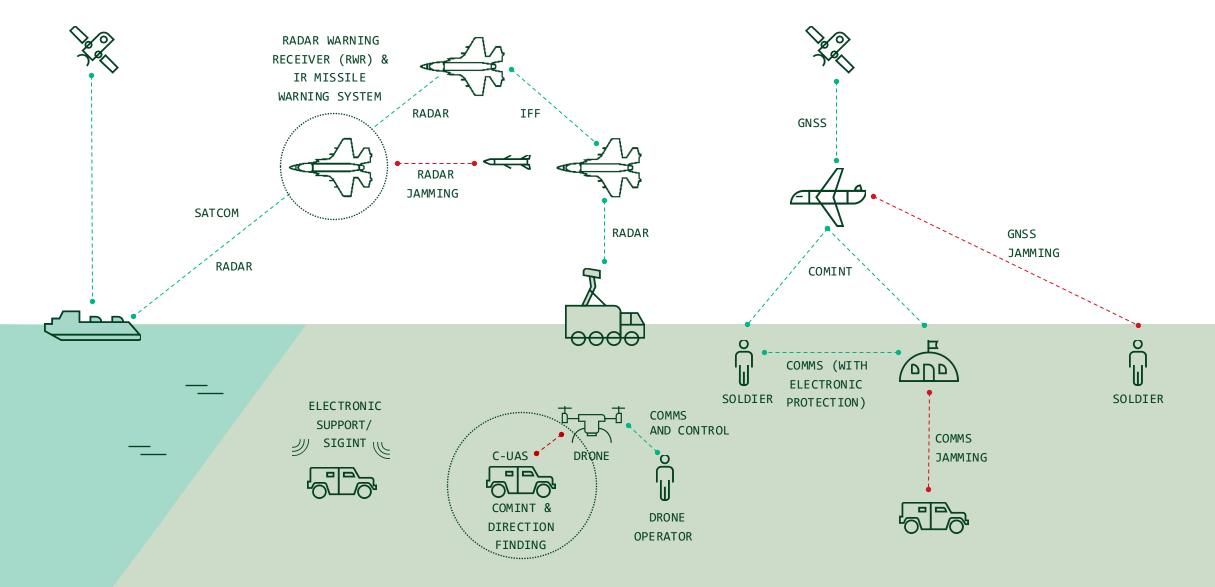
From Digital to Analog and Component to Systems

Haydn Nelson Business Development Manager

Pang Vadysirisack Field Applications Engineer

- Trends in Radar System Design and Test
- Radar Subsystem & Component Test Capabilities
 - Digital Radar Sub System Test
 - RF Parametric Test
- System Level Test Requirements
 - NI Radar Target Generation
 - Current deployments and new features
- NI Radar Target Generation Live Demo

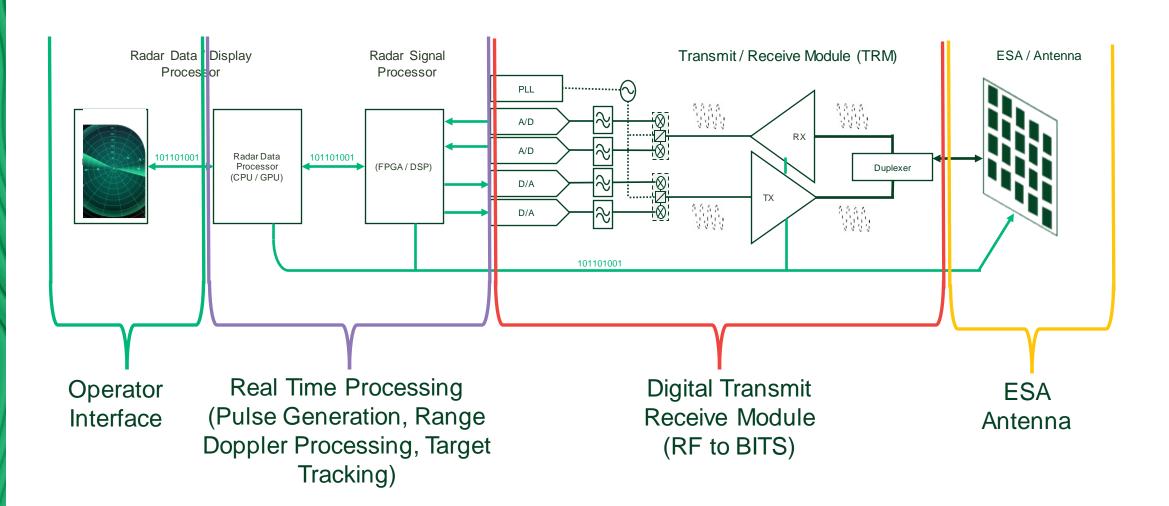
The Contested & Congested Electromagnetic Battlefield



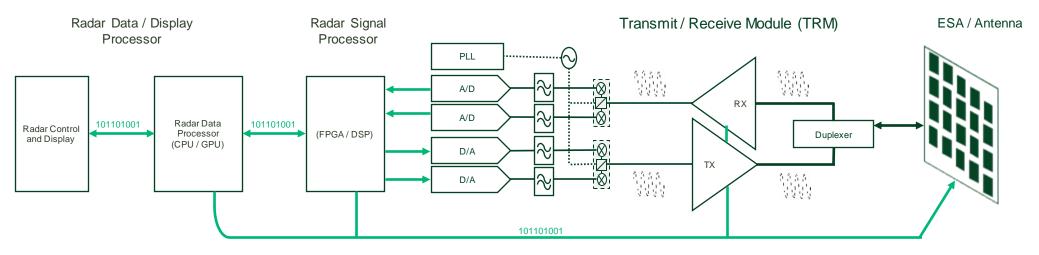
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Components of a Radar System



Components of a Radar System





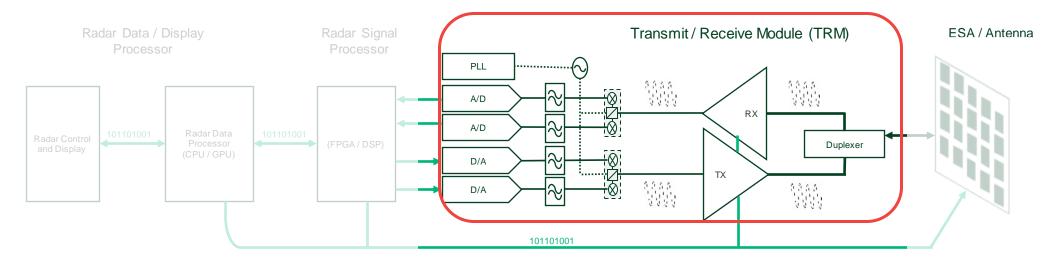
Application Test Capabilities

- System Level Hardware In the Loop Test
 - Radar Target Generation
 - RF Environment Generation
 - Multi-Channel RF Record & Playback
- <u>RF Component and Subsystem Test</u>
 - Pulse Profile, PAE, S-Parameters
- Digital Sub System Test
 - Digital Target Insertion
 - Sub-System Simulation



Digital Sub System Test / RF Parametric Test

Components of a Radar System





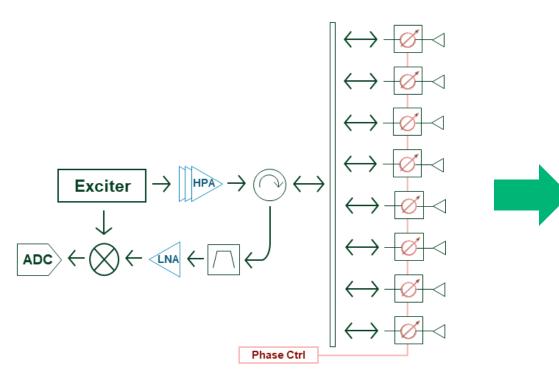
Transmit Receive module (TRM) Tests

Common Test IO Required

- RF Signal Generator
- RF Signal Analyzer
- High Speed Digital IO
- High Precision Power Supply
- Vector Network Analyzer

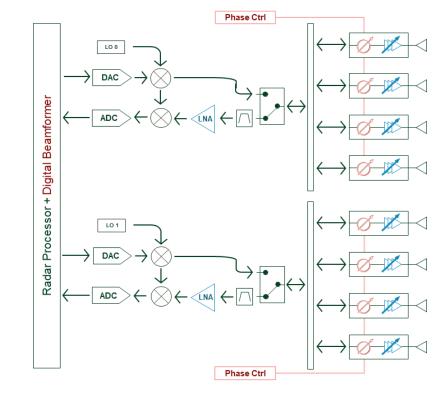
The Active Electronically Scanned Arrays (AESA)





- Single Receiver/Exciter
- Per Element Phase Control for Beam Scanning
- Number of Elements Limited by centralized Gain

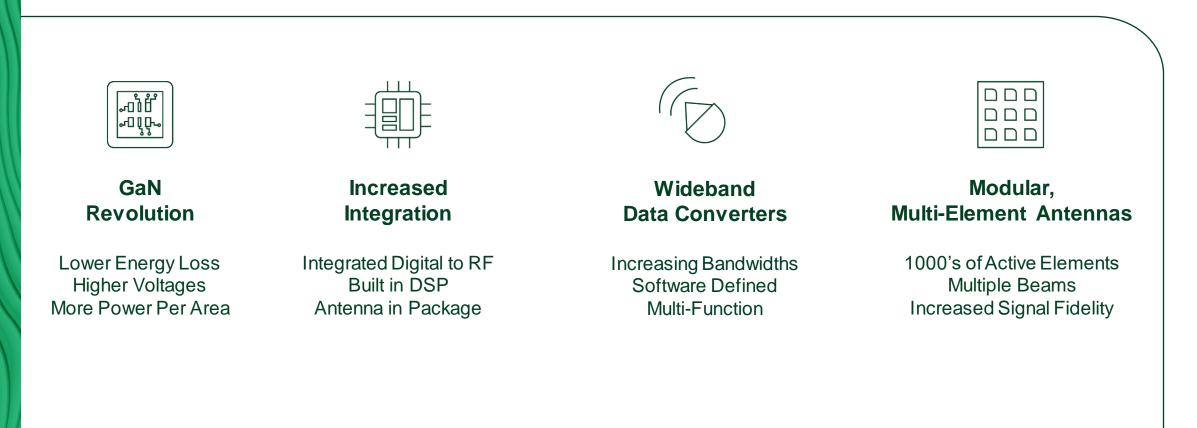
Active Electronically Scanned Array (AESA)



- Distributed Gain per Element -> Active T/R Modules
- Flexible Sub-Arrays allow for multiple beams
 - Varied frequencies and signal profiles

Technology Shifts and Application Evolution

Key technology shifts are leading to new mission capabilities along with new test challenges



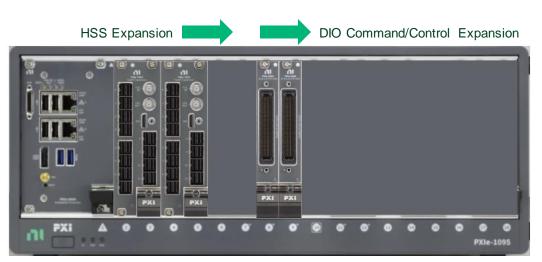
Digital AESA Digital Interfaces

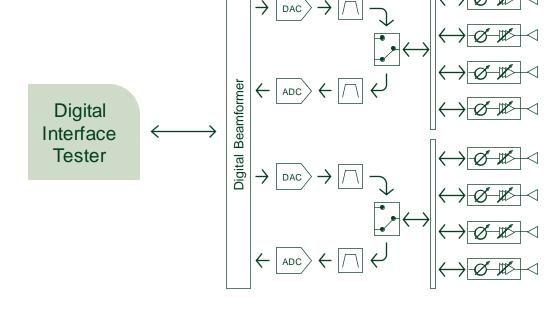
Key Test Challenge: Provide robust and abstractable mixed I/O interfaces that can scale and adapt to evolving DUT needs while easily integrating I/O such as highspeed serial interfaces with RF instrumentation in order test functionality in an optimized and synchronous manner.

The NI Approach

PXI Platform

- Expandability
- Synchronization
- High Throughput
- Customizable FPGA Functionality





2-Slot FlexRIO Coprocessor PXIe-7903

Features

- 12 MiniSAS zHD Connectors
- 28.2 Gbps Line Rate
- External Clock Input/Output
- Xilinx Virtex UltraScale+ FPGA, VU11P
- DRAM: ~25GB/s / Bank; 2 Banks of 10GB
- PCI Express Gen 3x8

Target Applications

- Real-time Spectrum Analysis
- Comms Algorithm Prototyping
- Beamforming RF Signals
- Spectral Stitching RF Instruments



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Scalable Digital Interfacing with NI FlexRIO

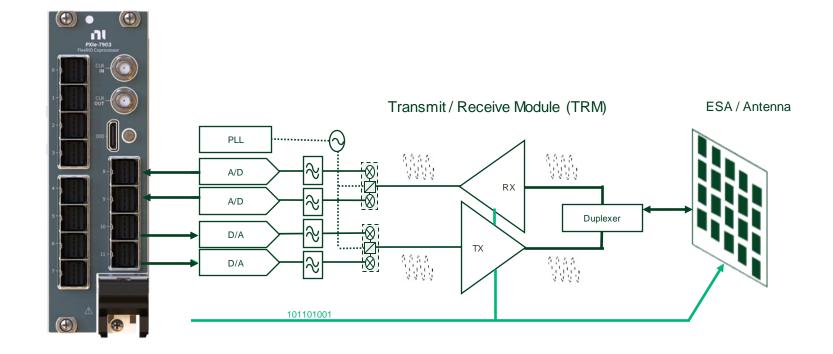


High Speed Serial Product Table Link

Product radie Link			
Specification	NI PXIe-6593	NI PXIe-6594	PXIe-7903
Line Rates	500 Mbps – 16.3 Gbps	500 Mbps – 28.2 Gbps	Up to 28.2 Gbps
Channels	8 RX/TX (GTH)	8 RX/TX (GTY)	48 MGTs (GTYs)
User Programmable FPGA	Kintex Ultrascale (KU040 or KU060)	Kintex Ultrascale + (KU15P)	Virtex Ultrascale+ (VU11P)
DRAM	4 GB	8 GB	16 GB
Host Streaming Bandwidth	7 GB/s	7 GB/s	7 GB/s
Connector	QSFP28	QSFP28	12x miniSAS zHD
Cabling Options	Copper or Optical	Copper or Optical	Copper or Optical (TBD)
Aux DIO	8 GPIO, 4 GTH (RX/TX)	8 GPIO, 4 GTY (RX/TX)	12 GPIO (MiniHDMI)
Relevant Protocols	JESD204B, 10/40 GbE, Aurora, Custom	JESD204B/C, 10/25/40/100 GbE, Aurora, Custom	100 GbE, Aurora 64b66b, Custom

Planned 2023

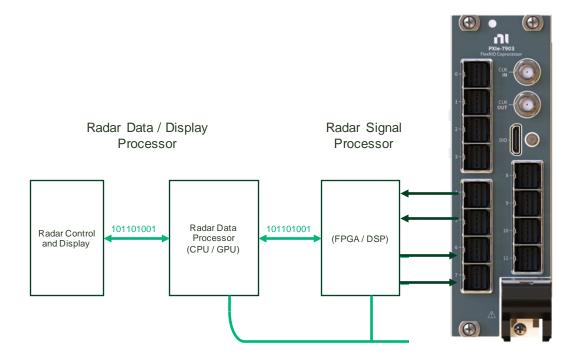
Components of a Radar System



Digital TRM Test

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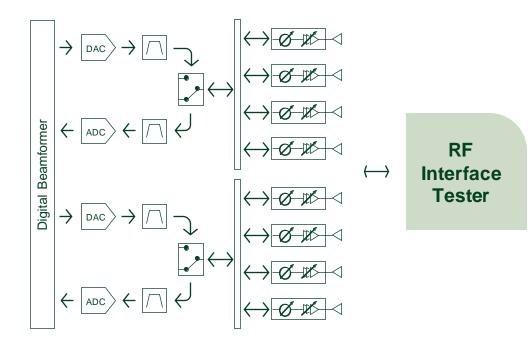
Components of a Radar System



Radar Digital Processor Test

Digital AESA - RF Interfacing & Measurements

Key Test Challenge: Provide robust and abstractable mixed I/O interfaces that can scale and adapt to evolving DUT needs while easily integrating I/O such as highspeed serial interfaces with RF instrumentation in order test functionality in an optimized and synchronous manner.



Common Technical Challenges

High Number of RF Channels and Need for Decreased Test Times Time/Phase Synchronization Between RF Channels Synchronization with Digital Links Frequency Coverage for High BW ADC/DAC's

Third-generation VST Provides Extended Frequency and Bandwidth Coverage

PXIe-5842 26.5 GHz VST

Parameter	Instrument Capability	
Frequency Range	50 MHz – 23 GHz (Q4 2022) 50 MHz – 26.5 GHz (H2 2023)*	
Bandwidth	Up to 2 GHz (Q4 2022) Up to 4GHz (TBD)	
RF IN / OUT Flatness (2GHz)	$< \pm 0.45$ dB typ. / $< \pm 0.4$ dB typ.	
RF IN / OUT Absolute Accuracy	< ±0.4 dB typ.	
Max Unleveled Tx Power	+20 dBm typ. (<18 GHz)	
802.11be, 320 MHz EVM	Better than -49 dB	

*Upgrade from 23 GHz HW to 26.5 GHz HW requires a paid upgrade service



PXIe-5842 VST

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Vector Signal Transceiver

Integrated, instrument grade VSA and VSG with up to 1 GHz of instantaneous bandwidth

Support Onboard and External LO's for phase noise optimization

Multi-Channel Synchronization (< 1nsec) and Phase Coherent LOs

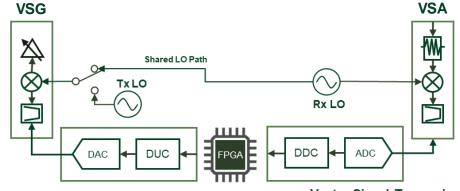
Easy SW and HW integration with mixed I/O and PXI

Optimized for automated characterization and production

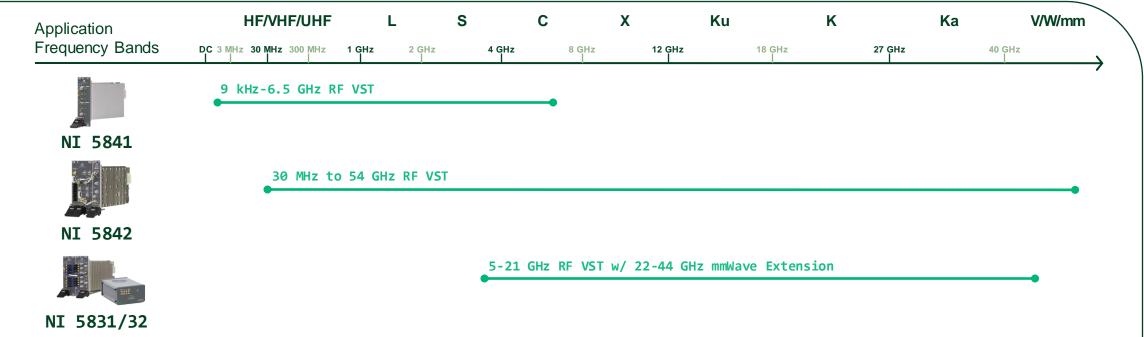
Customizable firmware for deploying application IP or test speed optimization

- Onboard, open FPGA
- Full rate peer to peer streaming to FPGA coprocessors

Vector Signal Transceiver Product Family



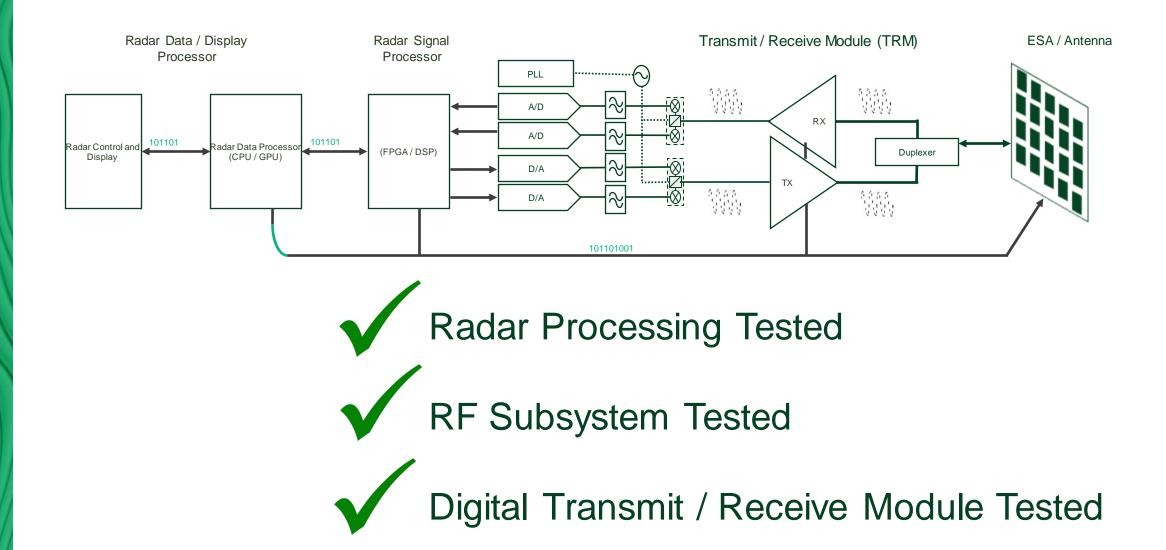
Vector Signal Transceiver



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System Level Test ?



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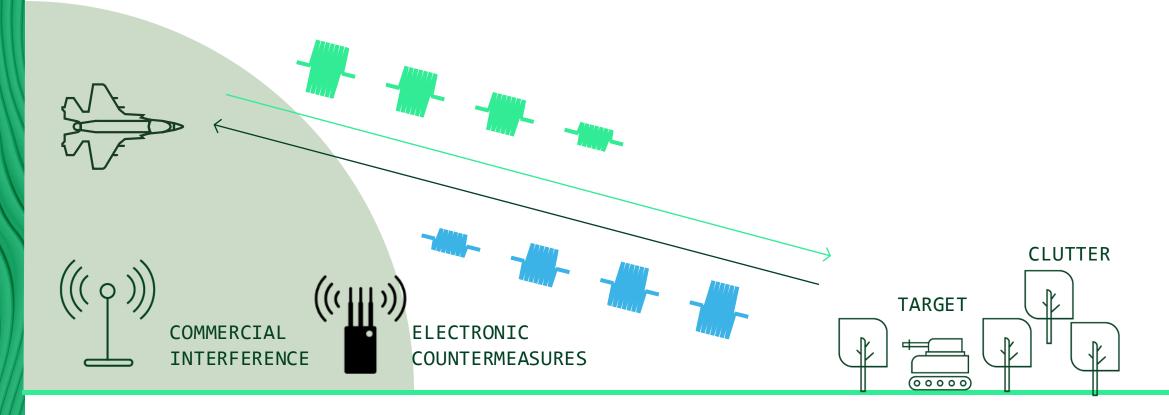
System Level Test Requirements

Radar Target Generation

What is a Radar Target Generator?

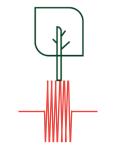
Problem Statement

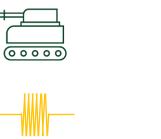
Today's military radars feature complex modes of operation, demanding more thorough testing during design to manage schedule risk and reduce probability of failure.



What is a Radar Target Generator?



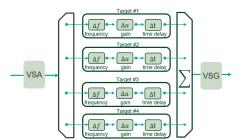


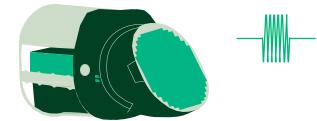




Your Radar

What is a Radar Target Generator?





Your Radar



Traditional Approaches to Radar Test

Delay Lines

Strengths

- · Capable of Very Low Latencies
- Cost Effective



- Robust Solutions
- Easy to Purchase & Use

Weaknesses

- Very Limited Flexibility
- · Cannot Simulate "Real World" Environmental Conditions
 - No testing of clutter, interference, ECCM techniques



COTS Target Generation

Strengths

- Hardware Tailored to Application
- Minimal NRE Required
 - Vendor has domain expertise

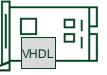
Weaknesses

- Very Expensive
- Less Flexibility
- Capabilities Slow to Evolve and Update
 - Reliant on Vendor to Implement New Modes

Test & Measurement Solutions

COTS FPGA DIY

Strengths



- Tailorable for Unique Requirements
- Low Capital Cost

· Capable of Low Latencies

Weaknesses

- Not Often "Test" Equipment
- Difficult to Maintain Variable Robustness
- High NRE Cost
 - · Require significant software/firmware development



Weaknesses

Great Dynamic Range

- · Vendor-Defined Functionality
- Higher Latency

Strengths

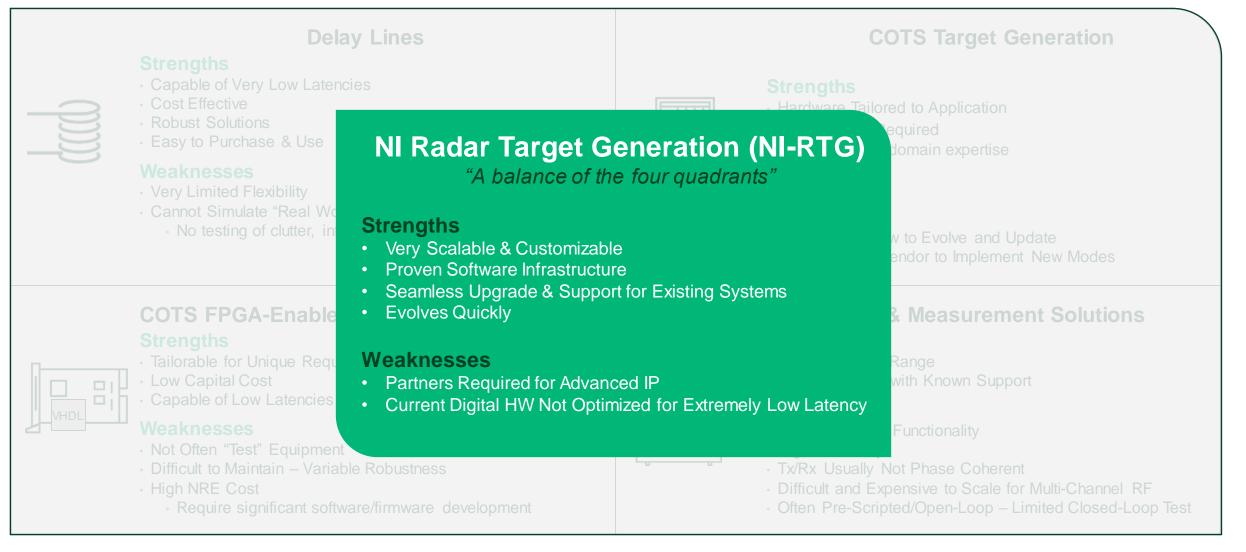
Tx/Rx Usually Not Phase Coherent

Well Calibrated with Known Support

- · Difficult and Expensive to Scale for Multi-Channel RF
- \cdot Often Pre-Scripted/Open-Loop Limited Closed-Loop Test



Traditional Approaches to Radar Test

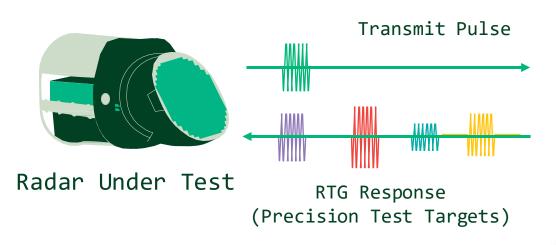


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Radar Target Generation Driver

Features

- Up to 4 Real-Time Test Targets
- Target Parameter Control *
 - Range(Time Delay): 150m 50,000km
 - Velocity(Doppler): +/- 2MHz
 - Path Loss (Attenuation)
- Built In Precision System Self Calibration
 - De-embeds cable loss and time delay
- Frequency Range: 10MHz 21Ghz
- Bandwidth: 1GHz
- Remote Procedure Call over Ethernet Protocol
- Licensed Alternative FPGA Image







Host Control App and API

Onboard IP

Target #1 Δa

gain

Target #2

 Δa

gain

Target #3

 Δa

αain

 Δa

Target #4

time dela

Δt

time delay

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time delay

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VSA

NI Radar Target Generation

Version 1.0 Features

- Up to 4 real-time test targets
- Target parameter control
 - Range (Time Delay): 150m 50,000km
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Investments in NI-RTG Capabilities

Version 1.0 Features

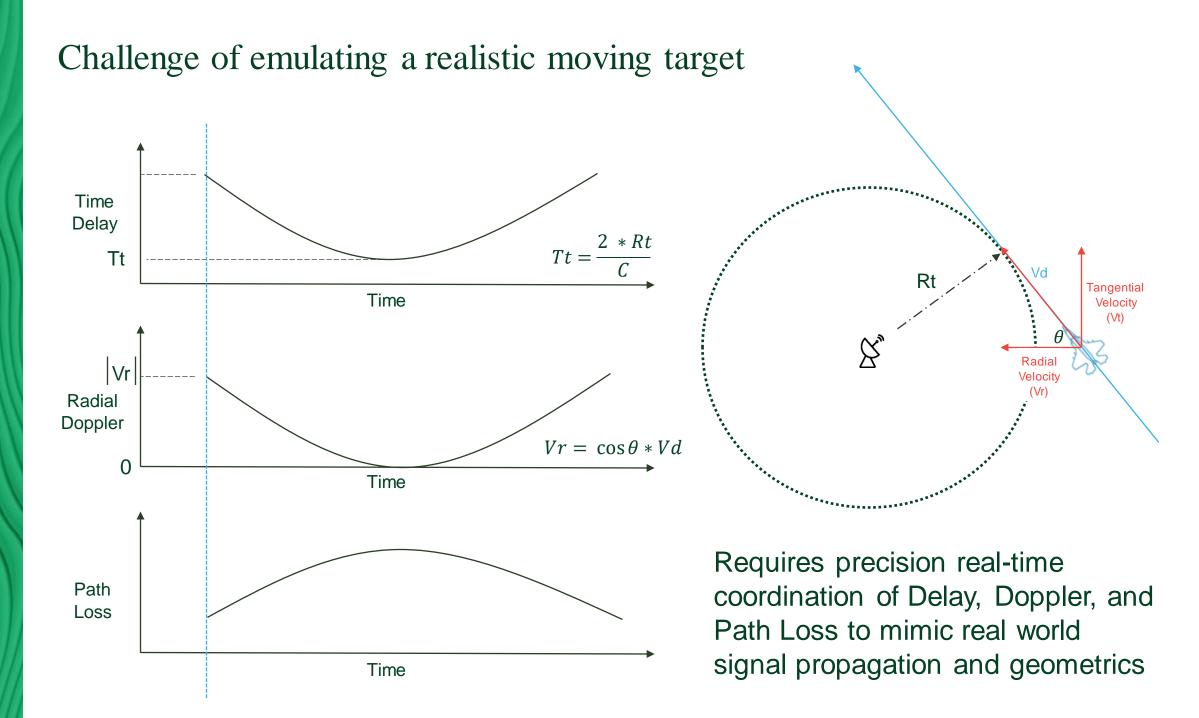
- Up to 4 real-time test targets
- Target parameter control
 - Range (Time Delay): 150m 50,000km
 - Velocity (Doppler): +/- 2 MHz
 - Path Loss (Attenuation)
- Built In precision system self calibration
 - De-embeds cable loss and time delay
- Frequency Range: 10 MHz 21 GHz
- Bandwidth: 1 GHz
- Remote Procedure Call over Ethernet Protocol
- Licensed alternative FPGA image

Version 1.2 Features

- All Version 1.0 features
- Interface to real-time simulator
 - Parameter streaming
- Complex pre-generated target scenario generation
 - Up to 10 million targets
 - Hardware or software timed
- Low latency pulse repeater
- FPGA co-processor harness
 - Ability to add customer IP and effects alongside RTG

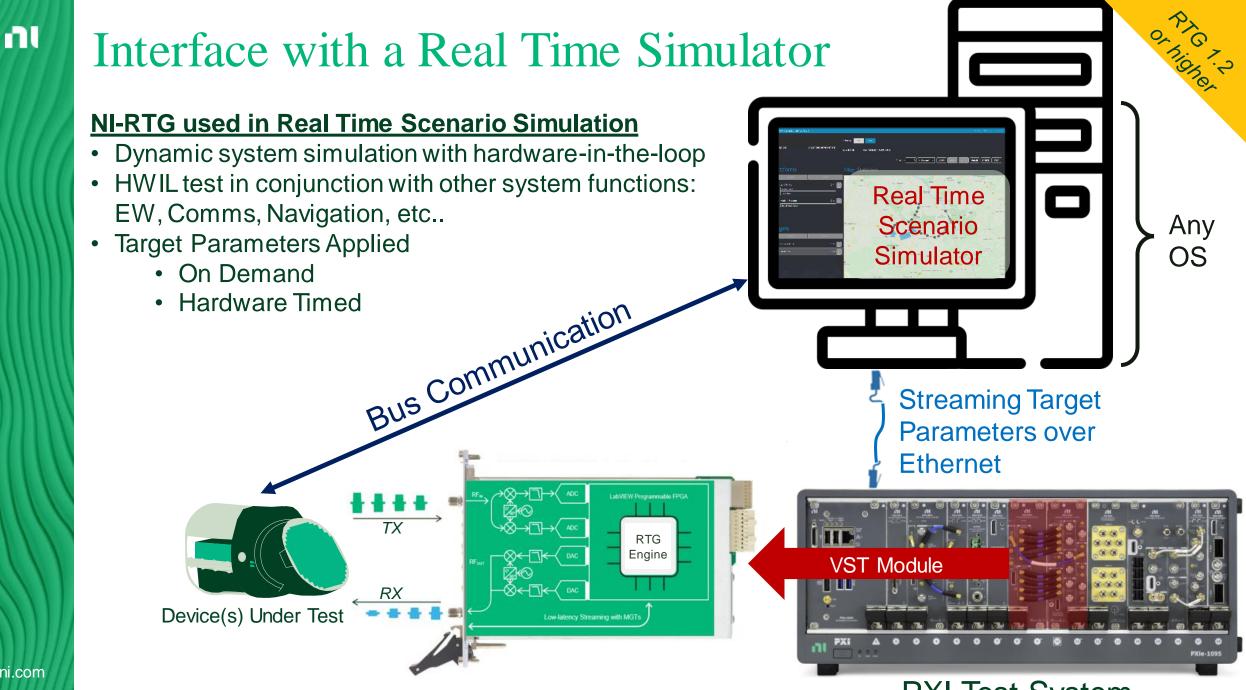
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Radar Target Generation Dynamic Scenario Generation



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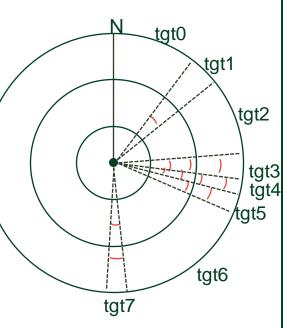
PXI Test System

Pre-Generated Target Scenarios "List Mode"

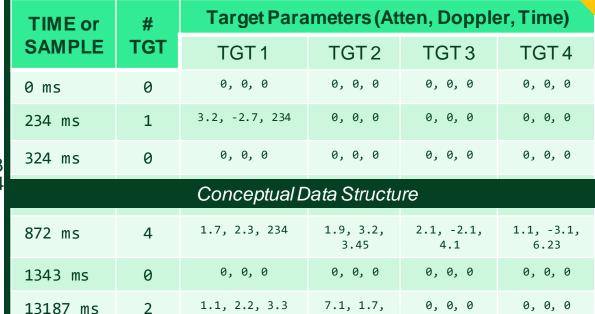
- Over 10 Million Targets
- Deterministic Timing
- Digital Triggered
- Software Triggered
- Time Reference Trig
- Synchronize to Radar
- File Driven

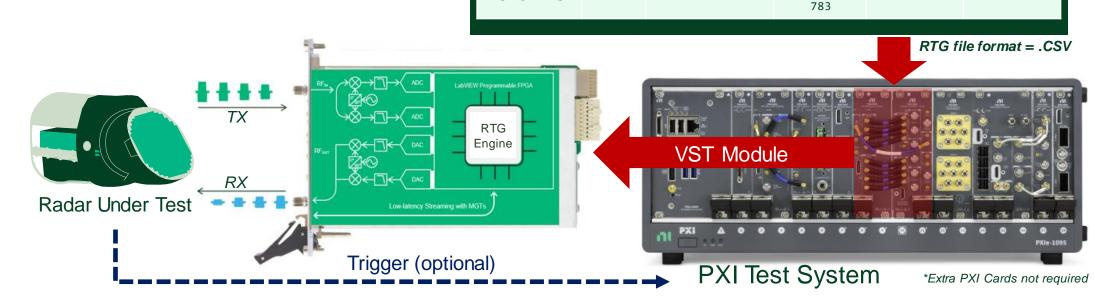
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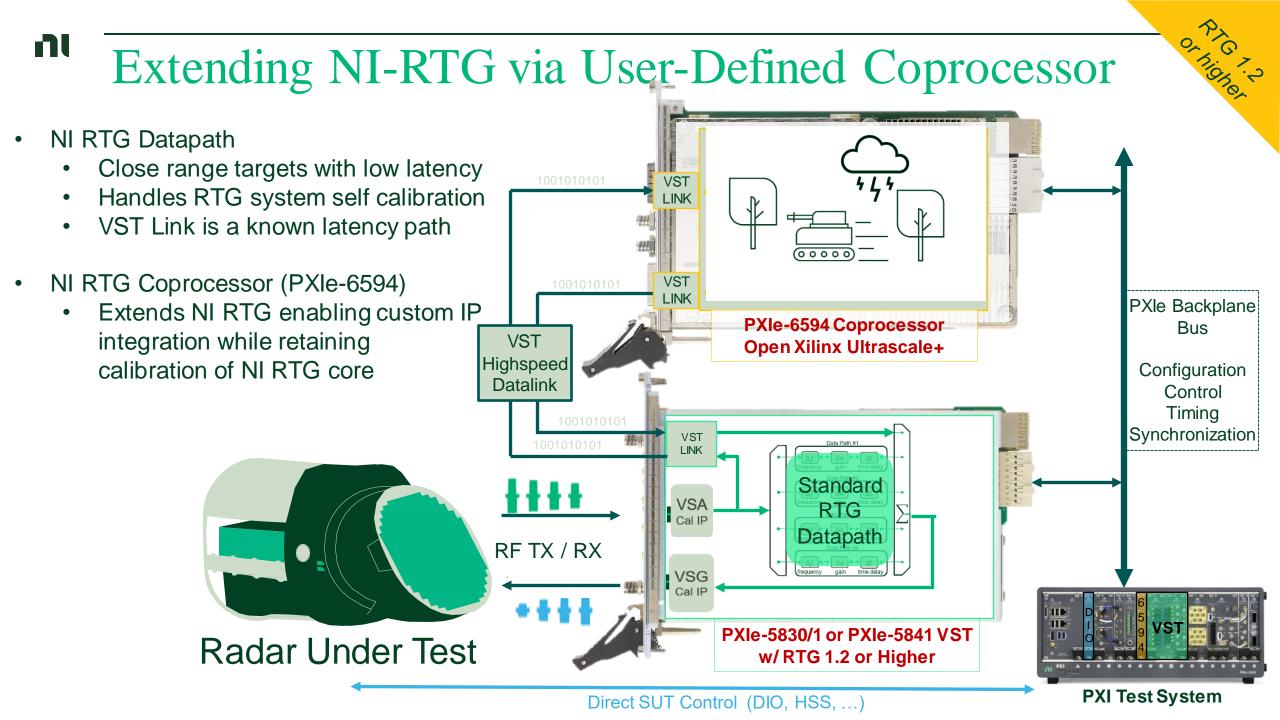
- Four Targets per Entry
- 15KHz Update Rate



Pre-Computed Target Parameter List







Further Investments in NI-RTG Capabilities

Enhanced Radar Test Capabilities

- High fidelity EM/RF environment simulation
- Classified & unclassified threat and terrain databases
- Customized target profiles
- Dynamic scenario simulation
- Environment parameters
 - Noise & clutter
 - Realistic flight scenarios
 - Atmospheric effects
- Others per customer feedback

NI Radar Partners



Explore All NI Radar Test Capabilities in the Expo Hall

2023 AUSTIN

Radar Target Generation Demo

