

Characterizing Digital T/R Modules and AESA Systems

Tim Sileo

Principal Applications Engineer



• The Digital AESA

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- Technology and Market Trends
- Next Gen Digital AESAs
- Defining the Digital + RF Test Challenge
- The NI Solution Digital + RF Test
 - Scalable High Speed Digital Interfacing
 - Wideband RF Stimulus and Response
 - A system level, NI solution
- Conclusion, Demo, and Q&A

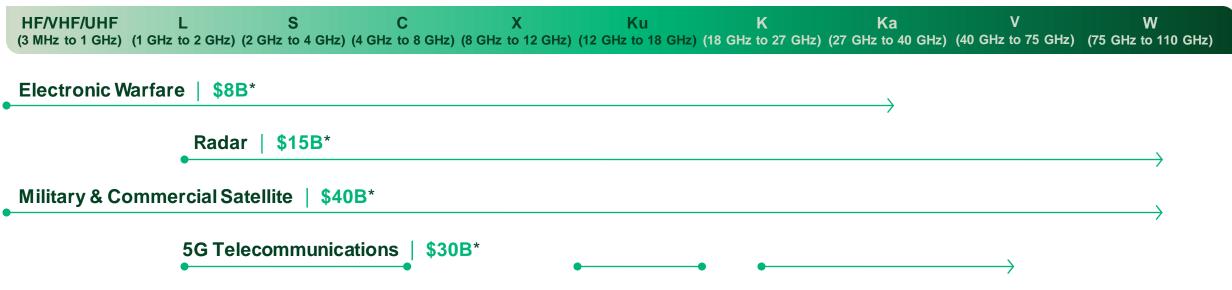


The Digital AESA

Technology and Market Trends

Market Trends and Momentum

*Forecasted In 2020



Example Market Drivers

Continued investment in 5th generation and exploration of 6th generation fighters

• Multi-functional RF Systems (Radar + EW + Communications)

High resolution SAR payloads for terrestrial imaging and monitoring

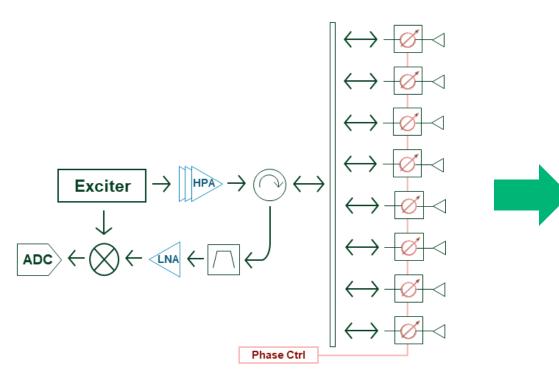
High throughput communications and convergence of Satcom and 5G

Hypersonic Intelligent weapons and next generation UAVs

Cognitive Electronic Warfare systems

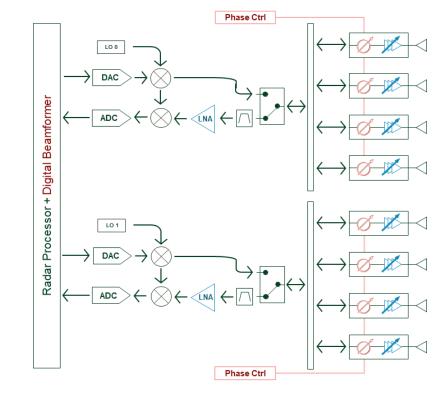
The Active Electronically Scanned Arrays (AESA)





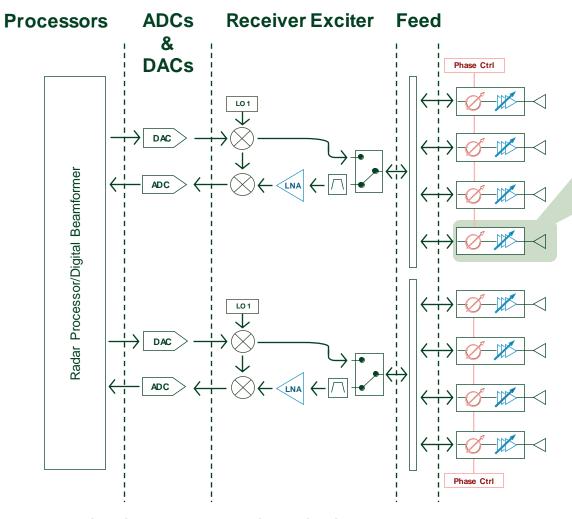
- Single Receiver/Exciter
- Per Element Phase Control for Beam Scanning
- Number of Elements Limited by centralized Gain

Active Electronically Scanned Array (AESA)



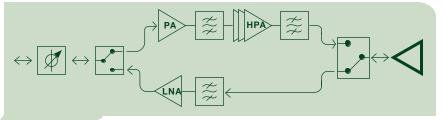
- Distributed Gain per Element -> Active T/R Modules
- Flexible Sub-Arrays allow for multiple beams
 - Varied frequencies and signal profiles

Testing AESA Components and Modules



Historical Test Boundaries Maintained – RF components and modules, Low frequency Data Converters, and Digital Processors

RF Transmit Receive (T/R) Module



Testing of AESA components and modules largely consists of traditional RF parametric measurements due to distributed architecture, including:

Common:

• S-Parameters

T/R Modules

- Relative Phase (Phase Shifter)
- Noise Figure
- Compression

Receiver/Exciter

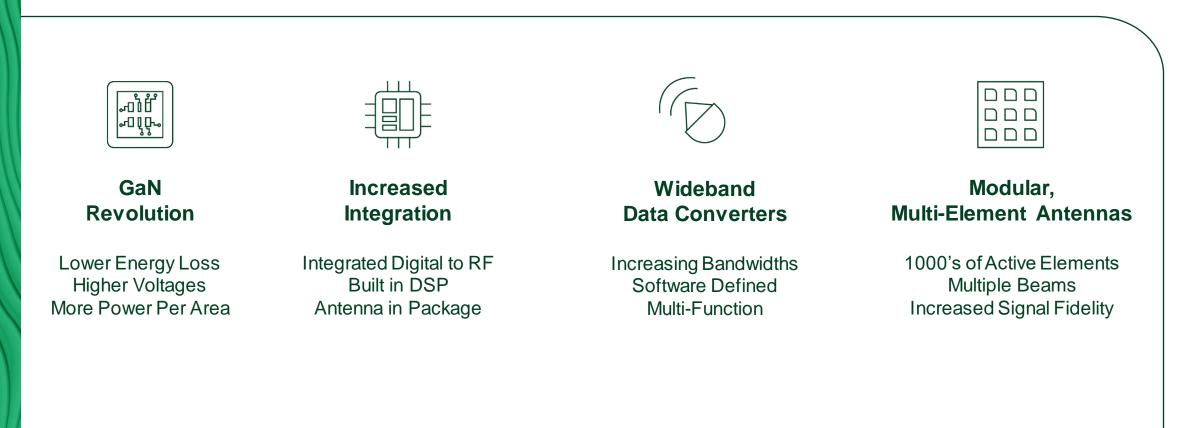
- Conversion Gain
- Phase Noise

ADCs & DACs

- SNR / SFDR
- Group Delay

Technology Shifts and Application Evolution

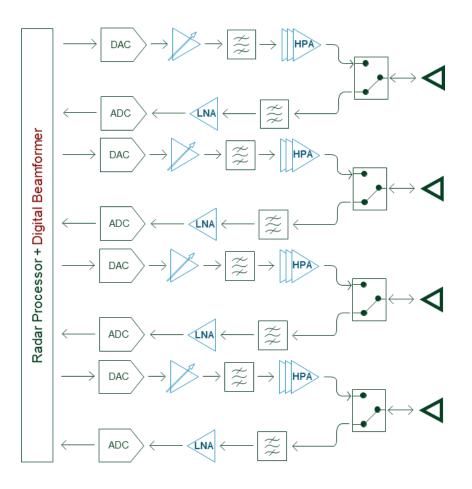
Key technology shifts are leading to new mission capabilities along with new test challenges



Looking Forward | The Next Generation Digital AESA

A True "RF to Bits" Architecture

- Wideband RF Data Converters allow for direct synthesis and acquisition of signals at mission frequencies
 - Digital and Analog BW rapidly scaling from low frequency to X-band without needing an up- or downconverter
- Simplified RF frontends and antenna integration allows for increased density and capability, per antenna element
- Robust Channel Synchronization and Coherency
- True Digital Beamforming and Multi-Frequency Functionality
- Software Defined Multi-Mode and Multi-Functional Operation
- Integrated High-Speed Data Transfer (i.e JESD204C, 100Gb Ethernet)



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The Digital AESA

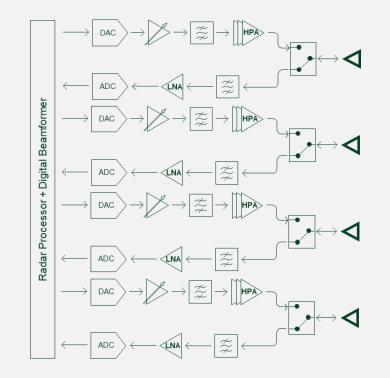
Defining the RF + Digital Test Challenge

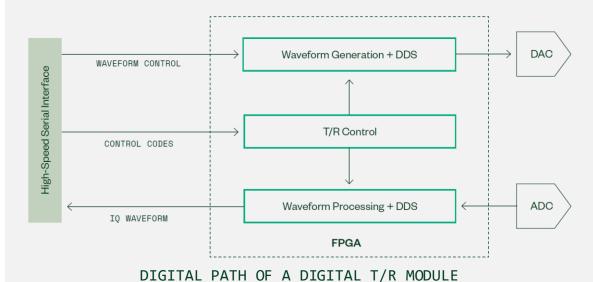
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Fully Digital T/R Modules

Common Test Challenges

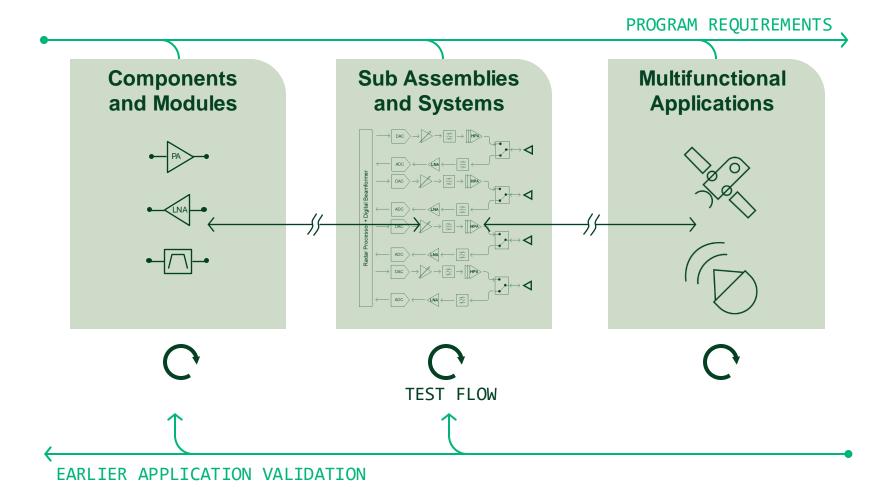
Increased sampling rates and real-time processing Multichannel synchronization and alignment Calibration and de-embedding of DUT characteristics Changes in measurement scope Diversity of operational and functional test scenarios RF connectivity limitations





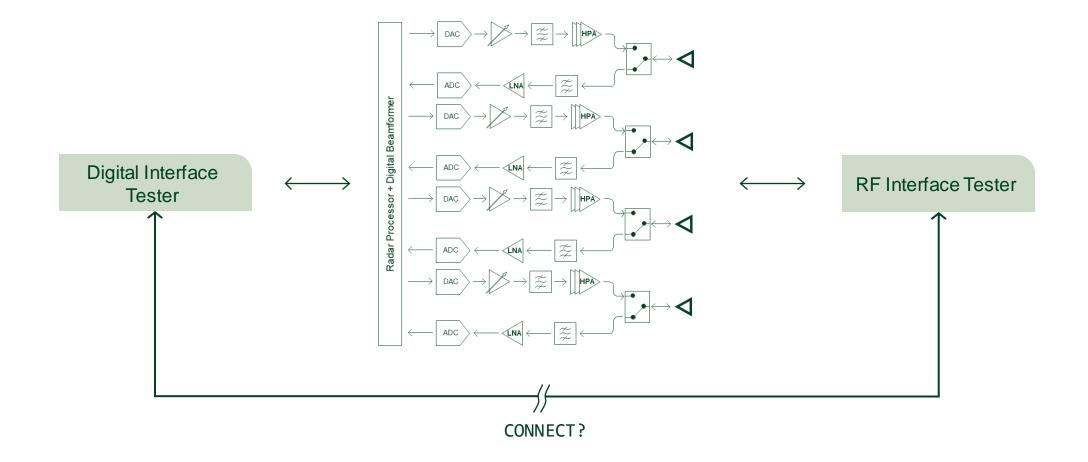
Connecting Parametric Test with System Validation

Key Test Challenge: Enable application specific validation earlier in the design and integration cycles to catch flaws sooner and reduce time to market



Digital Integration and the Need for Mixed I/O Test

Key Test Challenge: Provide robust and abstractable mixed I/O interfaces that can scale and adapt to evolving DUT needs while easily integrating I/O such as highspeed serial interfaces with RF instrumentation in order test functionality in an optimized and synchronous manner.





The NI Solution for RF + Digital Test

Scalable High Speed Digital Interfacing

Digital AESA - Digital Interfaces

Key Test Challenge: Provide robust and abstractable mixed I/O interfaces that can scale and adapt to evolving DUT needs while easily integrating I/O such as highspeed serial interfaces with RF instrumentation in order test functionality in an optimized and synchronous manner.

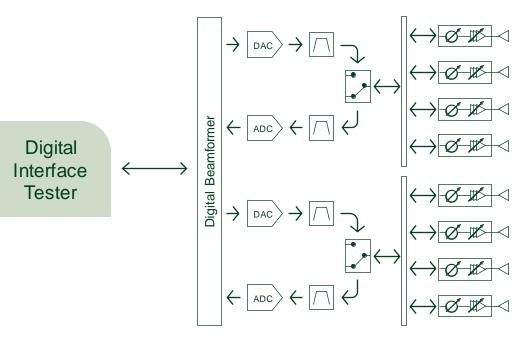
Common Technical Challenges

High Speed Serial (HSS) Interfacing Pushing Throughput Limits

Number of Links based on Array Size

Custom/Proprietary Protocols for Digital Interface

Command and Control DIO Synchronization (Embedded in HSS or Separate DIO)



2-Slot FlexRIO Coprocessor PXIe-7903

Features

- 12 MiniSAS zHD Connectors
- 28.2 Gbps Line Rate, 48 TX/RX
- External Clock Input/Output
- Xilinx Virtex UltraScale+ FPGA, VU11P
- DRAM: ~25GB/s / Bank; 2 Banks of 10GB
- PCI Express Gen 3x8

Target Applications

- Real-time Spectrum Analysis
- Comms Algorithm Prototyping
- Beamforming RF Signals
- Spectral Stitching RF Instruments



Scalable Digital Interfacing with NI FlexRIO



High Speed Serial Product Table Link

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Product Table Link			
Specification	NI PXIe-6593	NI PXIe-6594	PXIe-7903
Line Rates	500 Mbps – 16.3 Gbps	500 Mbps – 28.2 Gbps	Up to 28.2 Gbps
Channels	8 RX/TX (GTH)	8 RX/TX (GTY)	48 MGTs (GTYs)
User Programmable FPGA	Kintex Ultrascale (KU040 or KU060)	Kintex Ultrascale + (KU15P)	Virtex Ultrascale+ (VU11P)
DRAM	4 GB	8 GB	16 GB
Host Streaming Bandwidth	7 GB/s	7 GB/s	7 GB/s
Connector	QSFP28	QSFP28	12x miniSAS zHD
Cabling Options	Copper or Optical	Copper or Optical	Copper or Optical (TBD)
Aux DIO	8 GPIO, 4 GTH (RX/TX)	8 GPIO, 4 GTY (RX/TX)	12 GPIO (MiniHDMI)
Relevant Protocols	JESD204B, 10/40 GbE, Aurora, Custom	JESD204B/C, 10/25/40/100 GbE, Aurora, Custom	100 GbE, Aurora 64b66b

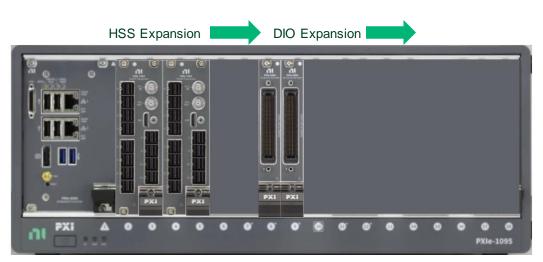
Digital AESA Digital Interfaces

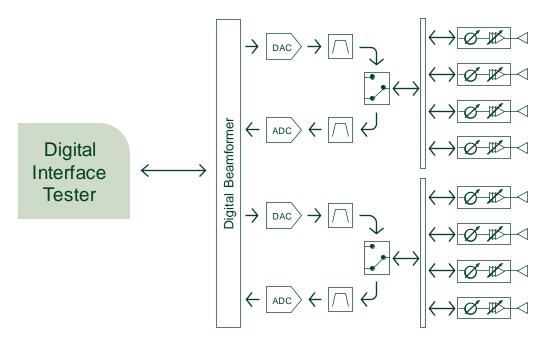
Key Test Challenge: Provide robust and abstractable mixed I/O interfaces that can scale and adapt to evolving DUT needs while easily integrating I/O such as highspeed serial interfaces with RF instrumentation in order test functionality in an optimized and synchronous manner.

The NI Approach

PXI Platform

- Expandability
- Synchronization
- High Throughput
- Customizable FPGA Functionality





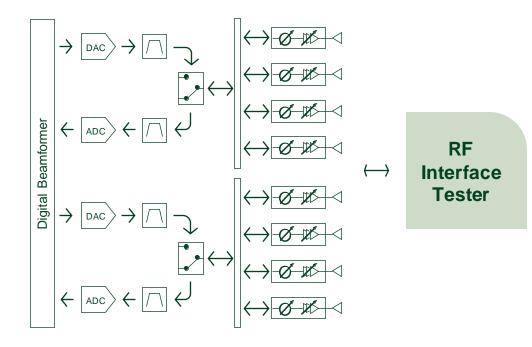


The NI Solution for RF + Digital Test

Wideband RF Stimulus and Response

Digital AESA - RF Interfacing & Measurements

Key Test Challenge: Provide robust and abstractable mixed I/O interfaces that can scale and adapt to evolving DUT needs while easily integrating I/O such as highspeed serial interfaces with RF instrumentation in order test functionality in an optimized and synchronous manner.



Common Technical Challenges

High Number of RF Channels and Need for Decreased Test Times Time/Phase Synchronization Between RF Channels Synchronization with Digital Links Frequency Coverage for High BW ADC/DAC's

Vector Signal Transceiver

Integrated, instrument grade VSA and VSG with up to 2 GHz of instantaneous bandwidth

Support Onboard and External LO's for phase noise optimization

Multi-Channel Synchronization (< 1nsec) and Phase Coherent LOs

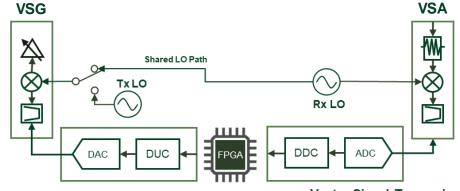
Easy SW and HW integration with mixed I/O and PXI

Optimized for automated characterization and production

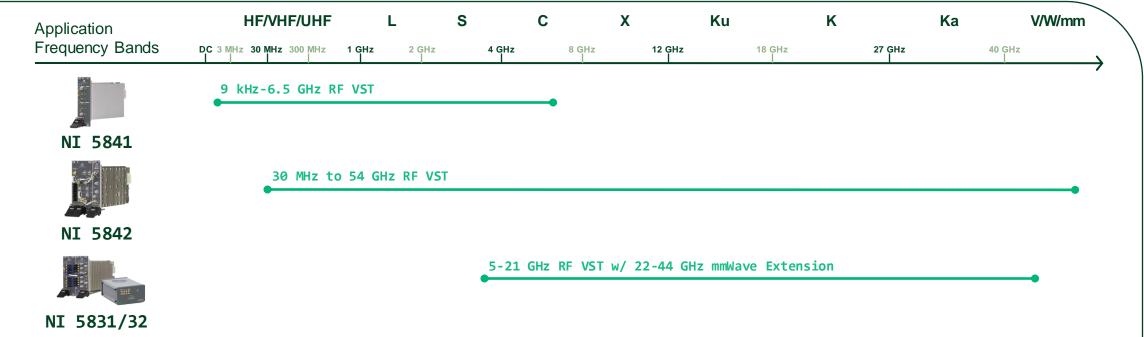
Customizable firmware for deploying application IP or test speed optimization

- Onboard, open FPGA
- Full rate peer to peer streaming to FPGA coprocessors

Vector Signal Transceiver Product Family



Vector Signal Transceiver



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Third-generation VST Provides Extended Frequency and Bandwidth Coverage

PXIe-5842 26.5 GHz VST

- Expand Capabilities with Flexible Licensing/Upgrade Options
- Expand Functionality with additional HW

- mmWave extension up to 54GHz
- Common SW tools to PXIe-583x and PXIe-5841
- Full IBW I/Q Data movement supported via integrated High-Speed MGT interfaces and PXI ecosystem including the new NI 7903 FPGA Co-Processor

Parameter	Instrument Capability	
Frequency Range	30 MHz – 23 GHz (Q4 2022) 30 MHz – 26.5 GHz (H2 2023)*	
Bandwidth	Up to 2 GHz	
RF IN / OUT Flatness (2GHz)	< ±0.45 dB typ. / < ±0.4 dB typ.	
RF IN / OUT Absolute Accuracy	< ±0.4 dB typ.	
Max Unleveled Tx Power	+20 dBm typ. (<18 GHz)	

*Upgrade from 23 GHz HW to 26.5 GHz HW requires a paid upgrade service

PXle-5842 (module)	PXle-5655 Required LO
PXIe-5842 Vector Signal Transceiver ACC ACTIVE	KF OUT
MGT 100 DDFF 3 BP 3 DUF 3 BP/PSE	LO UN LO UN LO UN LO UN LO UN NAX REVERSE
	RF IN LO OUT AV State MAX NOVERSE LO IN AV State MAX NOVERSE LO IN AV State AV State MAX NOVERSE LO IN State AV State MAX NOVERSE LO IN State NOVERSE LO IN State
N OUT	

PXIe-5842 VST

PXIe-5842 with 54GHz Freq Extension | High Level Overview

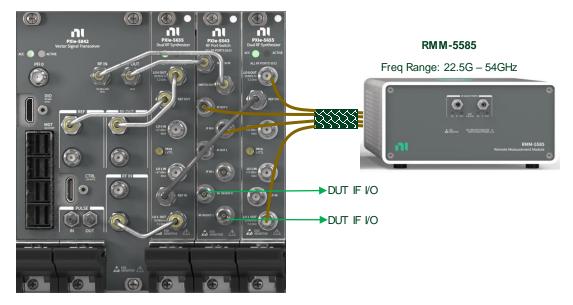
Key Features

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- Extended, Wideband coverage for mmWave Applications such as 5G, Satcom, Radar, and EW
- 2x Bidirectional RF ports for both mmWave and IF DUT connections
- Simultaneous operation of RF Tx & Rx ports on a single RMM-5585
- Independent frequency tuning of RF Tx & Rx ports on RMM-5585

Parameter	Instrument Capability	
Frequency Range	22.5GHz – 54 GHz (RMM-5585 RF IN/OUT) 100 MHz – 23 GHz (PXIe-5543 RF IN/OUT)	
Bandwidth	2 GHz	
RMM RF IN/OUT Flatness (2GHz BW)	1.2 dB (39GHz)	
RMM RF IN/OUT Absolute Accuracy	± 1.0 dB (39GHz)	
RMM RF OUT Max Power	28 GHz: +13 dBm	
5G NR,100MHz EVM	Better than -43 dB @ 47GHz	

PXIe-5842 VST with 54 GHz Freq Extension



High Dynamic Range Analyzer

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26.5 GHz Vector Signal Analyzer

High Dynamic Range

• Superheterodyne Architecture with Image Rejection and Signal Conditioning

Wide Instantaneous Bandwidth

Optimized Phase Noise

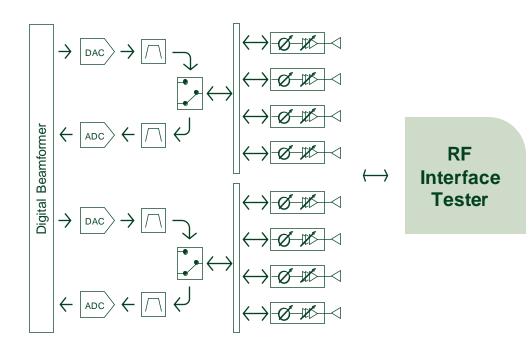
PXIe-5668 Specifications

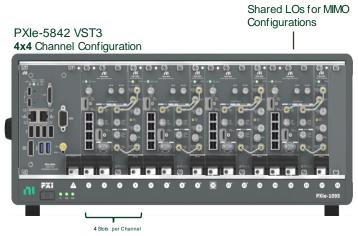
	Without NI 5698 Pre-amplifier	With NI 5698 Pre-amplifier	
Frequency Range	20 Hz to 26.5 GHz		
Analysis BW	320 MHz below 3.6 GHz 765 MHz above 3.6 GHz		
Phase Noise	-129 dBc/Hz @ 1 GHz (Typ, @10kHz offset) - 120 dBc/Hz @ 8 GHz (Typ, @10kHz offset)		
RMS Noise Floor (Nominal)	< -157 dBm/Hz (1 GHz) < -150 dBm/Hz (26 GHz)	< -170 dBm/Hz (1 GHz) < -157 dBm/Hz (26 GHz)	
тоі	> +19 dBm (20 Hz to 26 GHz)	> -13 dBm (1 GHz) > -13 dBm (1 GHz)	
Non-Input Related Spurs	< -115 dBm (1 GHz) < -105 dBm (26 GHz)	< -131 dBm (1 GHz) < -115 dBm (26 GHz)	
No. of Slots	7	8	



Digital AESA RF Measurements

Key Test Challenge: Provide robust and abstractable mixed I/O interfaces that can scale and adapt to evolving DUT needs while easily integrating I/O such as highspeed serial interfaces with RF instrumentation in order test functionality in an optimized and synchronous manner.





The NI Approach

High Performance, Multi-Channel RF Instrumentation

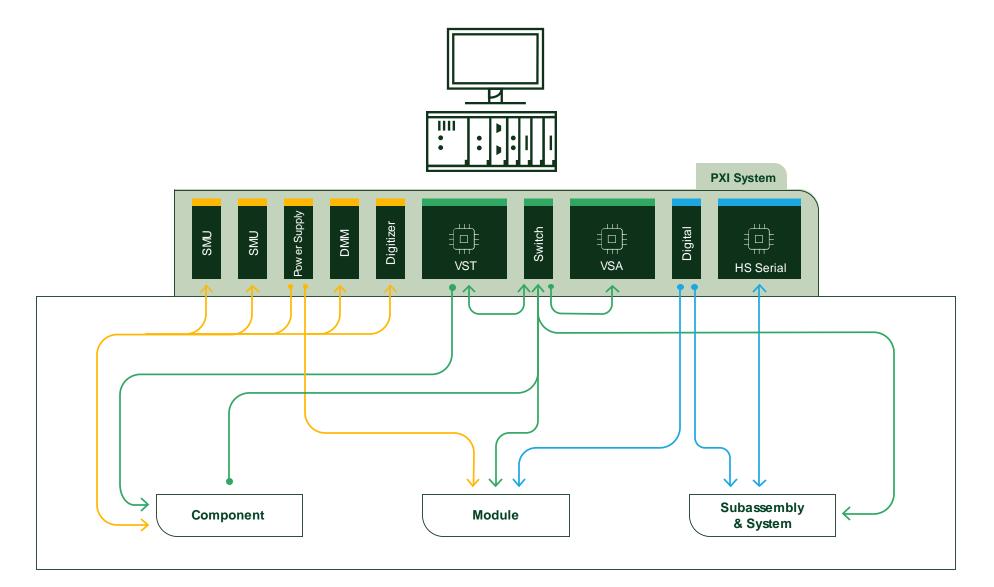
- Optimized for Wideband Measurements
- Expandable to multiple synchronized, phase-coherent channels
- Synchronization across PXI to Mixed I/O interfaces
- Scalable Measurements and Application IP
 - Traditional Host Based Data Processing and Customizable FPGAs for Real-Time HIL needs



The NI Solution for RF + Digital Test

A system level, NI Solution

Modular Automated Test Bench



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Modular Automated Test Bench

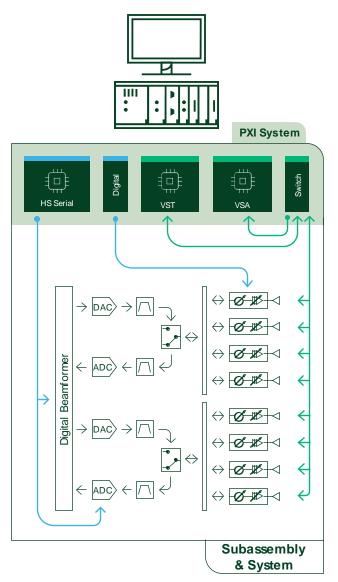
Digital Control & Highspeed Data

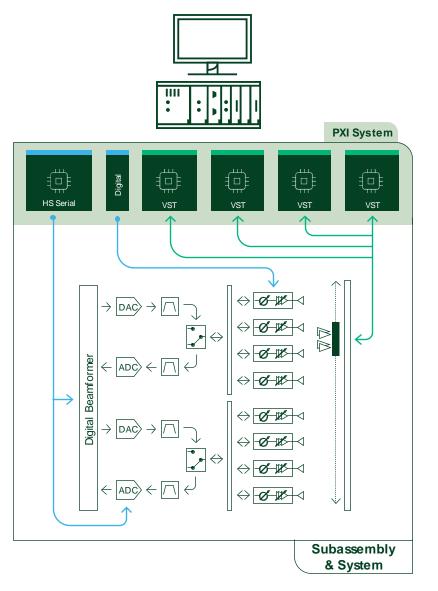
Digital Control

- LVDS, TTL Control Pattern Based Digital
 - 100 MVectors/s
- PPMU, Voltage and Current Highspeed Digital Transceivers
 - Up to 12.5 Gbps
 - 24 TX and RX lanes

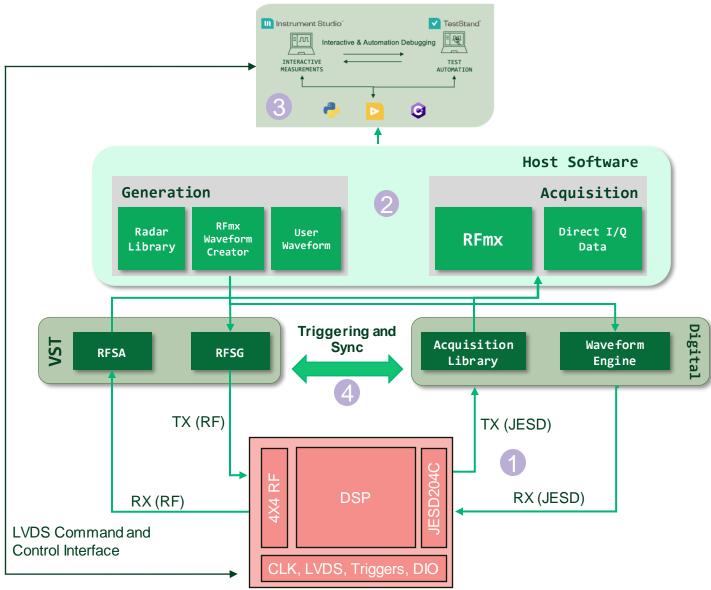
RF Stimulus and Response

- Vector Signal Analyzers, Generators, and Transceivers
- Up to 1 GHz of Instantaneous BW
- Software Defined with Open FPGA
- < 100psecsynchronization with phase coherency





Electronically Scanned Array Characterization (ESAC) Offering for "RF to Bits" Validation



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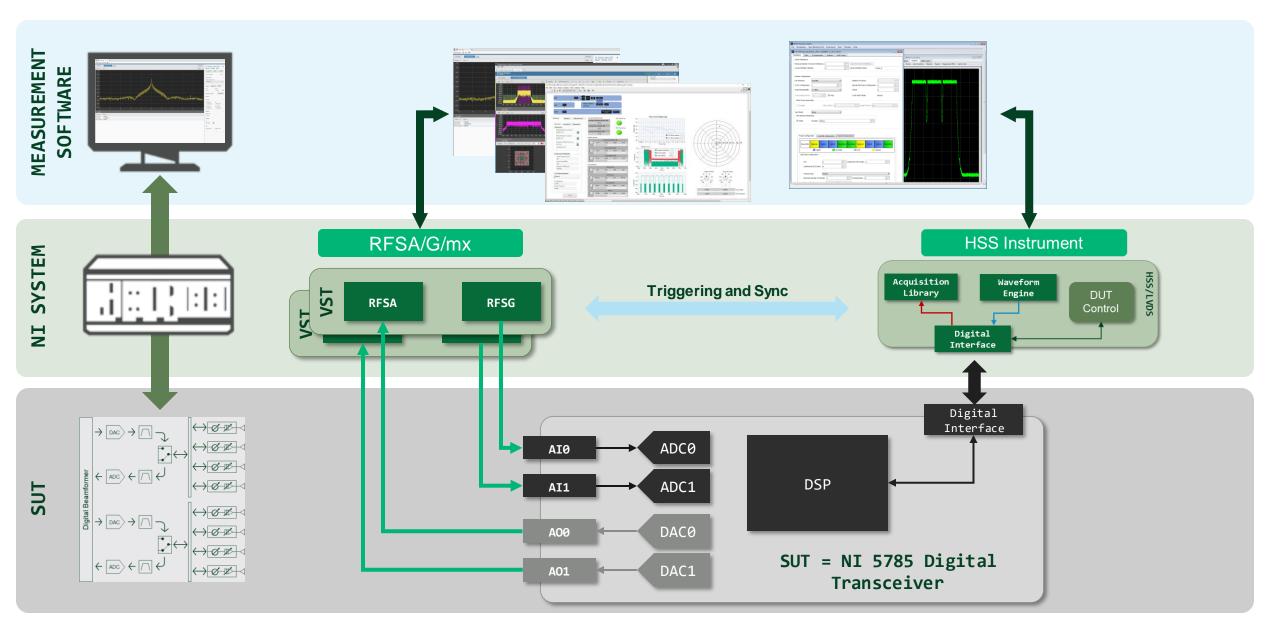
NI Provided Elements:

- 1. Industry Standard and Customizable Digital Interfacing
 - JESD204A/B/C, Aurora, 100Gb Ethernet, Proprietary
- 2. Integration of RF/Digital for standard measurement libraries
 - RFmx SpecAn, Phase Noise, Noise Figure
 - RFmx Pulse
 - Application Specific Measurements and Custom IP
- 3. Interactive Workflows supported by NI InstrumentStudio and NI TestStand
- 4. Synchronization between RF & Digital interfaces for coherent measurements (future)
- 5. Expansive Capabilities via PXI Ecosystem
 - Multi-Channel Synchronization, I/Q Data Movement, Real-Time FPGA based Processing, Record & Playback

Value Statements:

- 1. Minimize time to first measurement
- 2. Provide maximum measurement flexibility
- 3. Minimize integration issues
- 4. Implement software architecture that will scale throughout lifecycle

NI Digital TRM Characterization – Demonstration Overview



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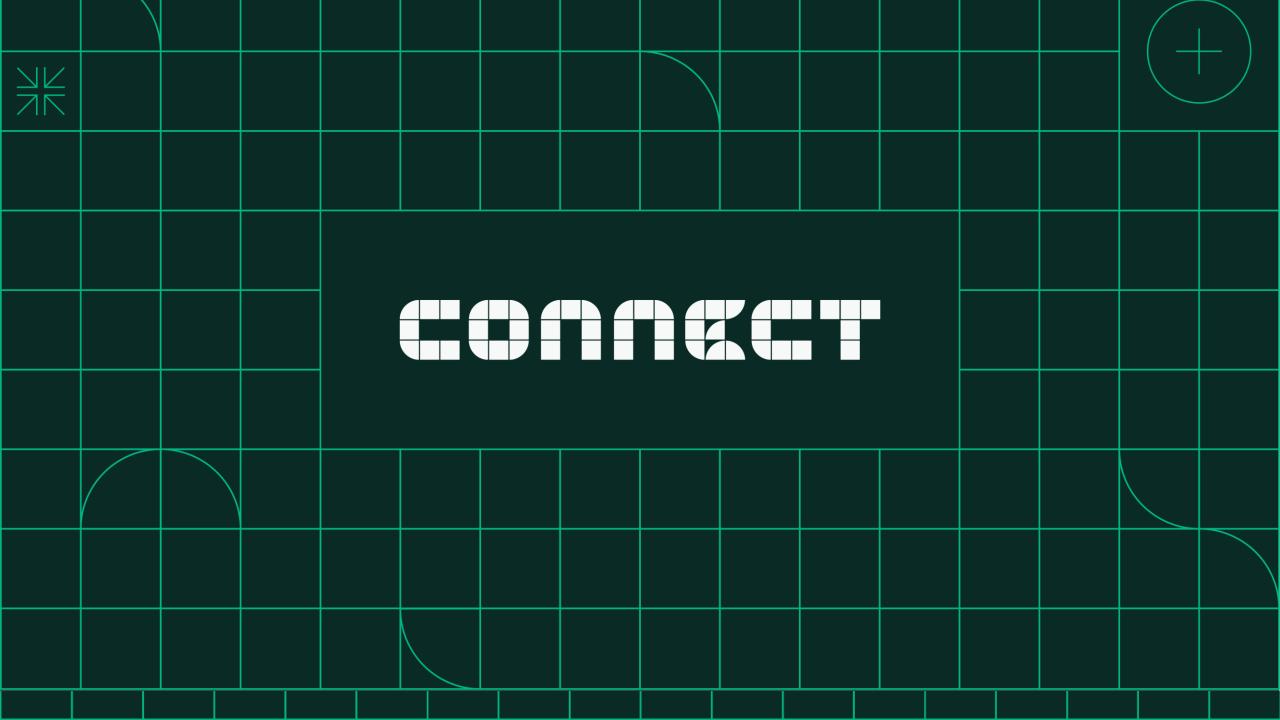
Today's Active Electronically Scanned Array (AESA) systems are becoming increasingly more capable due to market and technology trends such as

- Advances in GaN based RF components and Wide Bandwidth Data Converters
- High Density and Scalable Array Architectures
- Full Integration of Digital and RF Domains True "RF to Bits

The Digital AESA creates a unique test challenge for traditional RF centric measurement solutions and workflows based on the mixed domain interfaces, diversified mission and application space, and sheer amount of data generated.

NI approaches this challenge with the strengths of the PXI ecosystem and high-performance software tools that scale to higher RF channel counts, wider digital data pipes, and complex measurement science needs.

• See it in action in the Aerospace and Defense Experience Lounge, or contact your NI representative for more information!



Give us your feedback! Quick 2 Question Survey

In the mobile app, click into the session you would like to provide feedback for



10:15 AM Multichannel RF Data Recording 11:15 AM and Analysis

Meeting Room 19A

Aerospace & Defense •
 Technical Session

10:15 AM Optimizing Validation Processes: 11:15 AM Building Complex Test Systems with Distributed I/O

- Meeting Room 19B
- Aerospace & Defense •
 Technical Session

10:15 AM Panel: Continuous Integration (Cl/ 11:15 AM CD)—Don't Leave Home without It

- Meeting Room 12A
- Programming Essentials Technical Session

10:15 AM Using Python and TestStand to 11:15 AM Boost Your Test Development

Ballroom G

 Product & Technology • Technical Session

10:15 AM What Does Left Shifting Test 11:15 AM Mean in the NI Ecosystem?

Meeting Room 18A
 Transportation - Technical Session

〈 Tue May 23

🛨 Add to Schedule 🛛 🏥 iCal 🛛 👤 Check In

Optimizing Validation Processes: Building Complex Test Systems with Distributed I/O

Tue May 23 10:15 AM - 11:15 AM

Map Meeting Room 19B
 Aerospace & Defense • Technical Session

C Surveys

Take Session Survey

In this session, learn to improve efficiency and reduce non-recurring engineering costs in validation labs by connecting multiple distributed line-replaceable unit (LRU) test systems. Also learn how to abstract LRUs and construct complex test systems faster and more efficiently using existing distributed I/O and edge computation technology.

Click "Take the Session Survey"

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