From Tip to Tail: Solving Defense Aircraft Test Challenges

Tuesday, May 24th – 2:30pm

Brandon Treece, NI

Eric Metzler, Viewpoint Systems

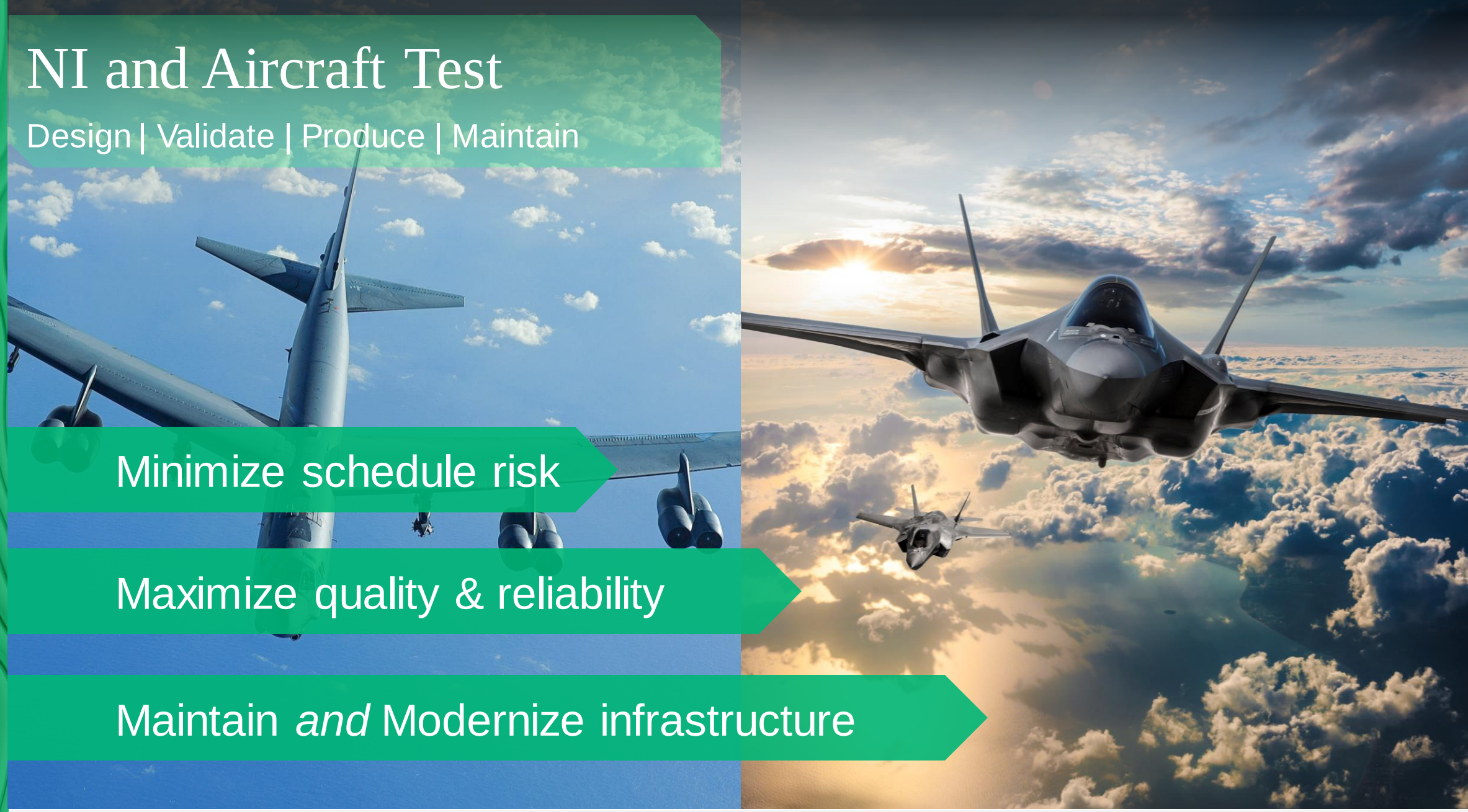
Jennifer Platt, Tech 180

From Tip to Tail: Solving Defense Aircraft Test Challenges

Brandon Treece
Chief Solutions Marketing Manager
Electronics Test, Defense Aircraft
Aerospace, Defense, and Government
NI

NI and Aircraft Test

Design | Validate | Produce | Maintain



Minimize schedule risk

Maximize quality & reliability

Maintain *and* Modernize infrastructure

“Modern” Aircraft

NI and Aircraft Test

Design | Validate | Produce | Maintain

Electrical & Mechanical

Test and simulate hundreds of systems to ensure reliable operation across all mission scenarios

Radar & Electronic Warfare

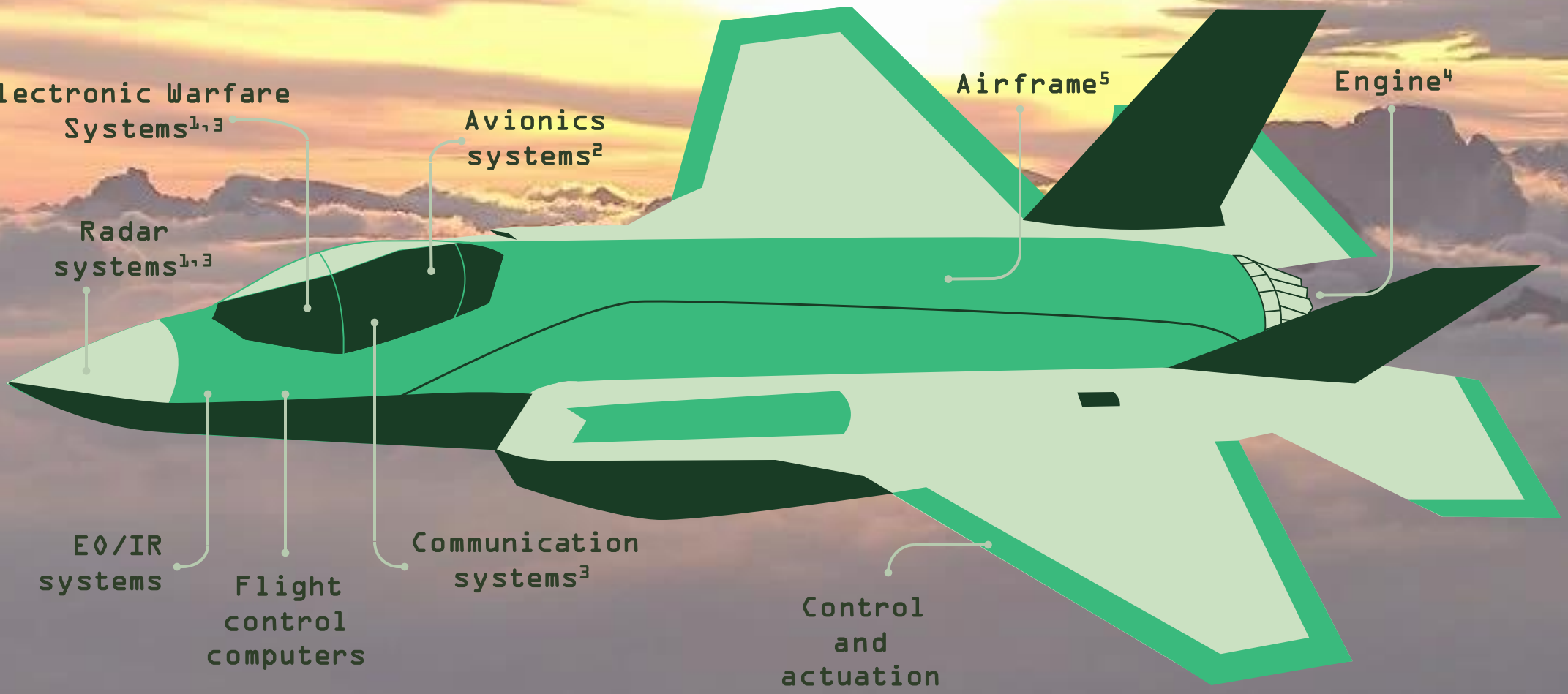
Ensure reliable operation in an increasingly contested and congested electromagnetic spectrum

Communication, Navigation, & Surveillance

Operate military navigation, telemetry, and datalinks while coexisting with commercial systems

“Modern” Aircraft

NI and Aircraft Test



[1]Solving the Latest Challenges for Testing Electronically Scanned Arrays - Tuesday @ 3:30
[2]Digital Avionics Interface Selection - Simplifying a Not So Simple Choice - Wednesday @ 9:00
[3]Rapidly Prototyping Cognitive RF Systems - Wednesday @ 10:15
[4]Testing Propulsion Systems Across the Aerospace Industry - Wednesday @ 11:00
[5]Deploy Static and Fatigue Structural Test Systems with COTS Tools - Aerospace Pavilion

Addressing Challenges of FPA Test

Eric Metzler

System Architect

CLA, CTA, CPI

Viewpoint Systems

Aedis Framework

FPA and Electronics Payload Emulation

Eric Metzler
System Architect
CLA, CTA, CPI
Viewpoint Systems

Carl Kosmerl
John Farnach

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EO/IR System Landscape by Mission

Remote Sensing

Night Vision

Rangefinding / Designation

ISR

IRST

IR Homing

Laser & IR Targeting

Electronic Warfare

IR Threat Warning

Laser Threat Warning

Laser / IR Countermeasures

Directed Energy

Typical FPA Payload Subsystems

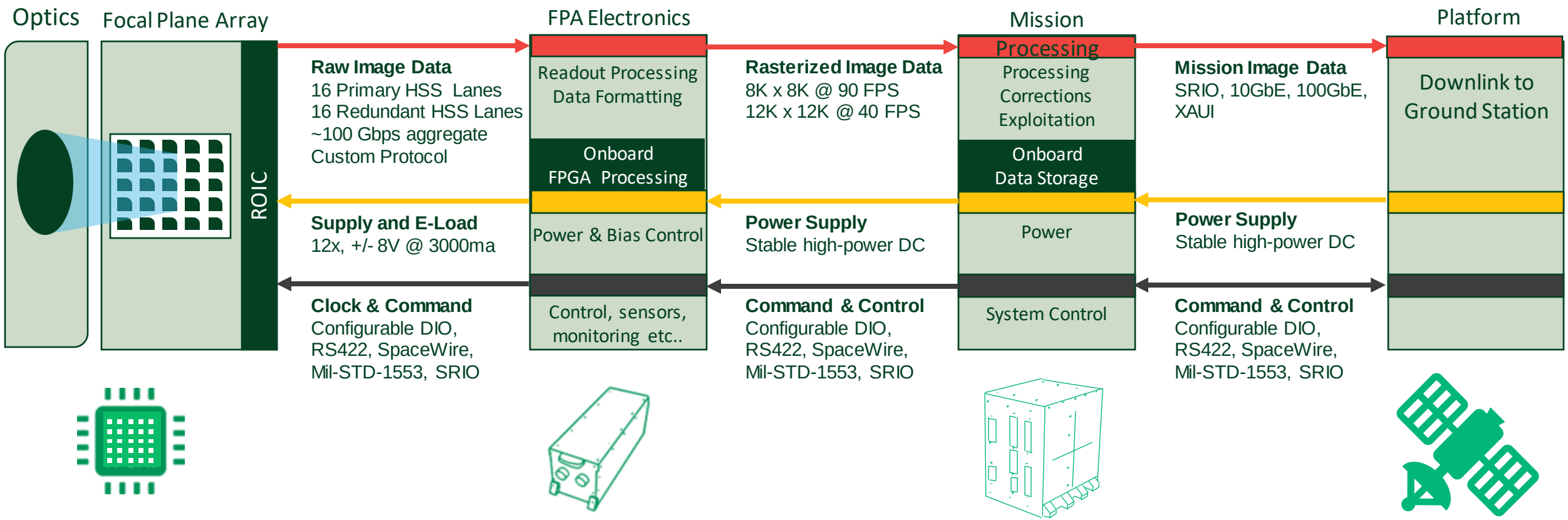
High Speed Data
DC Power
Digital Control

Data Flow

Photons to Bit
12K x 12K Image
Serialized For Transfer

De-Serialization
Image Pre-processing

Image Processing
Atmospheric correction
Cognitive Analysis



Device or Dewar Assembly

Space VPX Subsystem

Mission Processing System

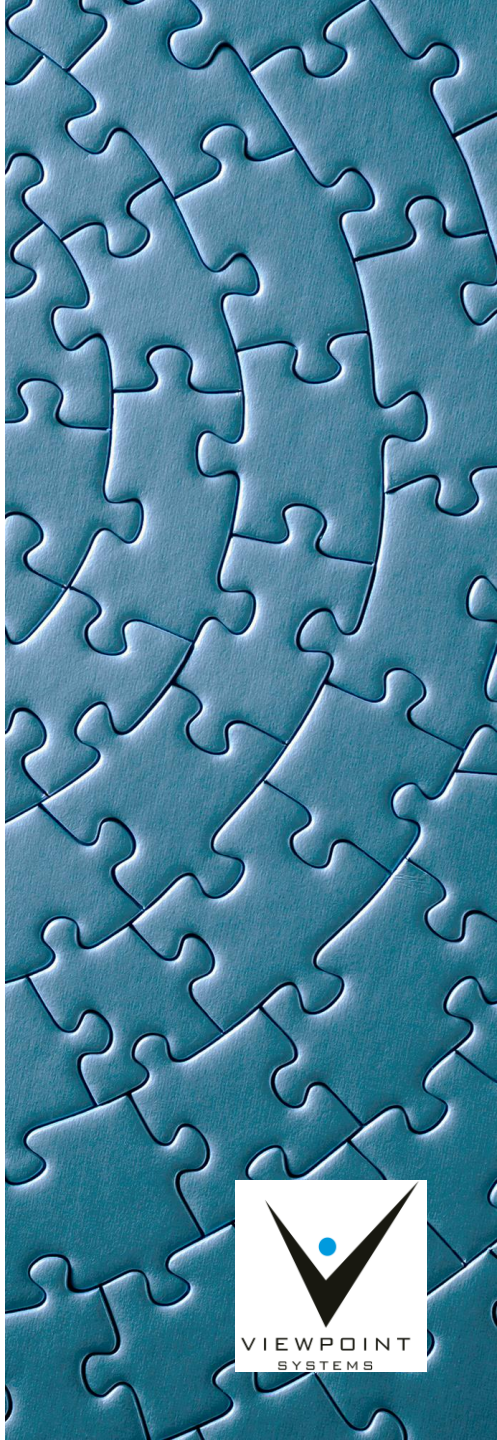
Key Challenges

- FPA testing/emulation is hard
  - High data rates/determinism
  - *Unique interfaces*
  - *Specialized hardware*
  - *No COTS test systems exist*
- Incomplete requirements
- Short, inflexible schedules
- Predetermined budgets

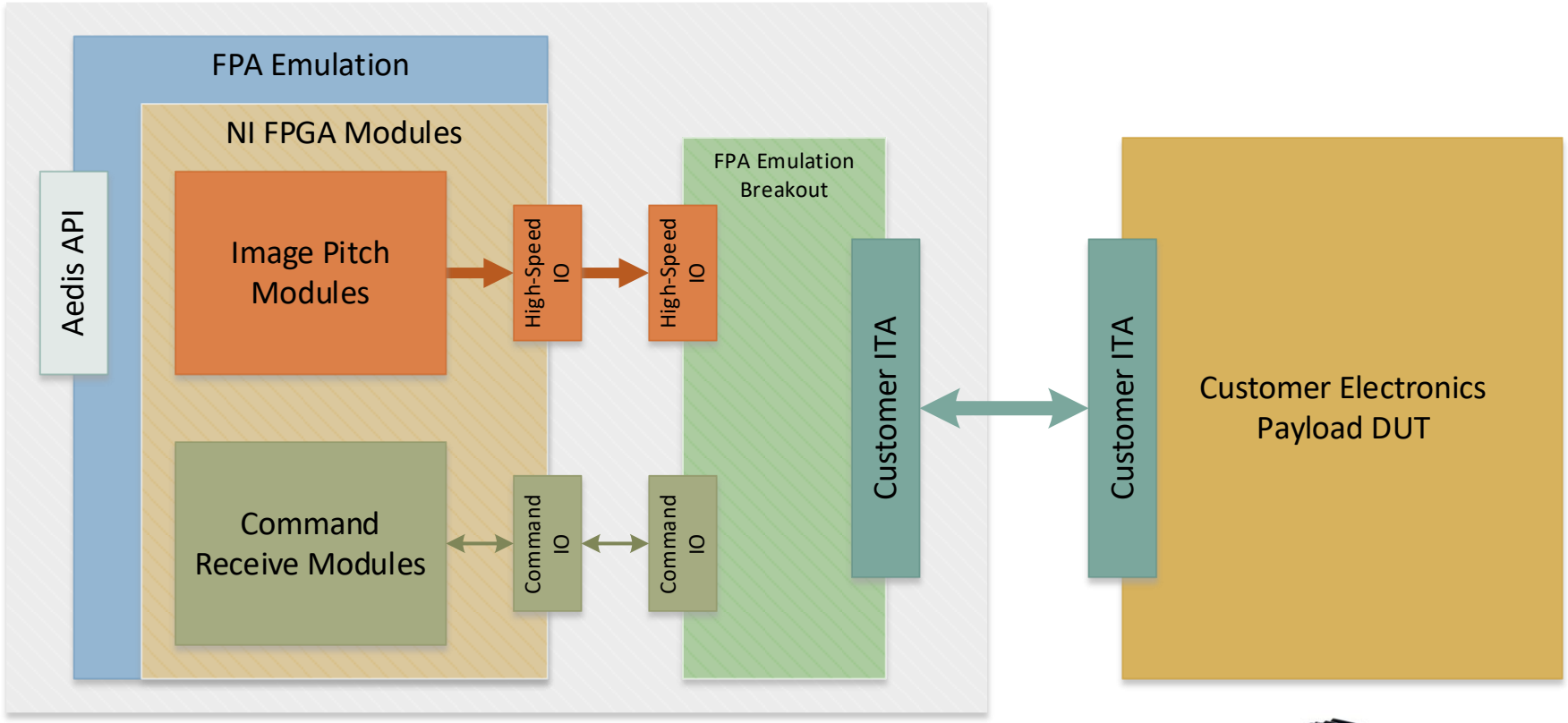
VIEWPOINT SYSTEMS

How is Aedis solving these problems?

- **Reduced development time**
  - Core set of customizable software components
  - Pre-built buffer electronics minimizes customization for specialized interconnects
- **Extendable architecture**
  - Allows for different sized sensor interfaces and IO count
  - Allows for unique customer processing in software
- **Validation readiness**
  - Hardware provides transmit and receive pathways
  - Complementary software modules for validating delivered system
  - Loopback capable
- Bridges the gap to complete requirements by providing pre-made solutions to common problems

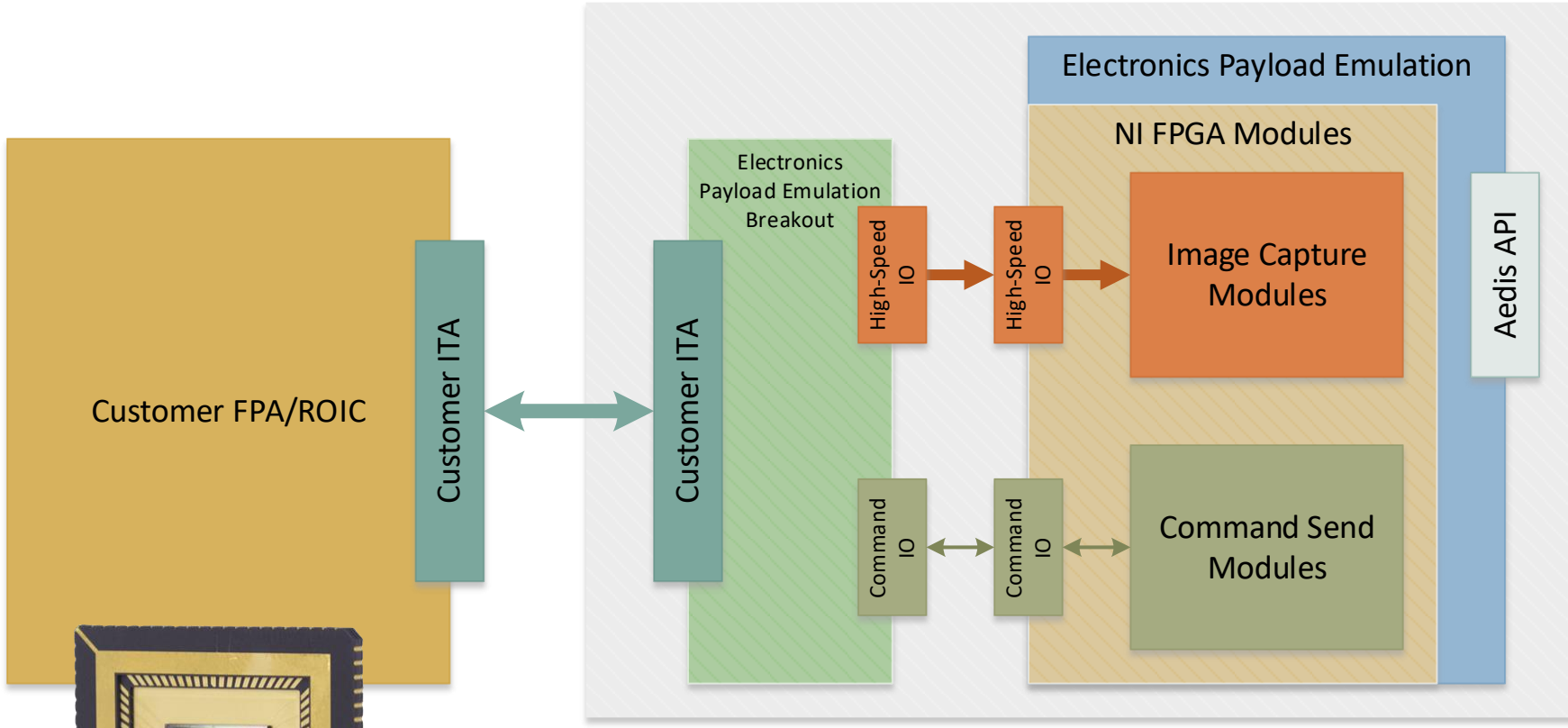


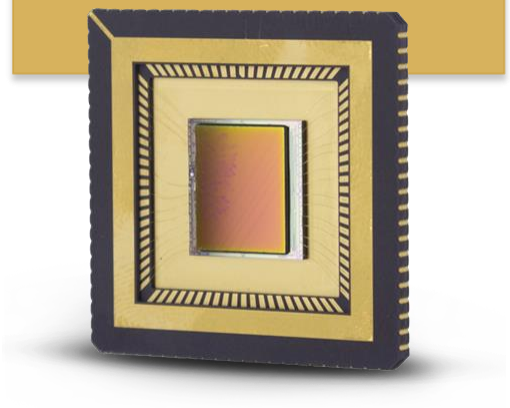
Aedis FPA Emulation Overview

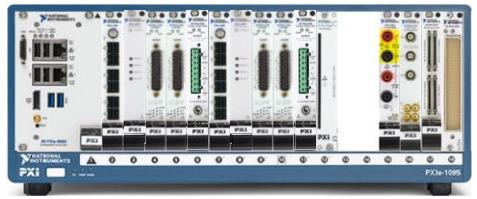


VIEWPOINT SYSTEMS

Aedis Electronics Payload Emulation Overview

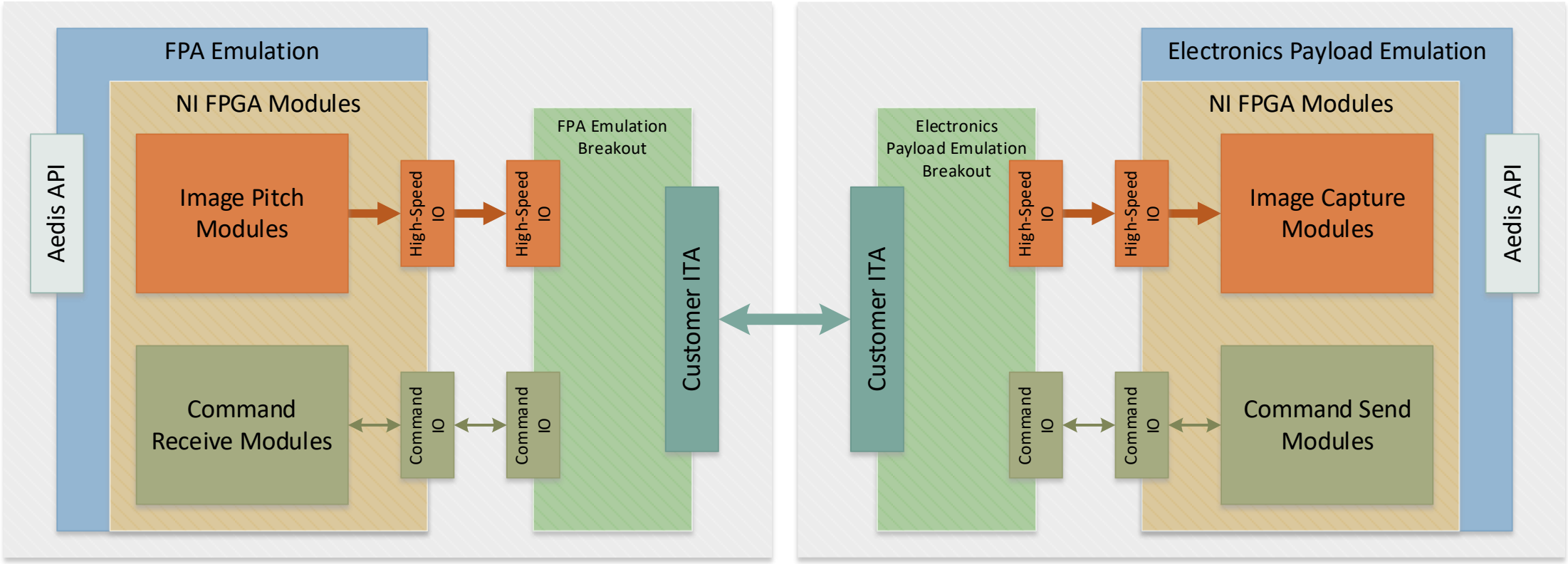




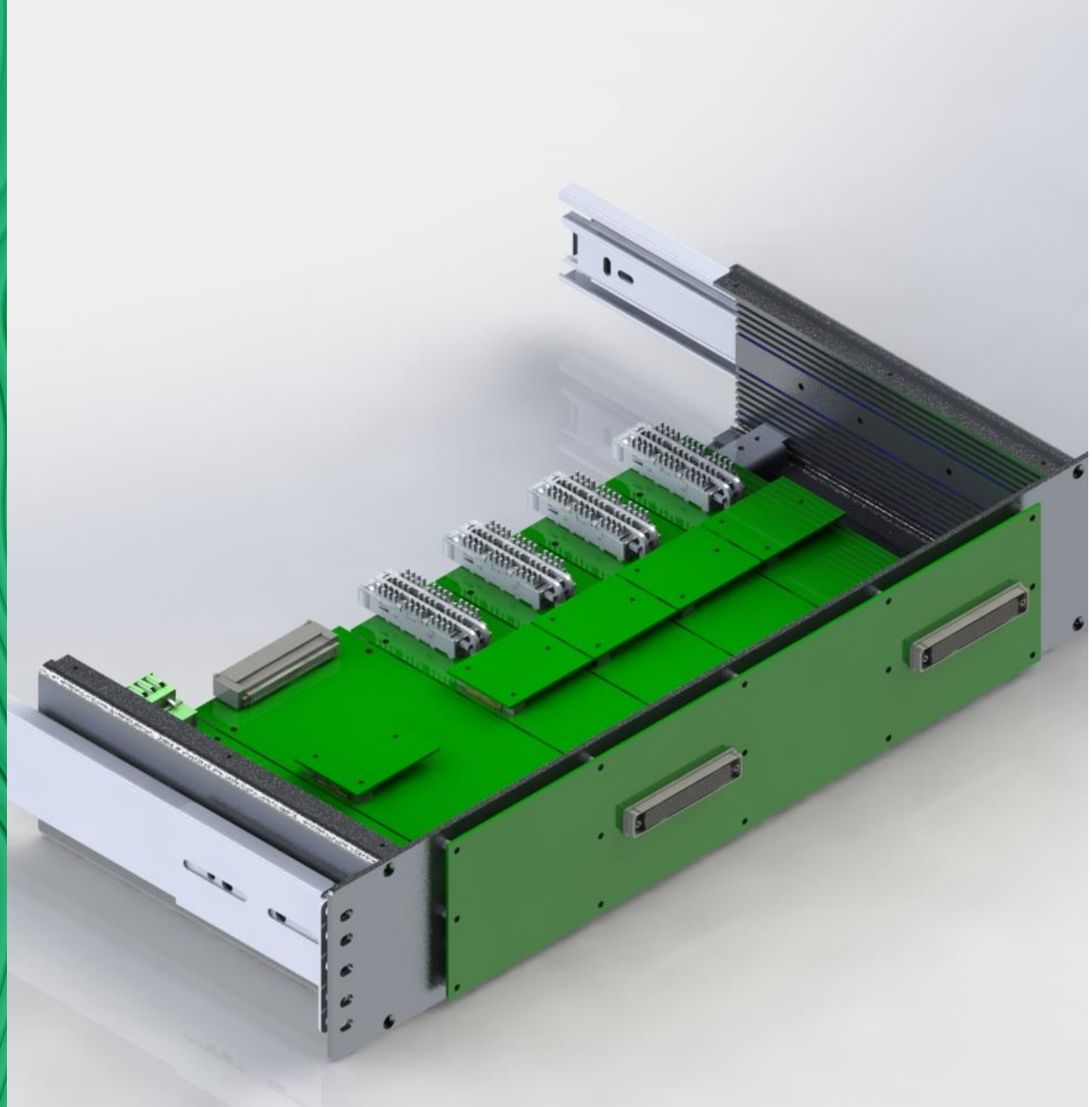


VIEWPOINT SYSTEMS

Aedis Validation Overview



VIEWPOINT SYSTEMS

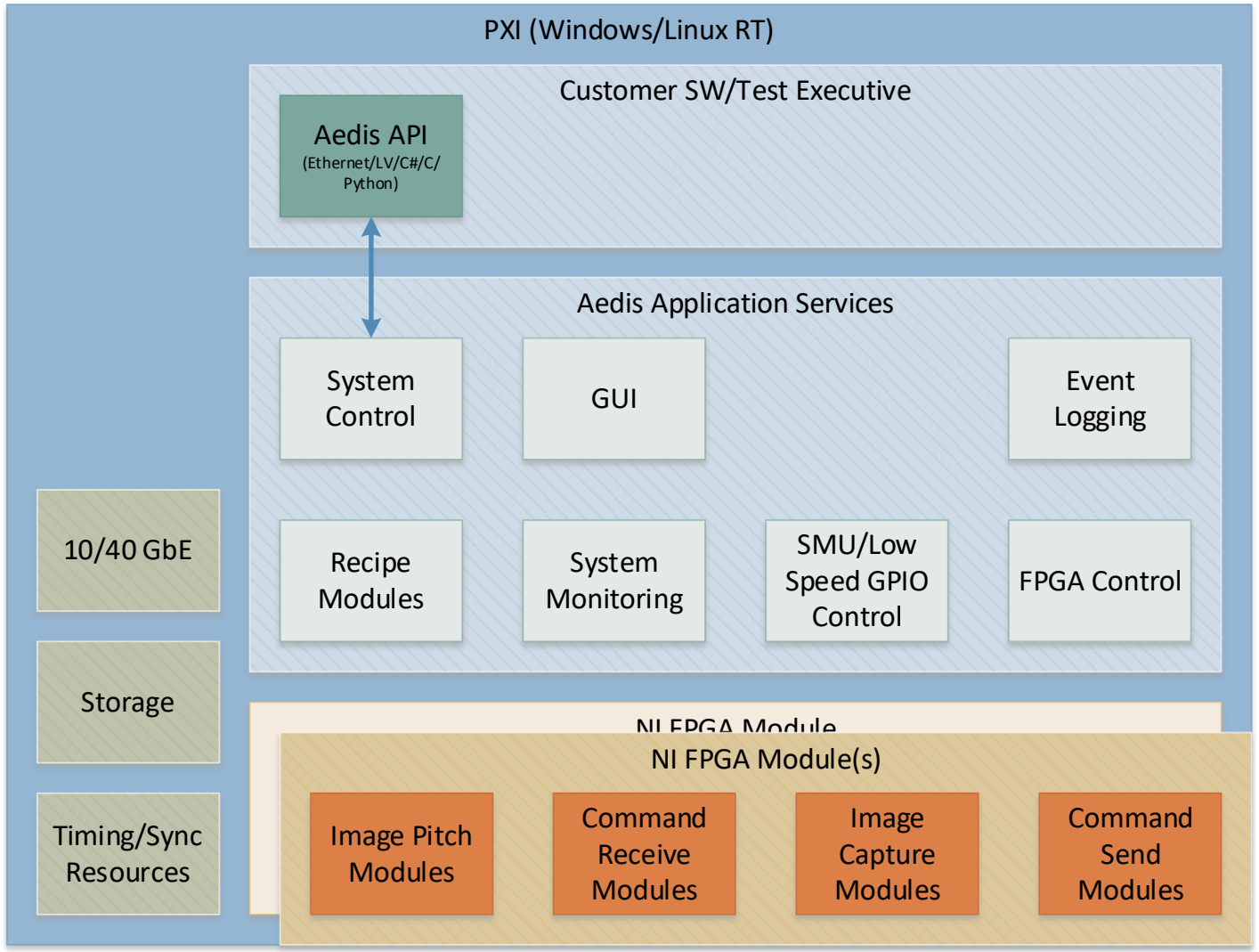


Interface Breakout

- NI interface to customer mass interconnect
- Modular electronics selected for application
- High-speed, full duplex signal buffering
  - LVDS
  - SERDES/CML
- Software configurable buffer control (per-channel)
- Test point access
- Power supply and load profiling

VIEWPOINT SYSTEMS

Aedis Software Overview



VIEWPOINT
SYSTEMS

Image Pitch Modules

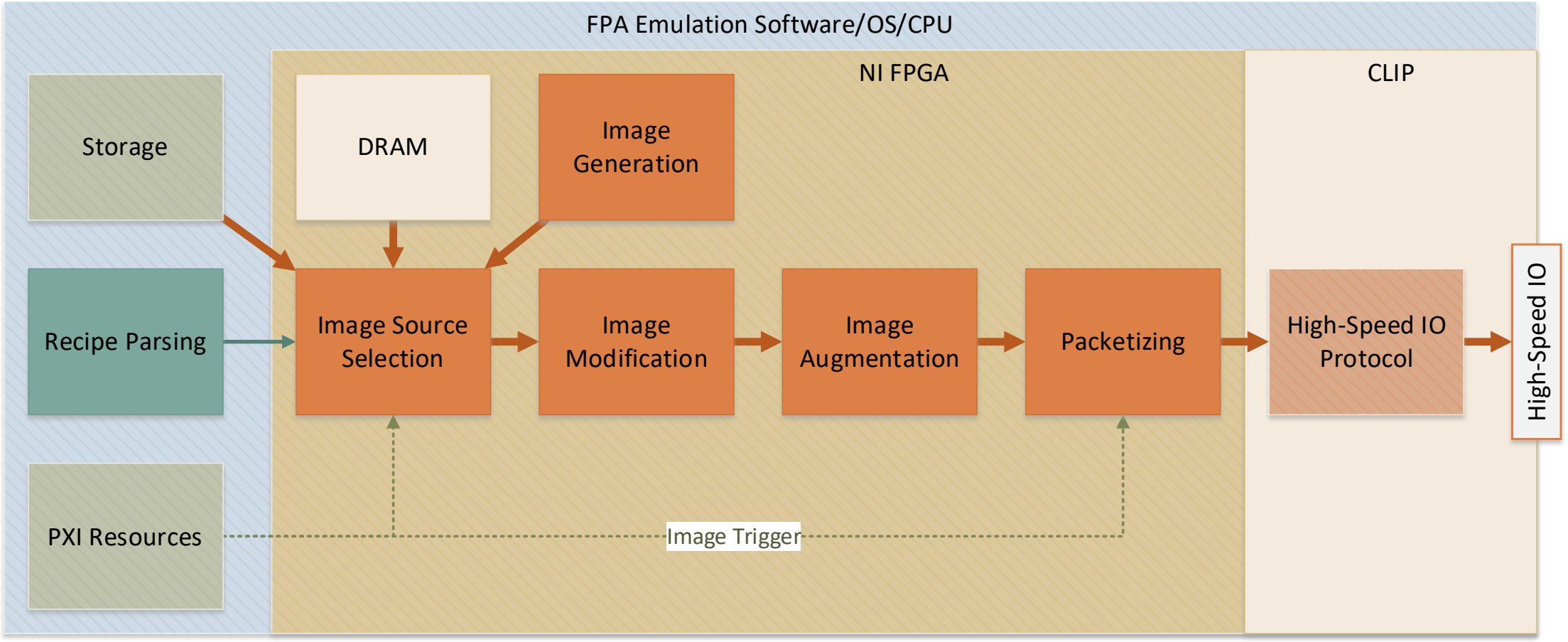
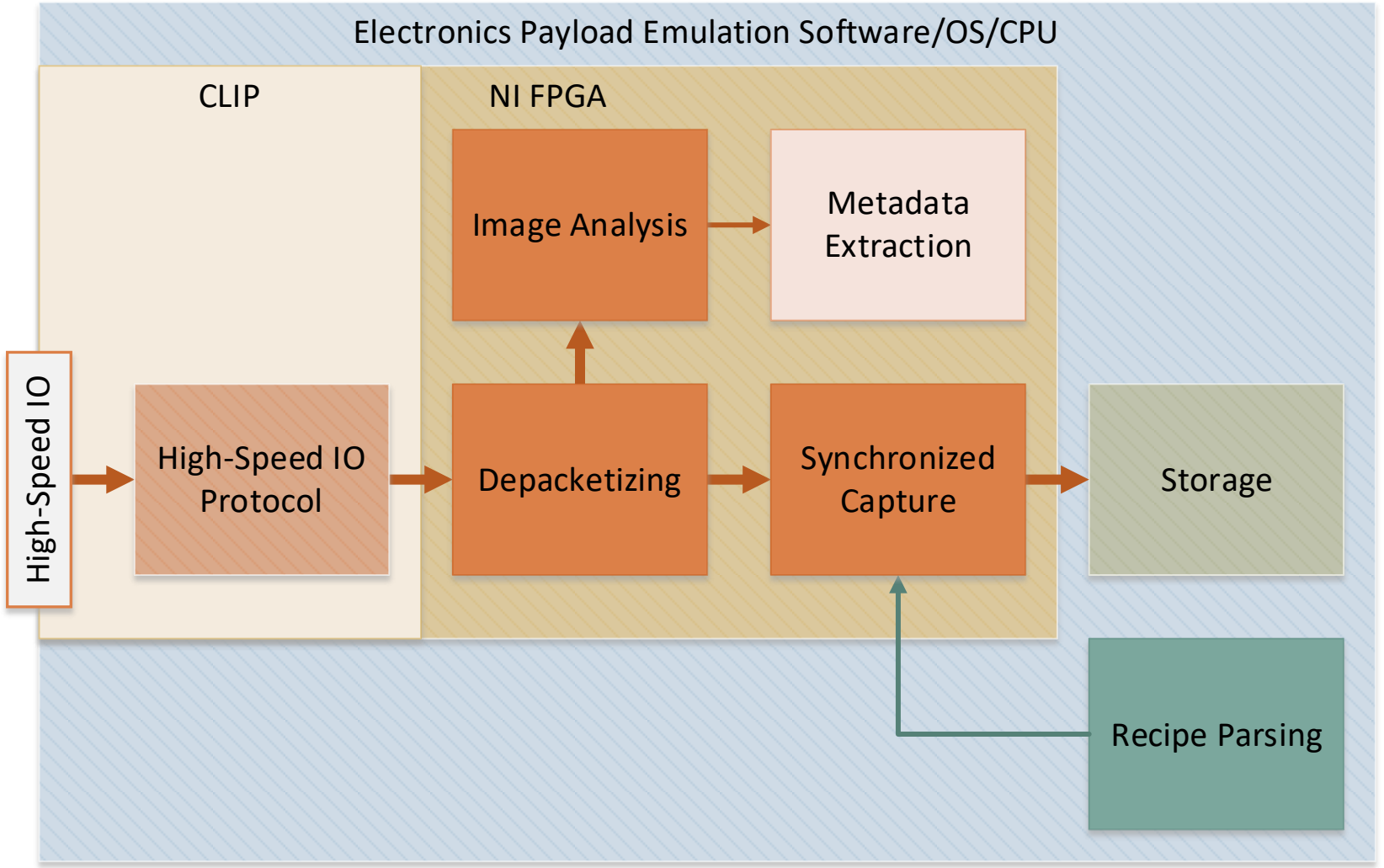
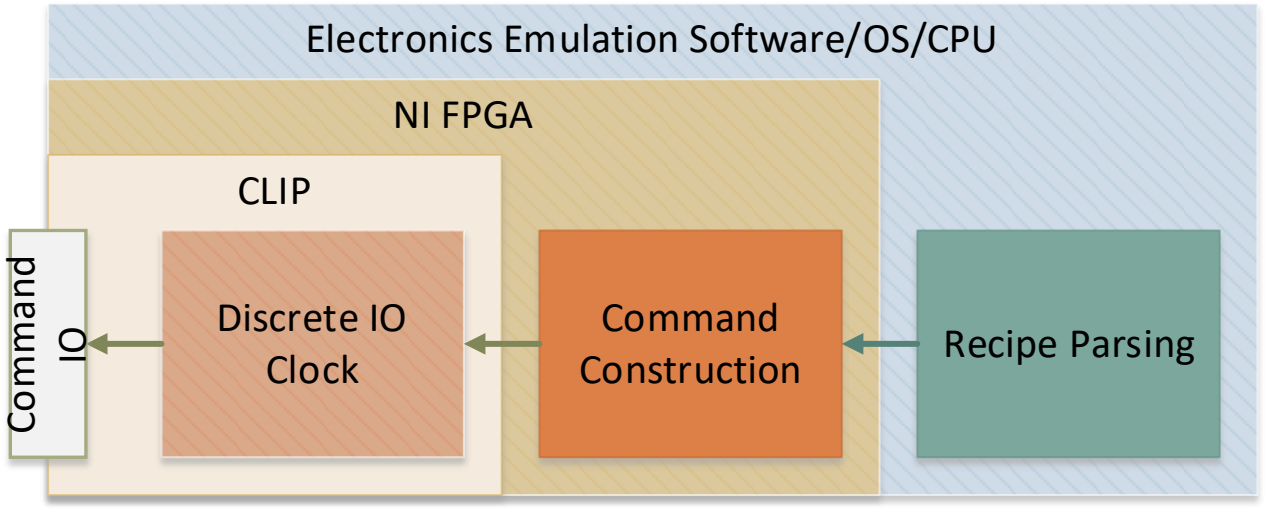


Image Capture/Analysis Modules



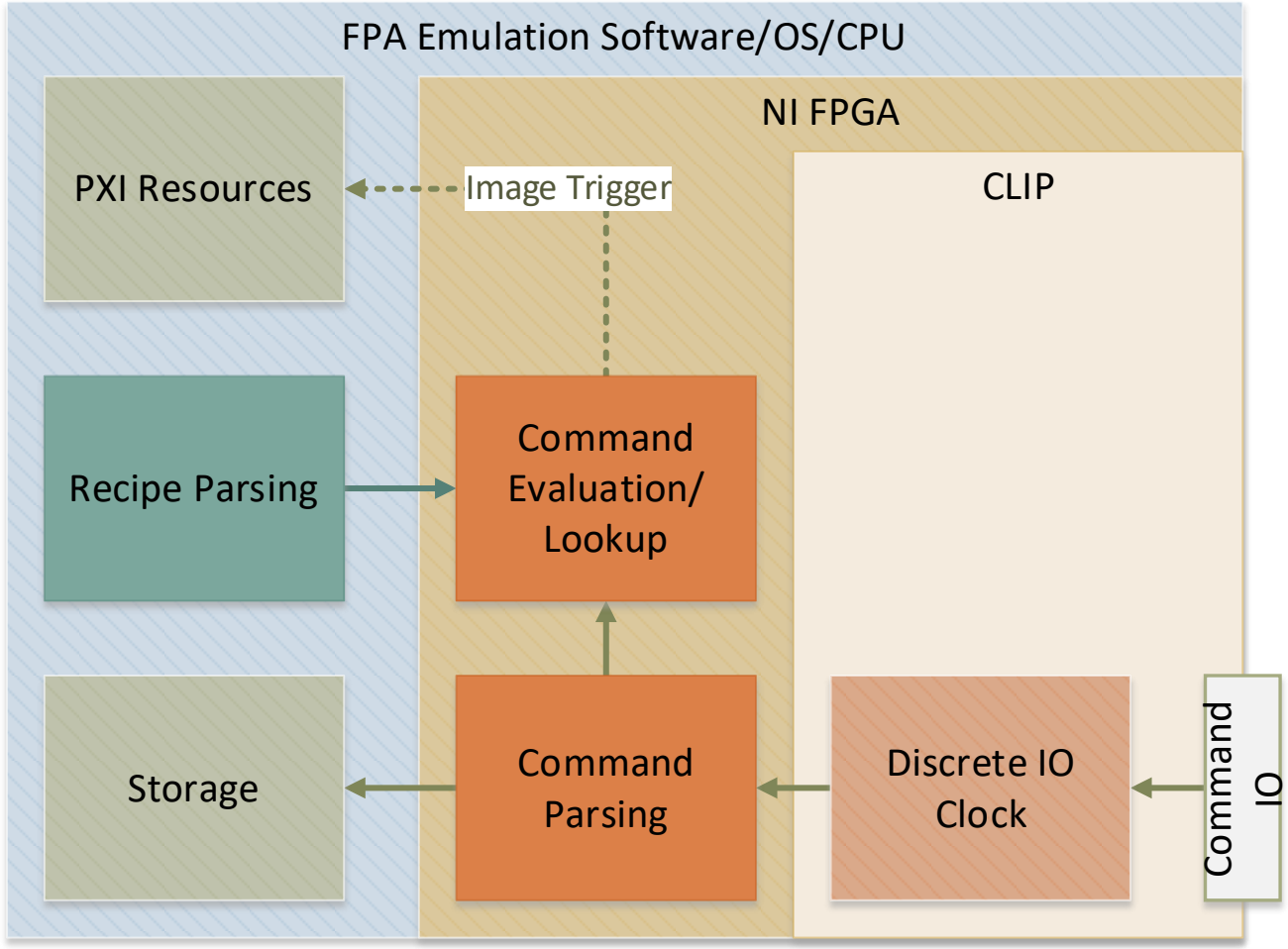
VIEWPOINT SYSTEMS

Command Send Modules



VIEWPOINT SYSTEMS

Command Receive Modules



VIEWPOINT SYSTEMS

Benefits and Contact

- Reduced development cost and time
- Expandability
- Extensibility
- Isolation of components for unit testing
- Ease of verification

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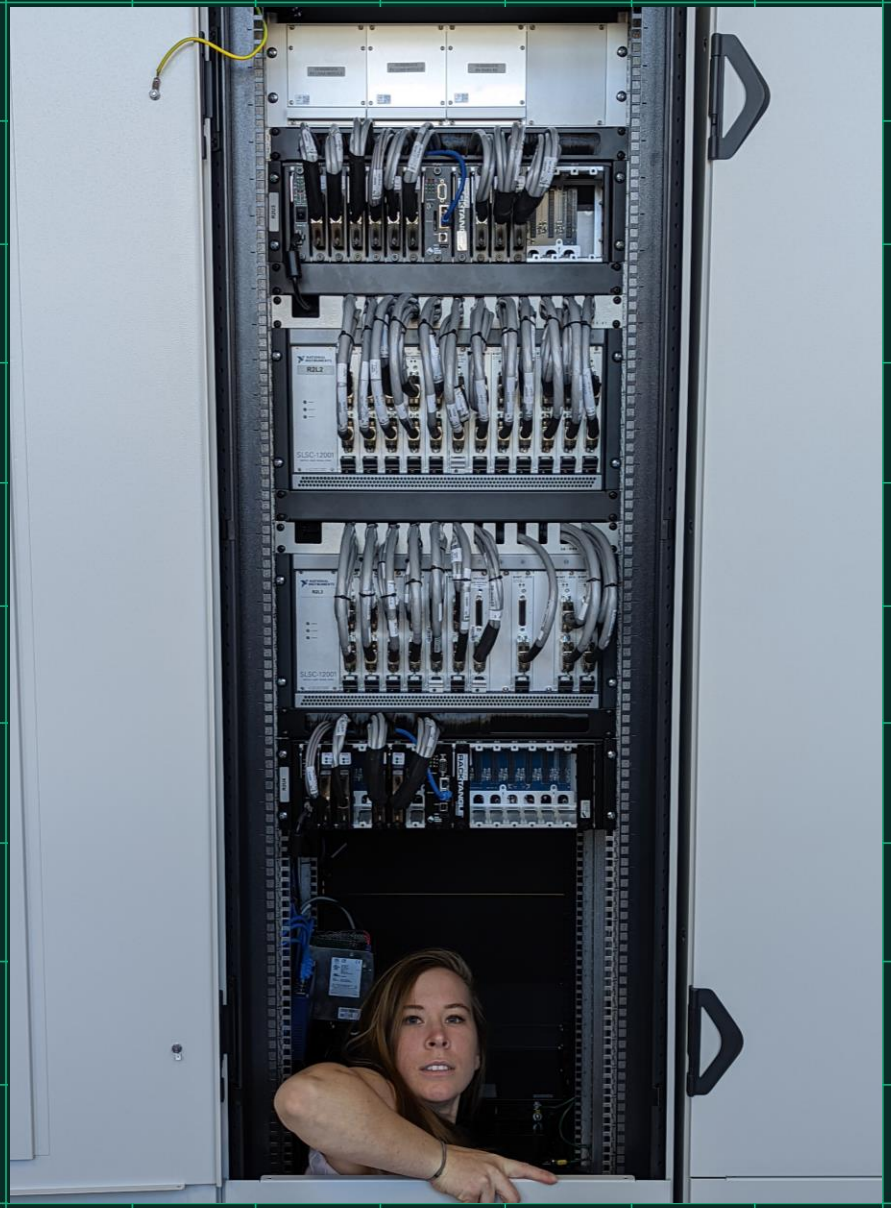
Addressing Challenges of LRU Test

Jennifer Platt
Lead Solution Engineer
Tech180



System-On-Demand (SoD)

Solving Complex Challenges in LRU Test

Jennifer Platt
Tech180
Systems Engineer

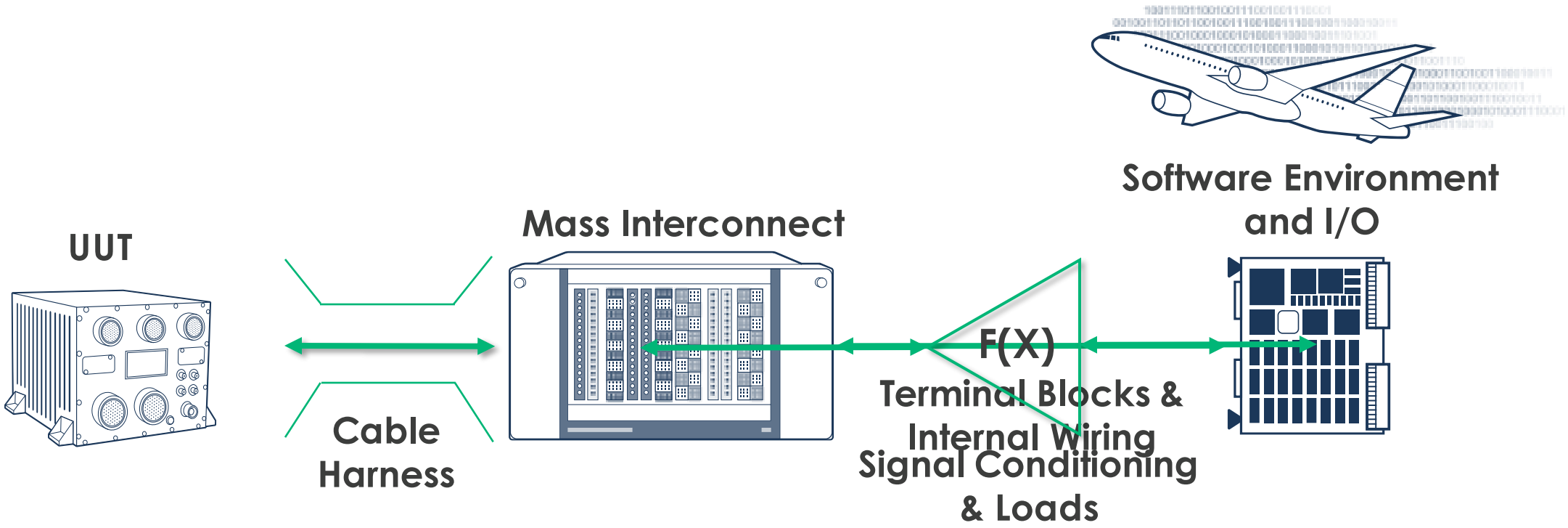
Overview

- What is System-on-Demand?
  - LRU test and SoD architecture
  - Key benefits
- How does System-On-Demand solve challenges in today's LRU market?
  - Single program schedule
  - Multiple lab integration

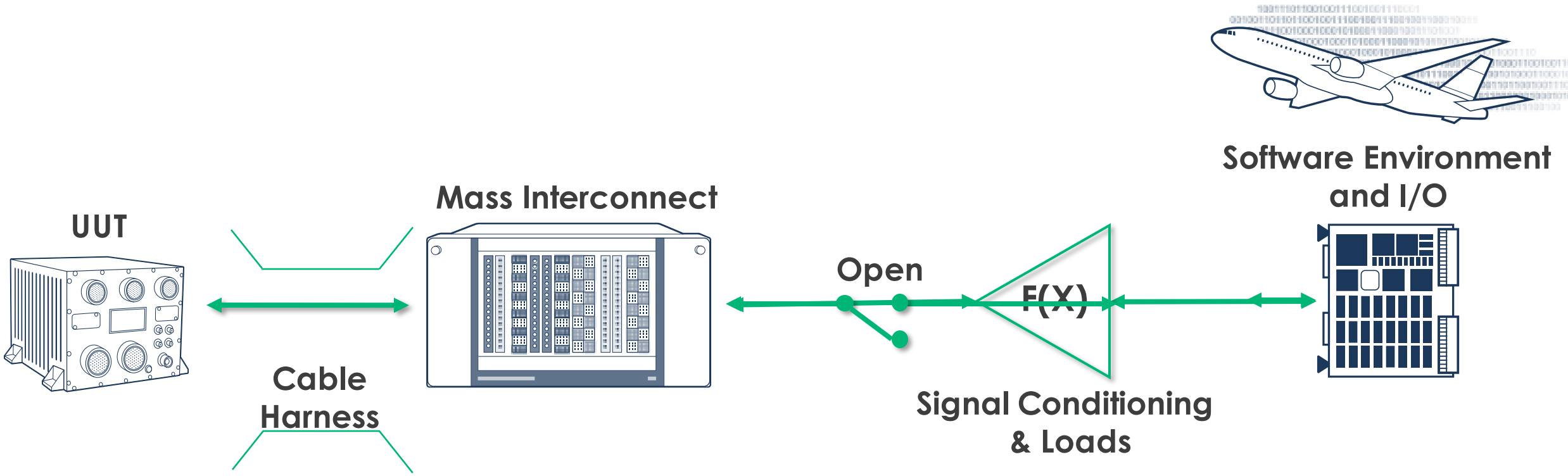
What is System-On-Demand?

- Powerful, flexible architecture built on NI PXI and SLSC platforms
- Supported by an automated toolchain and standardized parts

LRU Test Architecture



LRU Test Architecture



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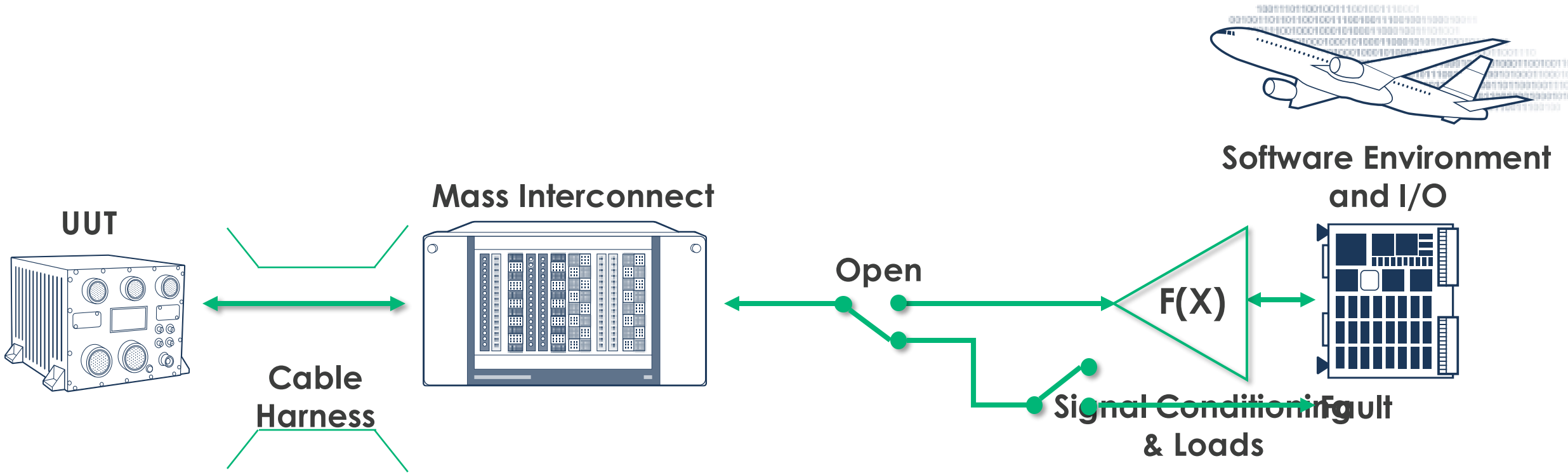

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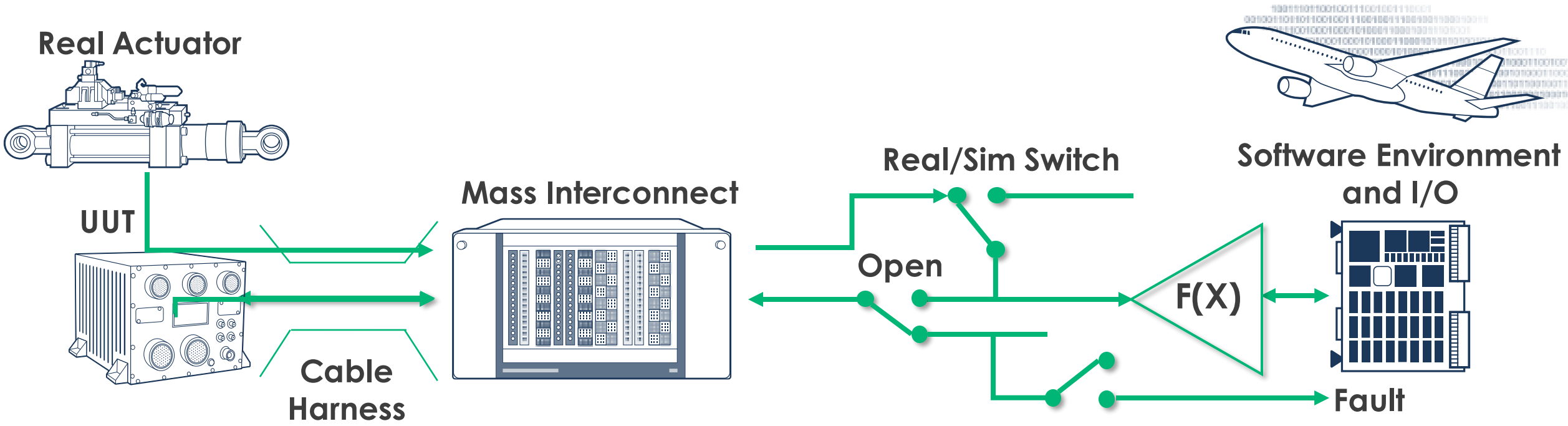

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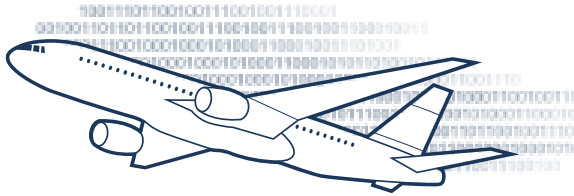
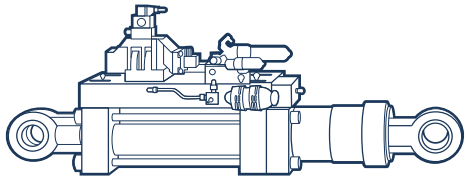
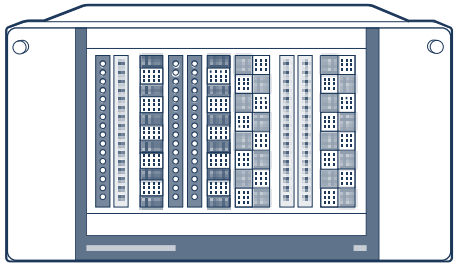


Real Actuator



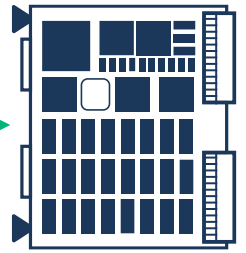
Software Environment and I/O

Mass Interconnect

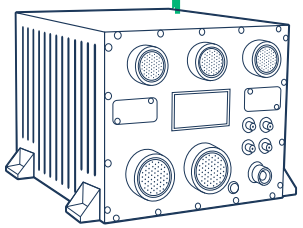


Real/Sim Switch

F(X)



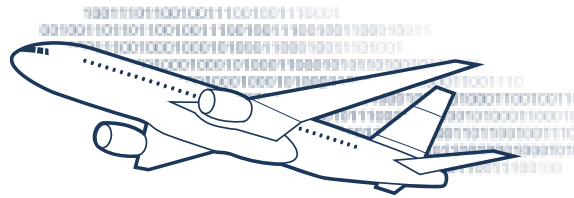
UUT



Cable Harness

Fault

LRU Test Architecture



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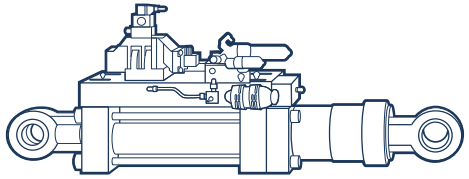

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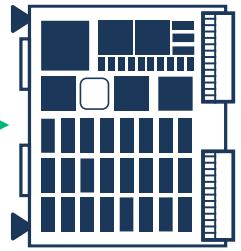

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F(X)

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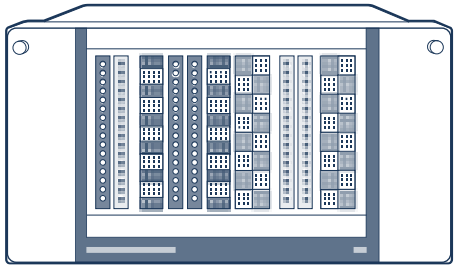
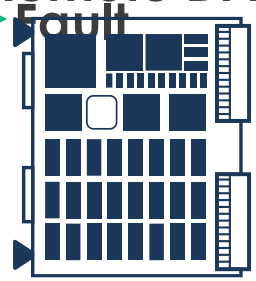


Remote DAQ Fault



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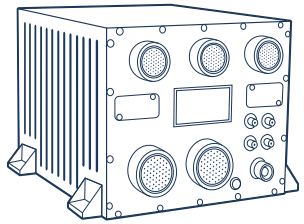
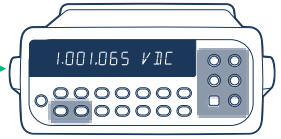


Cable Harness

Sense Lines

Instruments



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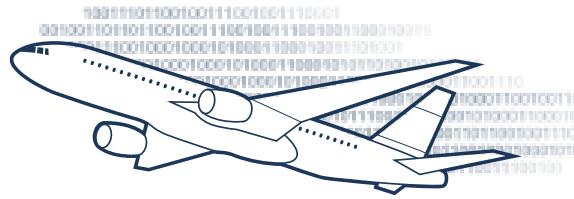

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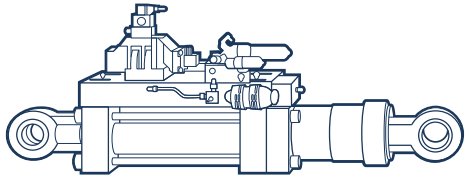
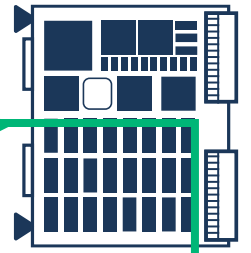


Software Environment and I/O

Real/Sim Switch

F(X)



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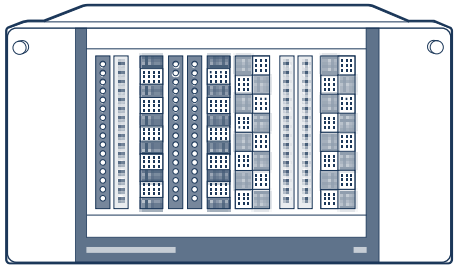
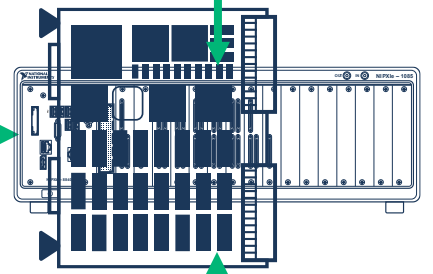
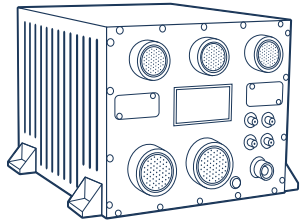


Fault

Remote DAQ



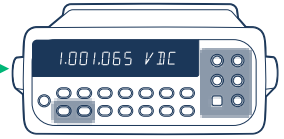
UUT



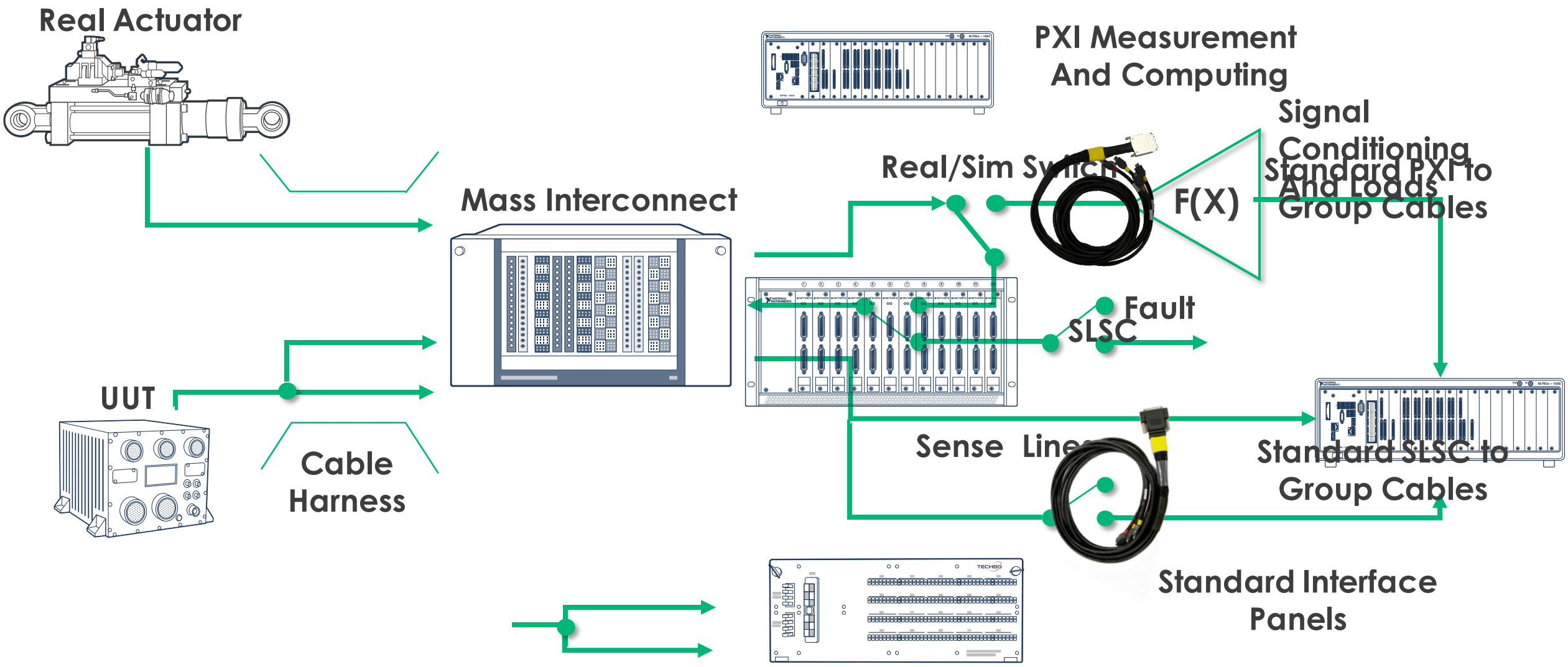
Cable Harness

Sense Lines

Instruments

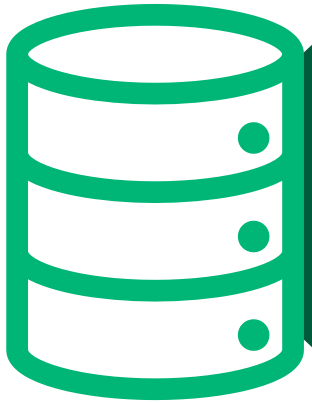


LRU Test Architecture



Automated Workflow

Product ICD & Requirements



Test System Model

- Software Configurations
- System SolidWORKS Models
- End-to-End Documentation
- BOMs & Hardware POs
- System Automated Test Scripts

Standard Signal Library

4.3 BI-DIRECTIONAL
4.3.102 RS-422/RS-485 FULL DUPLEX
COMMUNICATIONS 4

REQUIREMENTS COVERAGE

3.1 INPUT to UUT
3.1.106 INPUT 3-WIRE POTENTIOMETER
SPECIALIZED SENSORS 3

2.2 OUTPUT from UUT
2.2.400 ISOLATED OUTPUT CURRENT +/-20mA
ANALOG 2

1.2 OUTPUT from UUT
1.2.300 OUTPUT DISCRETE HIGH SIDE DRIVER
DISCRETE / DIGITAL 1

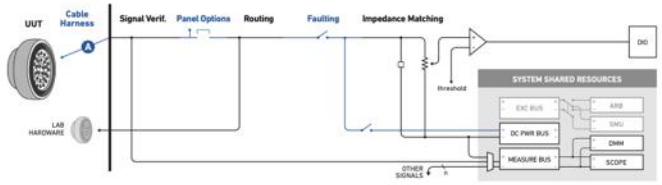
REQUIREMENTS COVERAGE

The UUT drives a signal on Pin A that requires a connection to ground through a load.

SPECIFICATIONS

In/Output Impedance	24 kΩ
Overvoltage Protection	+/-60 V

SCHEMATIC



CONFIGURATION OPTIONS

Signal Verification
- Instrumentation mode
- Continuous monitoring

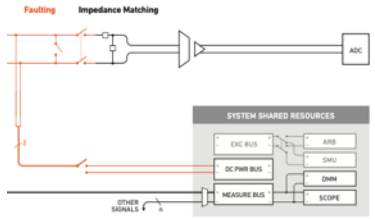
Routing
- Passthrough

Faulting
- Open faulting
- Bus faulting
- Line faulting

Impedance Matching
- Series impedance
- Parallel impedance

SPECIFICATIONS

	+/-20 mA	+/-40 mA
In/Output Impedance	92 Ω	92 Ω
Overvoltage Protection	30 V	30 V
Accuracy	0.13%	0.13%
Resolution	16 bits	16 bits
Max Update Rate	250 kS/s	250 kS/s

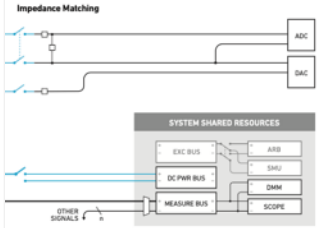


Faulting
- Open faulting
- Bus faulting
- Line faulting

Impedance Matching
- Series impedance
- Parallel impedance

ICATIONS

Impedance	25 mΩ
ive	20 mA
ge Protection	25 V
	0.091%
	16 bits
e Rate	250 kS/s



Impedance Matching
- Series impedance
- Parallel impedance

Type Options
- Transformer type
- Shared excitation
  (lines A, B needed only once per excitation signal)

Impedance Matching
- Series impedance
- Parallel impedance

Impedance Matching
- Series impedance
- Parallel impedance

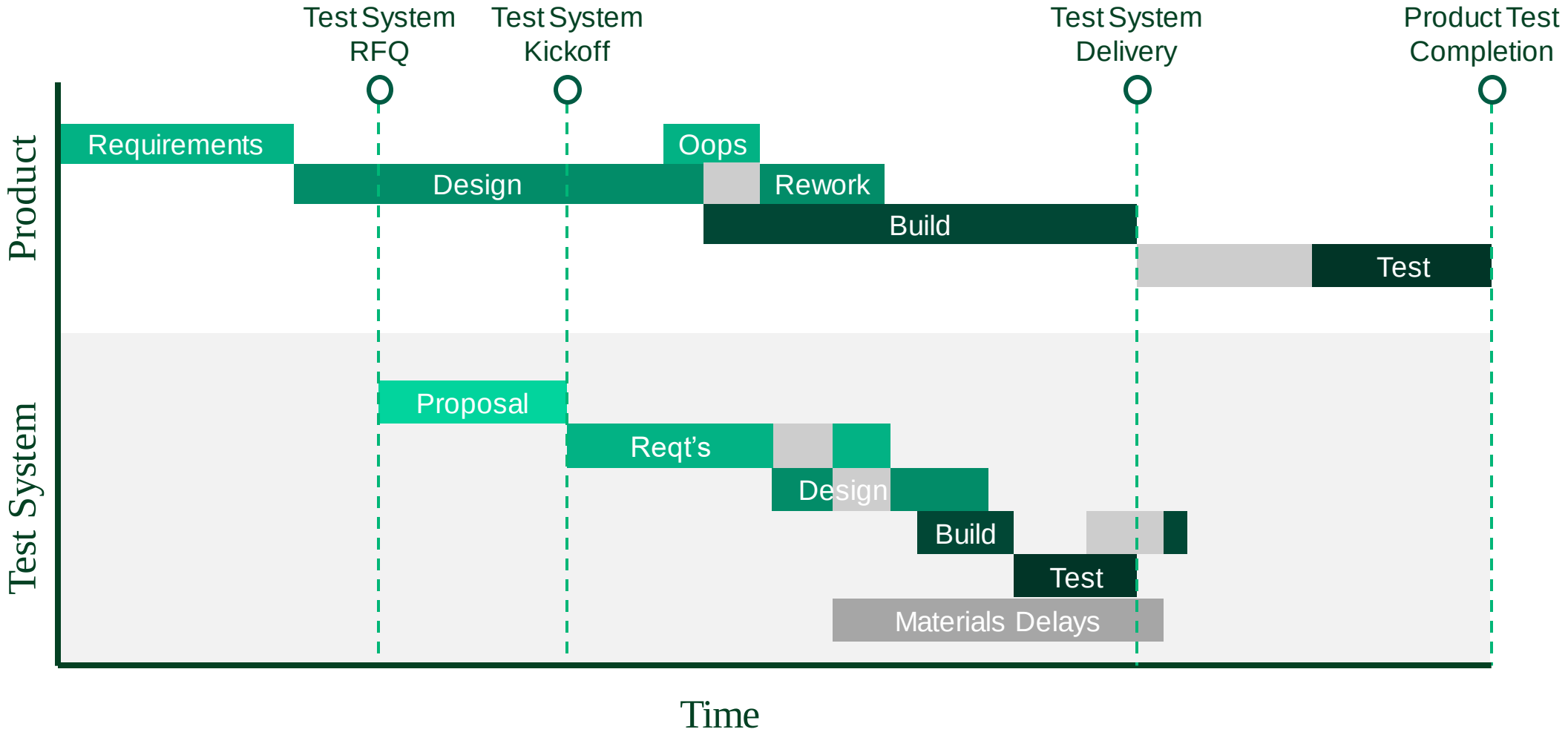
SoD Key Architecture Benefits

- 6 Routing Endpoints
  - Simulation
  - Open/Short/Line Fault
  - Load
  - Real/Sim
  - Parallel DAQ
  - Multiplexed Instrumentation
- Modular Architecture
- Commercial-Off-The-Shelf (COTS) Components
- Automated MBSE Workflow
- Signal Type Library

SoD in a Single Program

- Schedule
- Deliverables
- Maintainability

The Project Schedule



Requirements Discovery & System Design

Lengthy Requirements Discovery Period

- Pre-validated signal types allows for fast requirements mapping
- Modular architecture “black boxing”

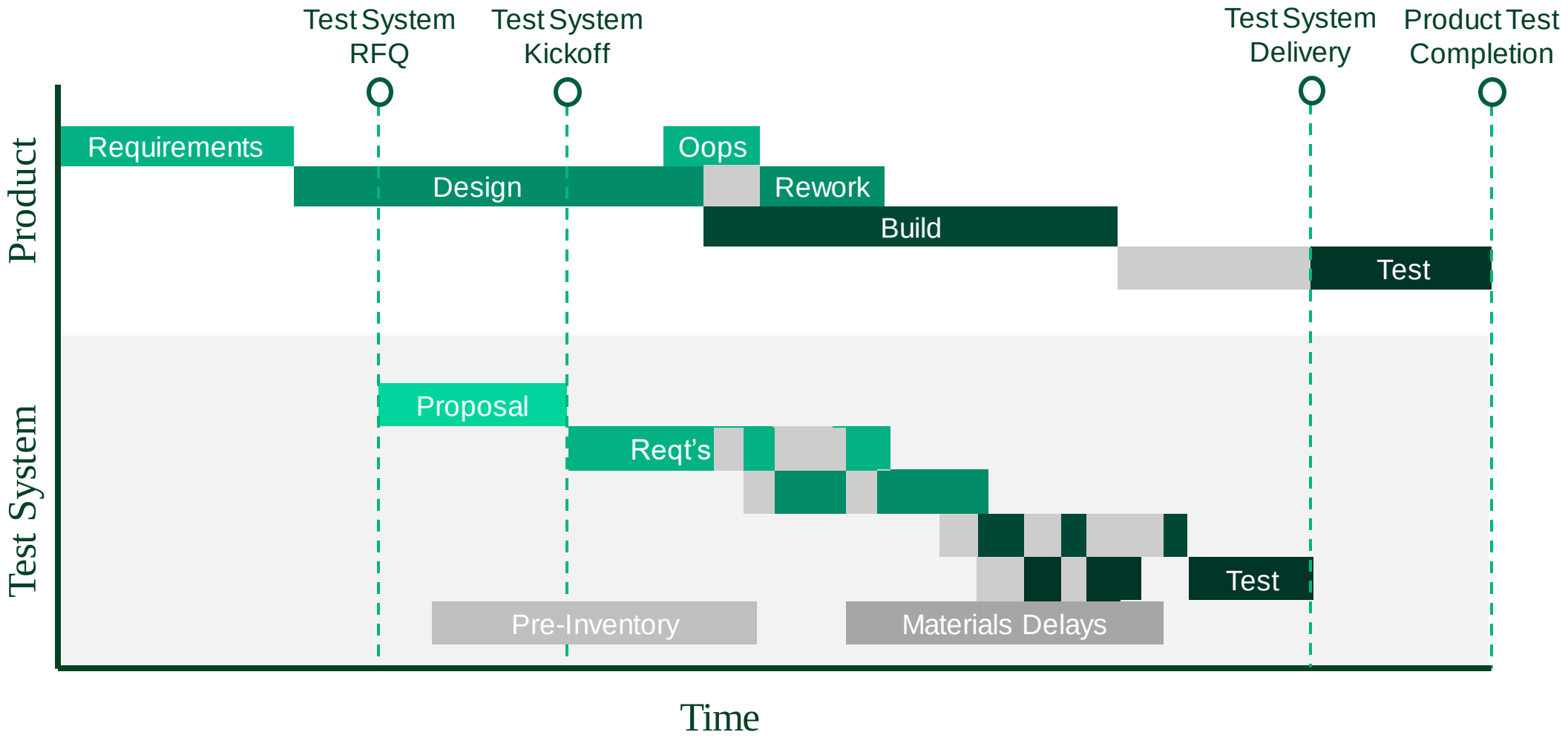
Requirements Churn

- Automated workflow allows for quick integration of requirements changes into the system

Materials Lead Times

- COTS components and standard types means that most system hardware is already known and can be stocked or ordered immediately, saving weeks of schedule

The Project Schedule



System Build & Validation

Documentation and Software Configurations

- Tedious software configurations, switch command sets, and assembly documents can be generated directly from the test system model

Validation of Test System Prior To Shipment

- Multiplexed instrumentation endpoint allows each signal to be directed to high fidelity instrumentation
- Software test scripts for requirements validation scripted directly from model to automatically exercise signal through fault conditions and expected behaviour
- Boilerplate validation scripts based on standard signal types and faulting implementations

UUT Integration & Obsolescence

Integration with Existing Toolchains

- IO server abstraction layer allows integration with existing software test script infrastructure
- Automated software generation allows software integration prior to delivery

System Capability Upgrades

- Modular approach and built-in signal endpoints allows easy addition of new signals or additional faulting or measurement capabilities

Parts Going End-Of-Life

- Easy integration of new hardware into modular architecture allows for for/fit/function upgrades to systems if products reach the end of their lifecycle

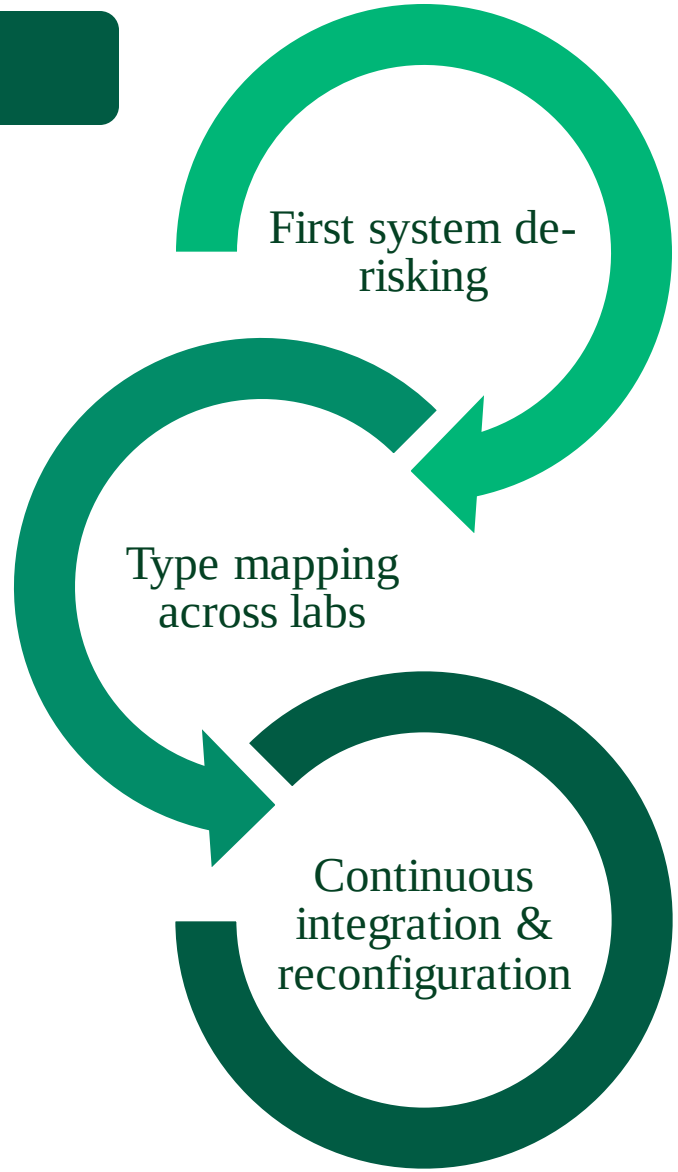
SoD over Multiple Labs

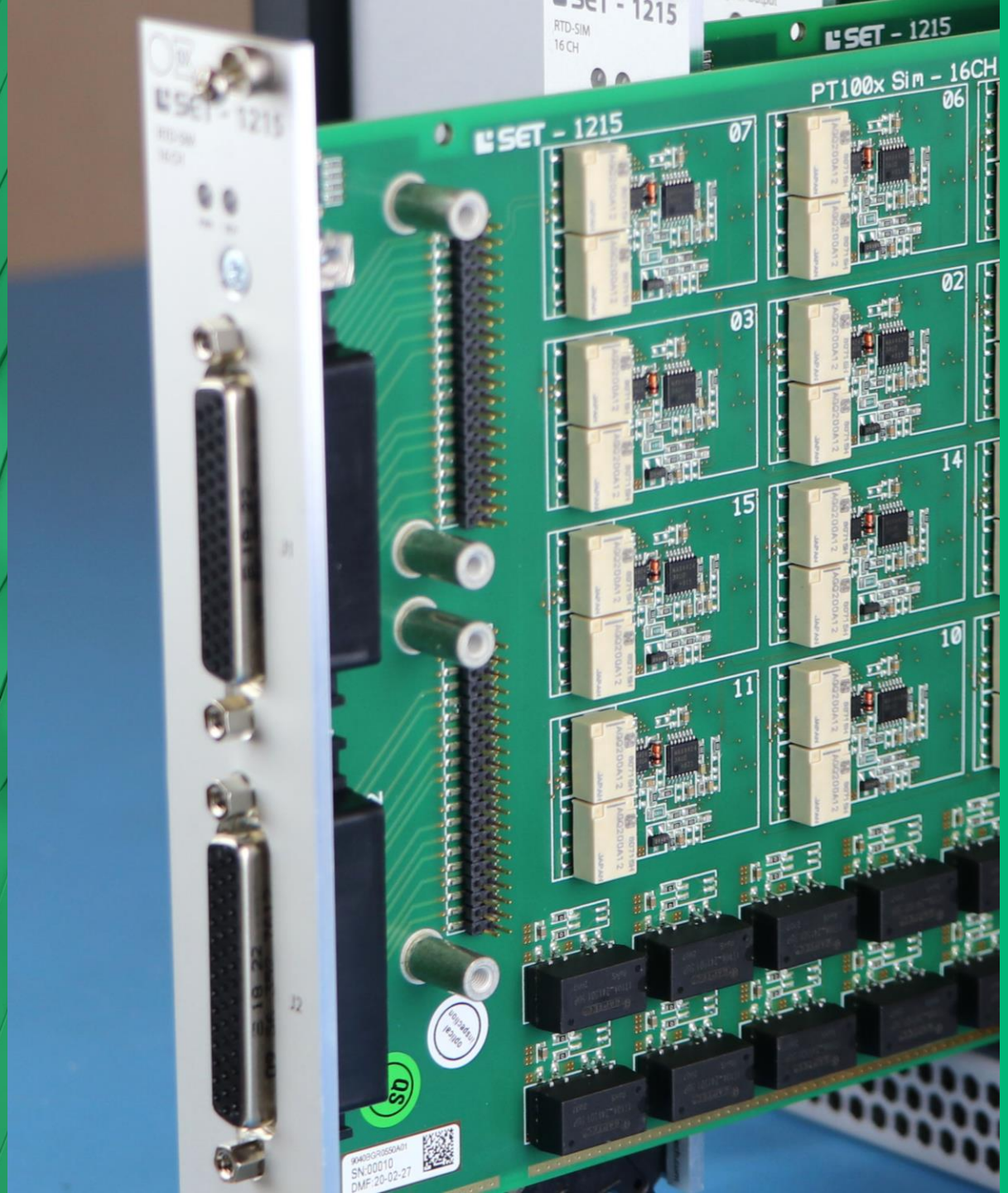
Requirements Mapping

- Product signal types mapped to Tech180 signal types
- New types on past projects can be integrated into standard Tech180 offerings
  - Reduced NRE and de-risking on future test systems

System Reconfiguration

- Commonality of design and type mappings allows for products with similar interfaces to be merged into on test system
- Allows for recapitalization of hardware investments





Summary

- Key benefits of SoD architecture and toolchain
  - 6 Routing Endpoints
    - Simulation
    - Open/Short/Line Fault
    - Load
    - Real/Sim
    - Parallel DAQ
    - Multiplexed Instrumentation
  - Modular Architecture
  - Commercial-Off-The-Shelf (COTS) Components
  - Automated MBSE Workflow
  - Signal Type Library
- Modularity, standardization, and automation allows for rapid development and flexible design

Thank you!

Questions?

Contact Tech180 at info@tech180.us

NI CONNECT