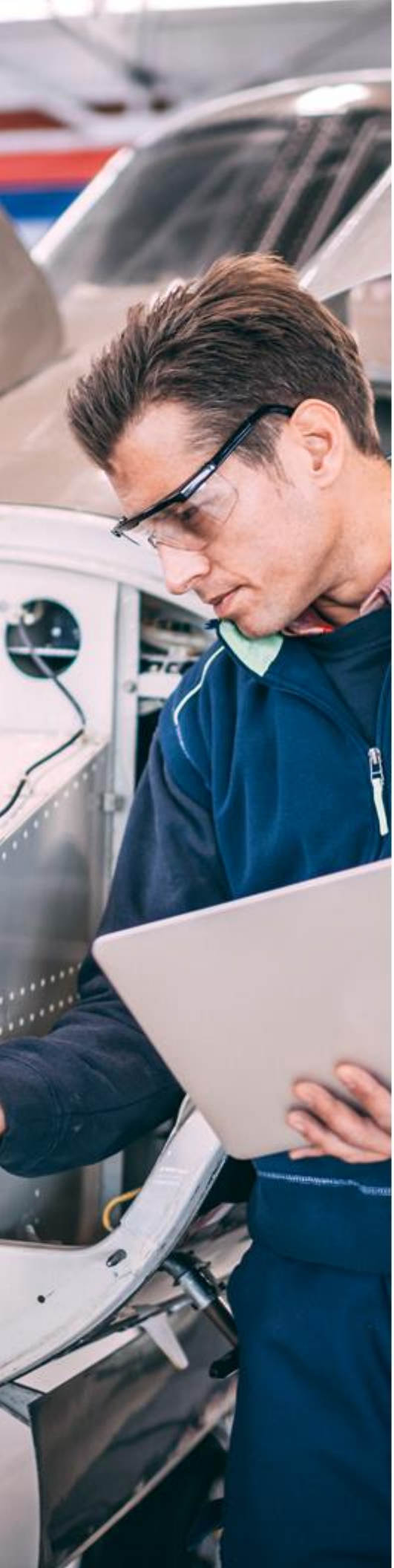
SOLUTION
BROCHURE

# Radar and EW Prototyping with NI COTS Components

ni.com



SOLUTION BROCHURE

# Radar and EW Prototyping with NI COTS Components

# Trends in Radar

Radar systems are experiencing considerable technology disruption because of the rapidly changing electromagnetic battlespace. Active electronically scanned arrays, ultra-wideband technology, and cognitive radar systems present new design and test challenges for even the most experienced organizations.

## Rapidly Prototype Radar Waveforms and Architectures

Threats and countermeasures continue to evolve at a rapid pace. Today, radar must track agile hypersonic weapons, resolve swarms of drones, and detect low-RCS aircraft. Radar system developers are expected to prototype new concepts quickly, such as cognitive techniques or fully digital beamforming, to counteract emerging threats, increase performance and capability, and assure operation in contested EM environments. COTS software defined radios (SDRs) with an integrated software workflow accelerated the transition from concept to testbed to deployed system.

FIGURE 01

Northrop Grumman E-2D Advanced Hawkeye: Airborne Early Warning Command and Control

> "The NI user-programmable FPGA instruments have delivered immediate and striking economic benefits across all project stages, from non-recurring engineering (NRE), to production, to life cycle management. This has led to a total project cost reduction of more than 50 percent."

**Armando Arenai**
NATO Support Agency (NSPA)

# Trends in Electronic Warfare

Spectrum superiority has never been more critical to success on the battlefield. Amid an increasingly contested and congested electromagnetic spectrum, the ability to reliably operate communications and navigation systems while deceiving and disrupting the adversary creates a significant tactical advantage. Software defined radio (SDR) provides the ideal platform for developing and deploying electronic warfare systems and the flexibility to adapt to modern and constantly evolving threats. COTS technology is ideal for system-level test of complex, intelligent EW receivers, reducing the need for flight test hours by modeling and simulating a multi-emitter environment.

## Electronic Attack

Be disruptive. Use COTS SDR to rapidly design and deploy systems that deny hostile access to the electromagnetic spectrum, such as communications jamming and counter-UAS systems.

## Electronic Protection

Be resilient. Prototype systems capable of assured operation in contested and congested electromagnetic spectrum with techniques like cognitive radio and frequency hopping.

## Electronic Support

Be aware. Deploy wideband, multi-channel acquisition systems with robust connectivity capabilities that support multi-domain operational and situational awareness through signals intelligence and direction finding.

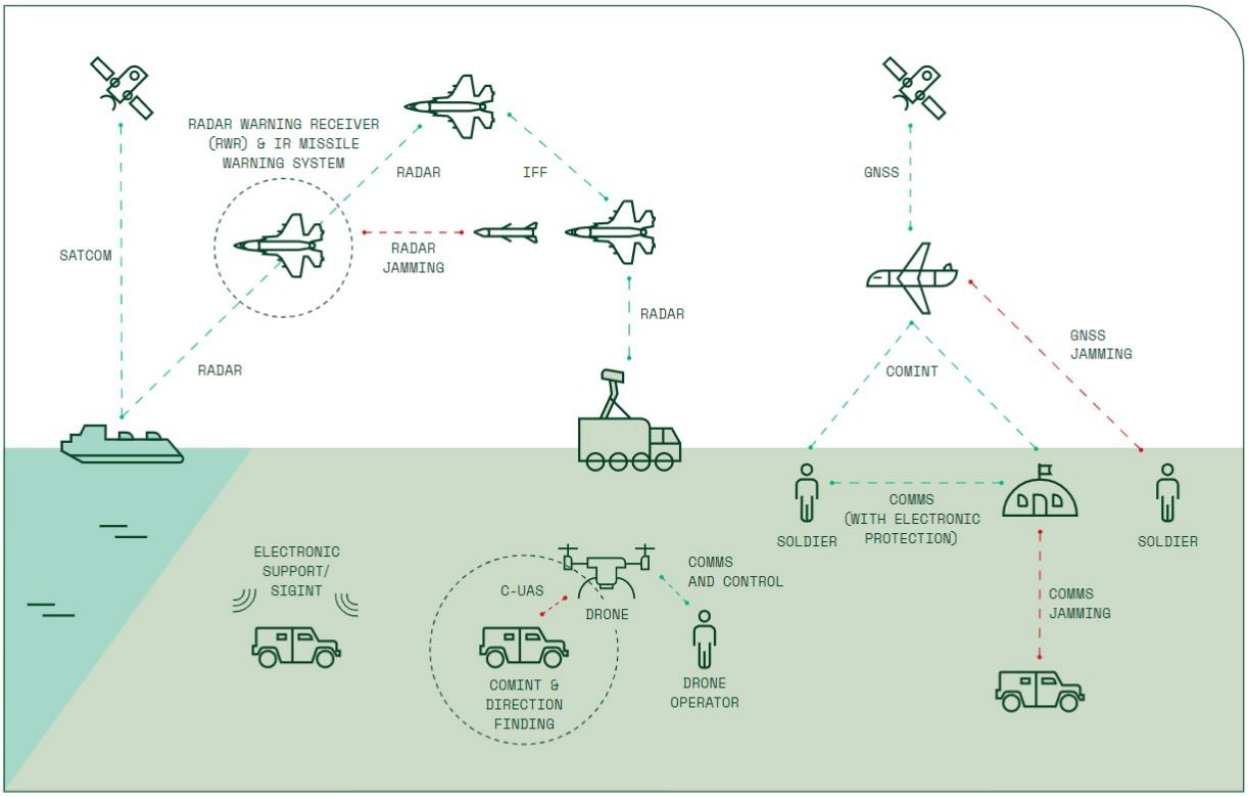



FIGURE 02

The electromagnetic battlefield is ever more contested and congested with radar, communications, navigation, and electronic warfare systems.

# Architectures for Multichannel Radar and EW Research and Prototyping

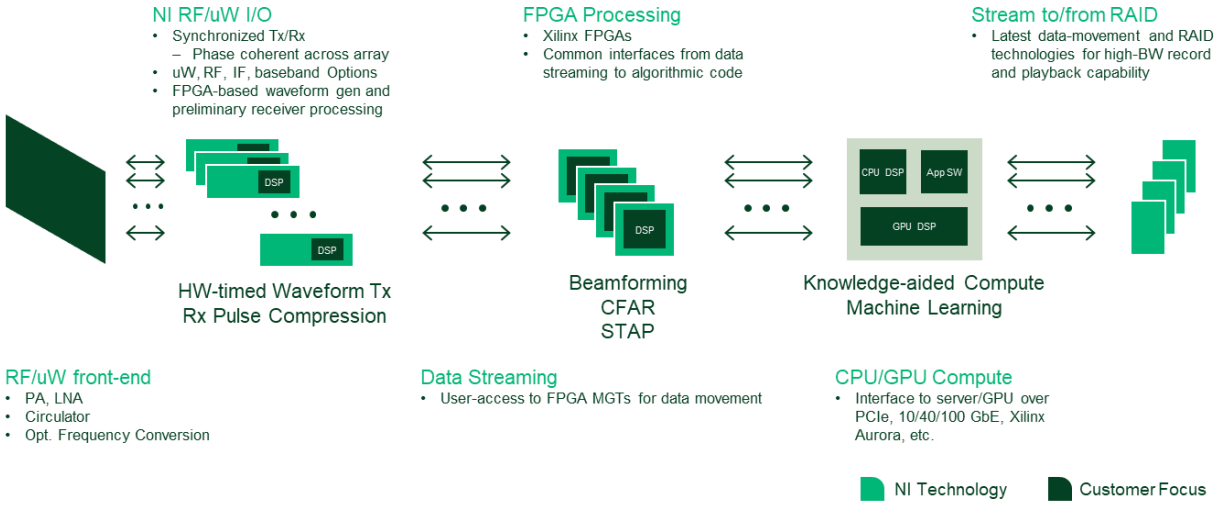



FIGURE 03

Radar researchers can focus more on their novel front end or DSP when the RF I/O, processing modules, and data movement infrastructure are provided by COTS components.

Modern radar systems incorporate capability including cognitive function, multi-channel operation, and machine learning/artificial intelligence. To prototype novel capability for such systems, systems engineers and researchers must work with a COTS platform that allows them to quickly develop a testbed for evaluating new ideas.

**Multichannel Systems**
For accurate ranging and positioning of targets, it is necessary for the transmit (Tx) and receive (Rx) chains of a radar system to be synchronized. For multi-channel systems, this becomes yet more important since multiple Tx and Rx chains must be synchronized across an array. NI COTS modular instruments based on the PXI platform provide phase coherency via the sharing of local oscillators, reference clocks, sampling clocks, and triggers.

**Data Streaming**
Wide bandwidth I/Q data necessitates high throughput streaming interfaces. NI provides users with access to FPGA multigigabit transceivers (MGTs) to avoid bottlenecks in moving data from I/O to processing.

**Digital Signal Processing (DSP)**
Novel capability such as spectral interference avoidance, clutter suppression, and automatic target recognition requires inline processing of radar return signals. NI incorporates Xilinx FPGAs onboard instruments like Vector Signal Transceivers and FlexRIO. This allows engineers and researchers to execute calculations like space-time adaptive processing (STAP), constant false alarm rate (CFAR), and beamforming with hardware-level latency and performance.

**Machine Learning/Knowledge-Aided Computing**
Today's cognitive radar system operates differently from yesterday's. And tomorrow's will operate differently from today's. That's because cognitive radars are constantly learning and evolving, adapting to new targets, new countermeasures, and new channel conditions. Machine learning algorithms make this possible, and so NI provides interfaces to CPU and GPU-based compute servers via PCI Express, 100 GbE, and Xilinx Aurora, to enable cognitive capability.

**Data Storage**
Large-volume and high-speed data storage is necessary for writing wide bandwidth I/Q data to disk for post-processing or playback.

# NI PXI

Powered by software, PXI is a rugged PC-based platform for measurement and automation systems. PXI combines PCI electrical bus features with the modular Eurocard packaging of CompactPCI and then adds specialized synchronization buses and key software features. PXI is both a high-performance and low-cost deployment platform for applications such as manufacturing test, military and aerospace, machine monitoring, automotive, and industrial test.

PXI systems are composed of three main hardware components: chassis, controller, and peripheral modules. The hardware systems are driven by software, often with individual portions of LabVIEW, C/C++, .NET, or Python code.

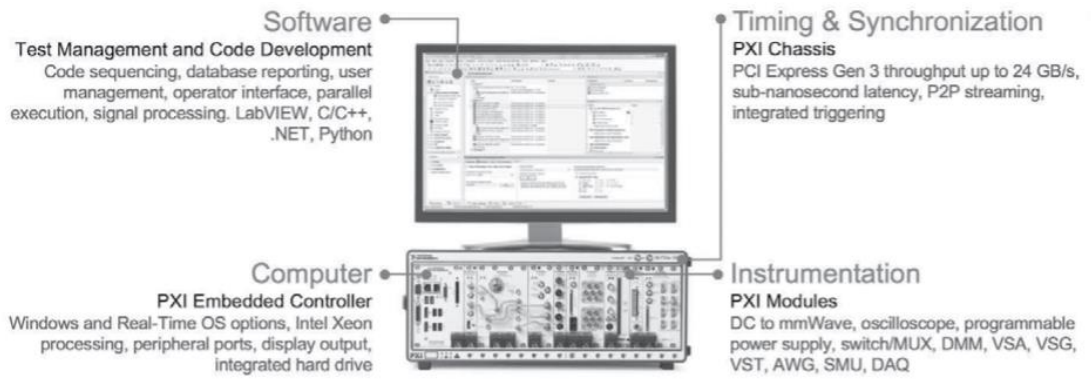



FIGURE 04

PXI systems consist of a chassis with synchronization and streaming, controller for CPU-based computing, and instrumentation for I/O and FPGA-based processing.

## PXI Chassis

The PXI chassis is the backbone of a PXI system and compares to the mechanical enclosure and motherboard of a desktop PC. It provides power, cooling, and a communication bus to the system, and supports multiple instrumentation modules within the same enclosure. PXI uses commercial PC-based PCI and PCI Express bus technology while combining rugged CompactPCI modular packaging, as well as key timing and synchronization features. Chassis range in size from two to 18 slots to fit the needs of any application, whether its intentions are to be a portable, a benchtop, a rack-mount, or an embedded system.

FIGURE 05

PXI chassis range in size, data movement bandwidth, cooling capacity, power, and clock types.

## Timing and Synchronization

One of the key advantages of a PXI system is the integrated timing and synchronization. A PXI chassis incorporates a dedicated 10 MHz system reference clock, PXI trigger bus, star trigger bus, and slot-to-slot local bus to address the need for advanced timing and synchronization. These timing signals are dedicated signals in addition to the communication architecture. The 10 MHz clock within the chassis can be exported or replaced with a higher stability reference. This allows the sharing of the 10 MHz reference clock between multiple chassis and other instruments that can accept a 10 MHz reference. By sharing this 10 MHz reference, higher sample rate clocks can phase-lock loop (PLL) to the stable reference, improving the sample alignment of multiple PXI instruments. In addition to the reference clock, PXI provides eight transistor-transistor logic (TTL) lines as a trigger bus. This allows any module in the system to set a trigger that can be seen from any other module. Finally, the local bus provides a means to establish dedicated communication between adjacent modules.

Building on PXI capabilities, PXI Express also provides a 100 MHz differential system clock, differential signaling, and differential star triggers. By using differential clocking and synchronization, PXI Express systems benefit from increased noise immunity for instrumentation clocks and the ability to transmit at higher frequency rates. PXI Express chassis provide these more advanced timing and synchronization capabilities in addition to all the standard PXI timing and synchronization signaling.

In addition to the signal-based methods of synchronizing PXI and PXI Express, these systems can also leverage synchronization methods using absolute time. A variety of sources including GPS, IEEE 1588, or IRIG can provide absolute time with the use of an additional timing module. These protocols transmit time information in a packet so systems can correlate their time. PXI systems have been deployed over large distances without sharing physical clocks or triggers. Instead, they rely on sources such as GPS to synchronize their measurements.

# PXI I/O Options for Radar and EW Research and Prototyping

| SPEC | PXIE-5832 VST | PXIE-5841 VST | PXIE-5785 FLEXRIO | PXIE-5764 FLEXRIO | PXIE-5668 VSA |
|---|---|---|---|---|---|
| Instrument Type | Transceiver | Transceiver | Transceiver | Digitizer | Vector Signal Analyzer |
| RF Architecture | Direct Conversion | Direct Conversion | Direct Sampling | Direct Sampling | Superheterodyne |
| Channel Count | 1 Tx; 1 Rx | 1 Tx; 1 Rx | 2 Tx; 2 Rx | 4 Rx | 1 Rx |
| Frequency Coverage | 5 – 21 GHz; 23 – 44 GHz | 9 kHz – 6 GHz | 6 GHz Rx; 2.85 GHz Tx | 400 MHz | 20 Hz – 26.5 GHz |
| Instantaneous Bandwidth* | 1 GHz | 1 GHz | 2.5 GHz | 400 MHz | 765 MHz |
| Synchronization Architecture | LO Sharing; 10 MHz; Hardware Start Trigger; Sample Clock Alignment | LO Sharing; 10 MHz; Hardware Start Trigger; Sample Clock Alignment | Ref Clock Sharing; Sample Clock Alignment; Hardware Start Trigger | Ref Clock Sharing; Sample Clock Alignment; Hardware Start Trigger | LO Sharing; 10 MHz; Hardware Start Trigger; Sample Clock Alignment |
| Backend Data Interface | PCIe Gen 3 x8 | PCIe Gen 3 x8 | PCIe Gen 3 x8 | PCIe Gen 3 x8 | PCIe Gen 2 x8 |
| Single Module Backplane Streaming Performance* | 1 GHz IBW | 1 GHz IBW | 1.25 GHz IBW | 1.25 GHz IBW | 765 MHz IBW |
| Front Panel Data Interface | x4 GTH Transceivers | x4 GTH Transceivers | x4 GTH Transceivers | x4 GTH Transceivers | n/a |
| Specification Type | Warranted w/ Calibration Service | Warranted w/ Calibration Service | Typical | Typical | Warranted w/ Calibration Service |
| Relative Cost Per Channel | $$$ | $$$ | $$ | $ | $$$ |

TABLE 01

PXI-based I/O modules for radar and EW prototyping include transceivers, digitizers, and vector signal analyzers.

* Consult individual product specification documents for frequency plan
** Performance for multichannel systems will be limited by system throughput

## PXIe-5841 Vector Signal Transceiver

**6 GHz, 1 GHz Bandwidth, RF PXI Vector Signal Transceiver**—The PXIe-5841 is a vector signal transceiver (VST) with 1 GHz of instantaneous bandwidth. It combines vector signal generator, vector signal analyzer, and high-speed serial interface capabilities with FPGA-based real-time signal processing and control. The PXIe-5841 features the flexibility of a software defined radio architecture with RF instrument class performance. This VST delivers the fast measurement speed and small form factor of a production test box with the flexibility and high performance of R&D-grade box instruments.

## PXIe-5832 Vector Signal Transceiver

**44 GHz, 1 GHz Bandwidth, mmWave PXI Vector Signal Transceiver**—The PXIe-5832 provides FPGA-based processing and the combined functionality of a vector signal analyzer and a vector signal transceiver. You can use the PXIe-5832 to perform stimulus and response measurements in the 5 GHz to 21 GHz and the 22.5 GHz to 44 GHz frequency ranges. Additionally, the PXIe-5832 features multiport configuration options that integrate solid-state mmWave switching to the 22.5 GHz to 44 GHz frequency range.


## PXIe-5785 FlexRIO IF Transceiver

**12-Bit, 6.4 GS/s, 2-Channel PXI FlexRIO IF Transceiver**—The PXIe-5785 enables direct RF acquisition up to 6 GHz and generation up to 3 GHz with 12 bits of resolution. You can use it in a dual-channel mode at 3.2 GS/s or in a single-channel interleaved mode at 6.4 GS/s. The PXIe-5785 is ideal for applications that require wideband acquisition and generation with multichannel synchronization, including radar, electronic warfare, and communications. The FlexRIO driver includes support for acquiring and generating waveforms out of the box, and you can use the LabVIEW-programmable Xilinx Kintex UltraScale FPGA to implement custom algorithms for real-time signal processing.


## PXIe-5764 FlexRIO Digitizer

**16-Bit, 1 GS/s, 4-Channel PXI FlexRIO Digitizer**—The PXIe-5764 is a PXI FlexRIO digitizer that simultaneously samples four channels at 1 GS/s with 16 bits of resolution and features 400 MHz of analog input bandwidth. With up to 70 dB of SNR, the PXIe-5764 is ideal for applications that require a wide dynamic range with a wideband digitizer. The FlexRIO driver includes support for finite and continuous streaming modes, and you can implement custom algorithms and real-time signal processing on the LabVIEW-programmable Xilinx Kintex UltraScale FPGA. Available in AC and DC coupled variants, the PXIe-5764 is ideal for both time and frequency domain applications, including radar, EW, and communications prototyping.

## PXIe-5668 Vector Signal Analyzer

**Up to 26.5 GHz PXI Vector Signal Analyzer**—The PXIe-5668 offers wide bandwidth with high-performance measurement performance and speed. It meets the challenging requirements of applications such as wireless communications, radio frequency integrated circuit characterization, radar test, and spectrum monitoring and signal intelligence. With its implementation as a PXI instrument, the PXIe-5668 also features the fast measurement speed required for high-volume manufacturing test, and multi-instrument synchronization capabilities for phase-coherent MIMO test. You can use the optionally included PXIe-5698 preamplifier to improve dynamic range and sensitivity near the instrument noise floor.

# PXI-Based FPGA Processing Modules

PXI-based FPGA processing modules feature high-performance FPGAs that add signal processing capability to PXI systems. These modules leverage the latest FPGAs from Xilinx, streaming technologies such as PCI Express, and NI Peer to Peer Streaming for high-bandwidth data communication with other modules over the backplane. When paired with another PXI device, such as a PXI Vector Signal Transceiver, coprocessor modules provide the additional FPGA resources required to run complex techniques and algorithms such as space-time adaptive processing (STAP), constant false alarm rate (CFAR), and beamforming in real-time.

## PXIe-6593/4 High-Speed Serial Instruments

**PXIe-6593—16 Gbps, 8-Channel PXI High-Speed Serial Instrument**
**PXIe-6594—28 Gbps, 8-Channel PXI High-Speed Serial Instrument**
PXI High-Speed Serial Instruments include a user-programmable FPGA with access to multigigabit transceivers to implement various standard and custom high-speed serial protocols. They are programmable in LabVIEW FPGA for maximum application-specific customization and reuse. PXI High-Speed Serial Instruments also benefit from PXI clocking, triggering, and high-speed data movement capabilities, including streaming to and from disk as well as peer-to-peer streaming.

## PXIe-7915 FPGA Coprocessor

**KU060 FPGA, 4 GB DRAM, x8 Gen 3 PXI Coprocessor Module**—The PXIe-7915 provides a Xilinx Kintex UltraScale FPGA that you can program with LabVIEW or Xilinx Vivado to add signal-processing capabilities to PXI Express systems. Using the x8 Gen 3 PCI Express architecture and peer-to-peer streaming, PXI FlexRIO Coprocessor Modules can stream data to and from other modules in a PXI chassis at up to 7 GB/s without a host controller. You can pair these modules with another PXI instrument, such as a PXI Vector Signal Transceiver, to add functionality, such as running complex algorithms in real-time. The PXIe-7915 KU060 FPGA is ideal for RF applications that require a substantial amount of signal processing.

## ATCA-3671

**Quad Virtex-7 690T FPGA Module for ATCA**—The ATCA-3671 features four user-programmable Virtex-7 690T FPGAs. It has four slots for both analog and high-speed serial I/O options. The ATCA-3671 is ideal for applications that require significant amounts of real-time signal processing including algorithm research, prototyping, and field trials. The ATCA-3671 is programmable with the LabVIEW FPGA Module.

# USRP Software Defined Radios

NI USRP devices are software defined radios (SDRs) that combine host-based processors, FPGAs, and RF front ends to help you rapidly design, prototype, and deploy wireless systems. The USRP product line offers a wide breadth of SDRs ranging from lower-cost options with fixed FPGA personalities to high-end radios with large, open FPGAs and up to 160 MHz of instantaneous bandwidth.

USRP SDRs are ideal for developing and prototyping complex wireless designs. After you design and simulate your digital signal processing (DSP) algorithms, you need to prototype in a real-world environment to ensure you deliver high-quality technology to market on time. The powerful processing capability of onboard FPGAs is especially beneficial for applications that require processing wide bandwidths of data in real time. USRP SDRs are also well suited for applications like spectral monitoring and direction finding because of their wide bandwidths and flexible RF front ends. On select models, an onboard x86 processor creates a complex yet powerful USRP that you can use as a stand-alone radio.

**NI recommends the N320 and N321 SDRs for multichannel radar/EW prototyping, due to the ability to share local oscillators for phase coherency across an array.**

## USRP N320 / N321 Software Defined Radios

The USRP N320 and N321 are networked software defined radios that provides reliability and fault-tolerance for deployment in large scale and distributed wireless systems. They are high performance SDRs that use a unique RF design by Ettus Research to provide 2 Rx and 2 Tx channels in a half-wide RU form factor. Each channel provides up to 200 MHz of instantaneous bandwidth, and covers a frequency range from 3 MHz to 6 GHz. The baseband processor uses the Xilinx Zynq-7100 SoC to deliver a large user programmable FPGA for real-time, low latency processing and a dual-core ARM CPU for stand-alone operation.

Support for 1 GbE, 10 GbE, and Aurora interfaces over two SFP+ ports and 1 QSFP+ port enables high throughput IQ streaming to a host PC or FPGA coprocessor. A flexible synchronization architecture with support for LO sharing for TX and RX, 10 MHz clock reference, PPS time reference, GPSDO, and White Rabbit enables implementation of phase coherent MIMO configurations. The USRP N320/1 leverages recent software developments in UHD to simplify control and management of multiple devices over the network with the unique capability to remotely administrate tasks such as debugging, updating software, rebooting, resetting to factory state, and monitoring system health.

The USRP N321 features 2 four-way power splitters for distributing an LO signal to other USRP N32x units in a multi-USRP system.

The USRP N321 and N320 modules are the radios used in NI's **Open Architecture for Radar and EW Research**, which provides an accelerated starting point for building a radar/EW prototyping testbed.

| | USRP B2XX | USRP N310 / N32X | USRP X310 | USRP E320 | USRP X410 |
|---|---|---|---|---|---|
| Frequency | 70 MHz – 6 GHz | 3 MHz – 6 GHz (N32X)<br>10 MHz – 6 GHz (N310) | *10 MHz – 6 GHz | 70 MHz – 6 GHz | 1 MHz – 7.2 GHz |
| Bandwidth | 56 MHz | 200 MHz (N32X)<br>100 MHz (N310) | *160 MHz | 56 MHz | 400 MHz |
| Channels | 2 Tx, 2 Rx | 2 Tx, 2 Rx (N32X)<br>4 Tx, 4 Rx (N310) | 2 Tx, 2 Rx<br>*4 Rx (TwinRx) | 2 Tx, 2 Rx | 4 Rx, 4 Tx |
| RF Performance | Good | Best | Best | Good | Better |
| Architecture | Integrated | Integrated | *Configurable w/ Daughterboards | Integrated | Integrated |
| Communication | USB | 10 GbE or PCIe | 10 GbE or PCIe | 10 GbE | 100/10/1 GbE or PCIe |
| Synchronization | 2x2 MIMO | Up to 128x128 (N32X) Full Phase Synchronization | *2x2 MIMO | 2x2 MIMO | 4x4 MIMO |
| SW Support | GNU Radio, C++, Python, MATLAB®, LabVIEW | GNU Radio, C++, Python, MATLAB, RFNoC | GNU Radio, C++, Python, MATLAB, RFNoC, LabVIEW, LabVIEW FPGA | GNU Radio, C++, Python, MATLAB, RFNoC | GNU Radio, C++, Python, RFNoC, LabVIEW *Q4 2021 |
| Key Features | Low SWaP-C, Highly portable | Stand Alone, Wide bandwidth, Multi-Channel Sync Ready (N32X) | *Configurable RF Front End, Programmable FPGA | Low-SWaP, Embedded Deployable, Standalone | RFSOC Based, 5G Ready, Wide Band, Multi-Channel |

## TABLE 02

USRP SDRs range from low-SWaP (size, weight, and power) to high-performance, and can be used for radar and EW prototyping. NI recommends the N320 and N321 SDRs for multichannel radar/EW prototyping, due to the ability to share local oscillators for phase coherency across an array.

# Open Architecture for Radar and EW Research

The Open Architecture for Radar and EW Research is NI's blueprint for a system that meets key requirements of a hardware testbed for prototyping novel radar and EW technology. Follow NI's recommended solution to build up a multi-channel radar/EW research system as quickly as possible; this reference architecture has been validated by NI engineers to ensure it delivers the specified performance. Based on COTS hardware and open-source software, this solution is ideal for rapidly transitioning radar IP through its development life cycle: from software simulation to proof-of-concept demonstration to tactical deployment.

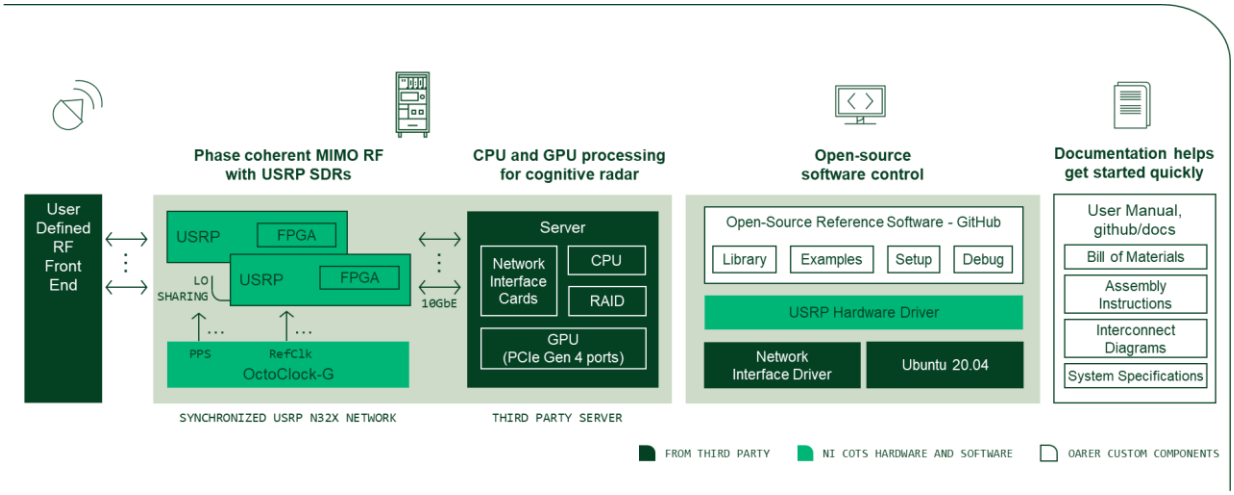



FIGURE 06

Open Architecture for Radar and EW Research system overview, including hardware, software, and documentation.

## Key Specifications & Features

- Direct conversion RF sampling
- Up to 200 MHz instantaneous bandwidth per channel
- 3 MHz – 6 GHz total RF frequency coverage
- Phase coherent operation via shared local oscillator, PPS, and 10 MHz reference clock signals
- Scalable multi-channel architecture
- Controlled with open-source software
- Up to 33.33 MSp/s on 32 channels simultaneously—streaming received data to disk or memory
- CPU and FPGA processing nodes
- Open PCIe slots for user customization
- Ideal for both over-the-air (OTA) and cabled operation

# Reusing IP Throughout the Development Cycle

Workflows that allow researchers and systems engineers to migrate IP from simulation to prototyping testbed to mission hardware can save many hours of code rewrites.

## Migrating Simulation IP to a Prototyping Testbed

Traditionally, moving algorithmic IP from simulation into hardware has been anything but simple. Code must be rewritten to:

- Run optimally across multiple computing architectures, such as FPGAs and GPUs
- Account for data movement between RF/digital instrumentation and heterogeneous processors
- Operate within real-time latency constraints
- Consider real-world imperfections and parametrics

With the right tools and some planning, you can accelerate the process of moving into hardware. Together, NI and MathWorks offer many routes from modeling and simulation to testbed.

There are several ways to call MATLAB from LabVIEW:

- Interfaces for MATLAB—These are documents in which you define calls to a MATLAB file in your G dataflow application. When the application is executed, the MATLAB interface invokes MATLAB: Input data passes from the LabVIEW diagram to the MATLAB file for execution, then data is subsequently returned to the diagram.
- MATLAB Script Node—These nodes are added to a LabVIEW block diagram and invoke the MATLAB software script server to execute scripts written in MATLAB language syntax.
- Call Library Function Node—This method can be especially useful if you do not have access to a MATLAB license. Create a DLL from MATLAB, then call it in LabVIEW using the Call Library Function Node.

In addition to linking NI and MathWorks software, there are more direct methods of targeting NI and Ettus Research Universal Software Radio Peripheral (USRP) SDR devices from MATLAB or Simulink. HDL Coder is a tool that generates portable, synthesizable VHDL and Verilog code from MATLAB functions and Simulink models. You can integrate the generated HDL code into LabVIEW FPGA designs to rapidly introduce into hardware testbeds with real-world inputs and outputs. With correct planning and execution, this is a more efficient way to reuse algorithmic IP from software simulations. You then can utilize IP migrated into LabVIEW FPGA within a testbed built upon NI COTS FPGA-based hardware such as FlexRIO, USRP devices, or Vector Signal Transceivers.

When developing code, you should follow the principles discussed in Importing HDL Coder™ Exports into LabVIEW FPGA Designs. This document covers how to import an example model or algorithm written in MATLAB or Simulink, generate VHDL using HDL Coder, import into LabVIEW FPGA, and test on NI FPGA hardware connected to real-world inputs and outputs.

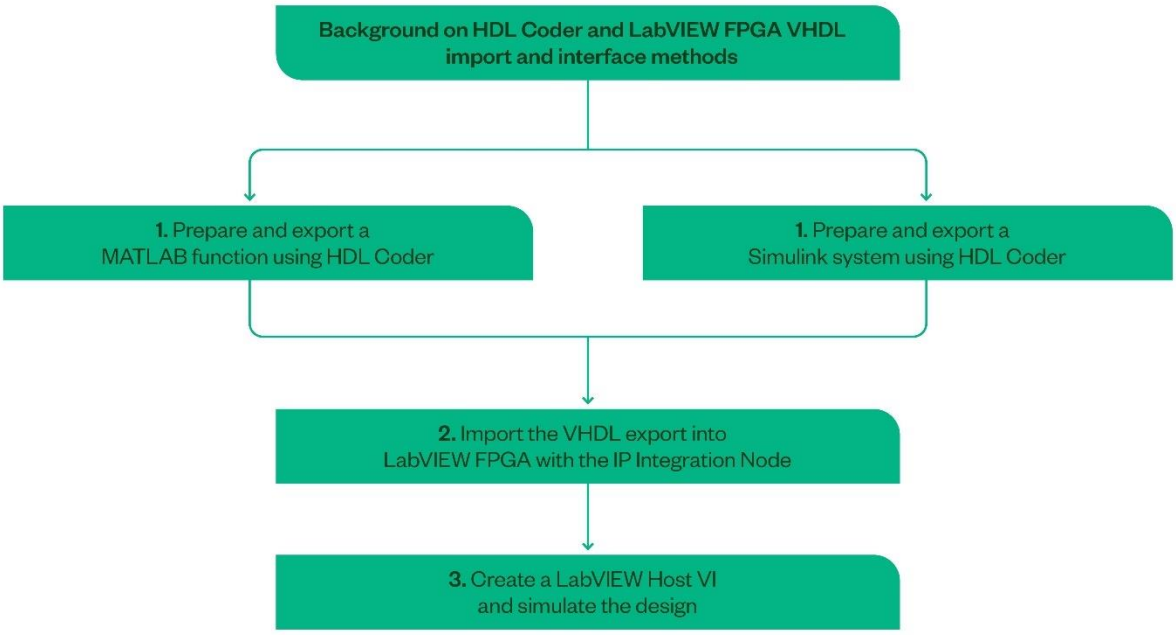



FIGURE 07

Process for importing HDL Coder Exports into LabVIEW FPGA Designs

## Exporting LabVIEW FPGA VIs as Vivado Design Suite Projects

The LabVIEW FPGA Module provides an option to export an FPGA VI as a Vivado Design Suite project. This option allows you to design the exported project and compile it into a bitfile in the Vivado Design Suite. You can then run the bitfile on an FPGA target, such as a Kintex-7 FlexRIO target or a high-speed serial instrument, in the LabVIEW FPGA Module. This option takes advantage of the design features provided by the Vivado Design Suite while making full use of NI FPGA hardware resources.

Follow this how-to guide for more information:
https://zone.ni.com/reference/en-XX/help/371599P-01/lvfpgahelp/export_fpga_vis_howto/

## Converting LabVIEW FPGA VIs into VHDL Code

An FPGA VI can be exported as an encrypted netlist or plain text VHDL code using the NI LabVIEW FPGA IP Export Utility. This utility can be used to export your algorithm, allowing it to be integrated into your Vivado project and used on any Xilinx FPGA device of the same family. The LabVIEW FPGA IP Export Utility provides the following editions:

- LabVIEW FPGA Netlist Export Utility—Exports an FPGA algorithm as an encrypted netlist.
- LabVIEW FPGA VHDL Export Utility—Exports an FPGA algorithm as an encrypted netlist or plaintext VHDL.

# Assessing Radar Algorithms and Systems with Target Generation

Radar target generators are typically used to test radar subsystems in the validation stage of development. They can also be a useful tool for assessing the performance of enhancements to algorithms and waveforms in a prototyping testbed.

NI radar target generators allow you to simulate real-world test scenarios to efficiently evaluate your radar under numerous conditions, considerably reducing the time spent in costly field trials and flight tests. Unlike target generators built with custom hardware, NI systems are open to the customer, and designed and built upon instrument-grade hardware using LabVIEW and LabVIEW FPGA development platforms, known for their easy-to-use data acquisition/generation and analysis capabilities.

- Simulate multiple targets with individual position, velocity, and attitude
- Apply per-target delay, attenuation, Doppler shift, and RCS modelling
- Implement models for atmospheric propagation, terrain clutter, and multipath

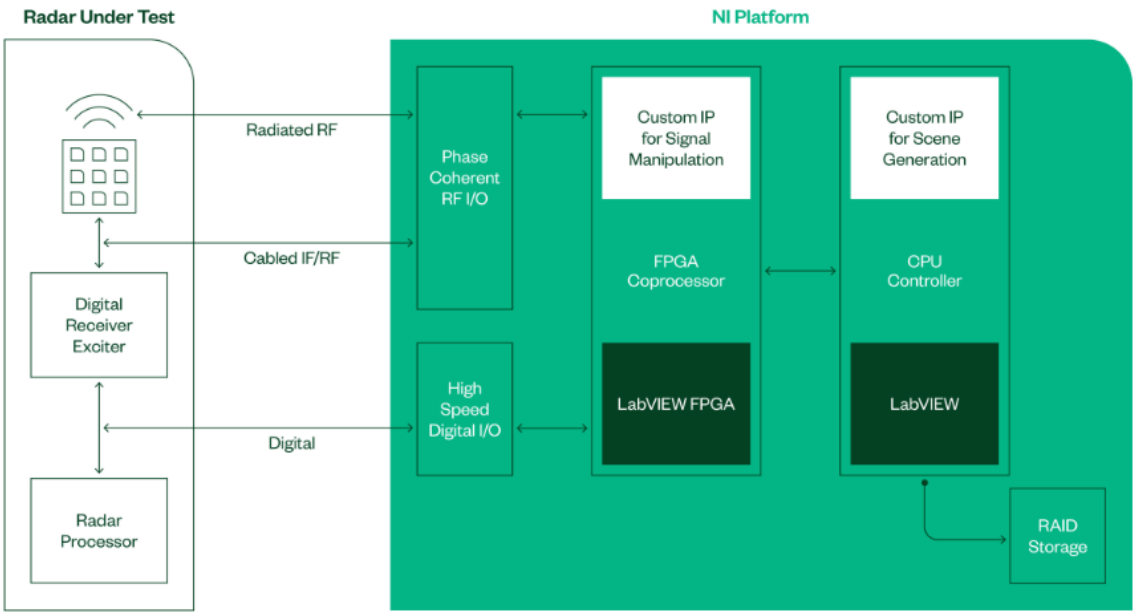
Phase-coherent multichannel RF acquisition and generation with sub-nanosecond synchronization on NI Vector Signal Transceivers

Closed-loop, low-latency scenario simulation with real-time signal processing with NI FlexRIO user-programmable FPGA modules

Modular I/O platform provides flexibility to interface at multiple test points: high-speed digital, direct-inject IF, over-the-air RF

**Key Features**

- Scale system resources as required to meet the channel count, I/O types, signal processing needs of your application
- Leverage a proven software and hardware infrastructure to minimize development time and costs
- Create custom, user-owned IP for target generation, scenario management, signal propagation, and jamming
- Upgrade software and hardware to add new features when you need them to quickly meet evolving test requirements
- Record results to the cloud or local RAID as full I/Q spectral data, parameterized results, or measurement metrics



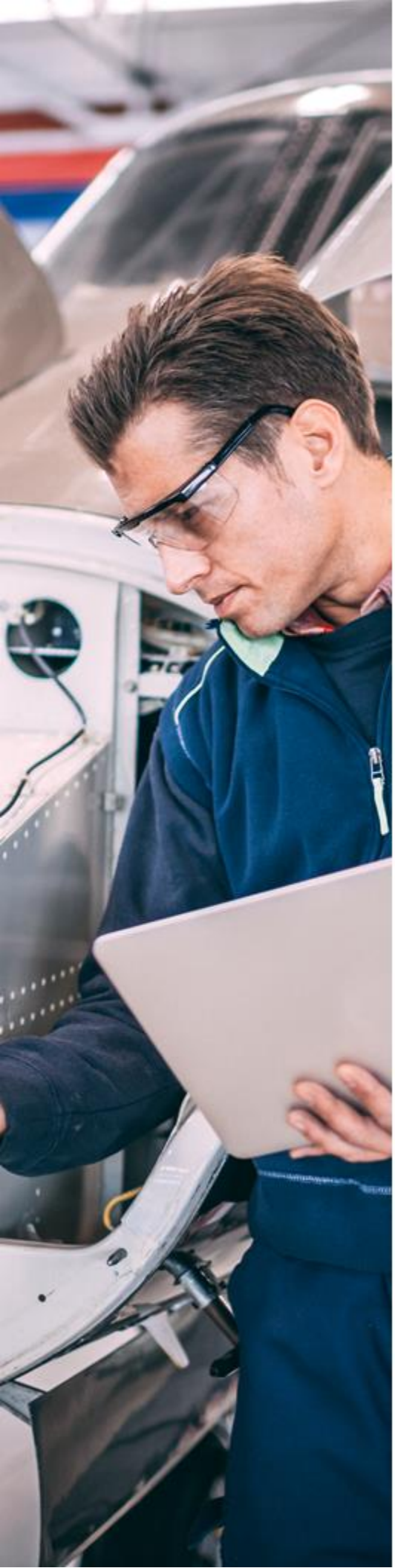

## FIGURE 08

System Diagram for Radar Target Generators Based on PXI Instrumentation and LabVIEW FPGA

| KEY SPECIFICATIONS | |
|---|---|
| Frequency | RF transmit and receive coverage from 9 kHz to 44 GHz |
| Bandwidth | Up to 1 GHz of instantaneous RF bandwidth |
| Channel Count | 4 to 34 independent input and output channels per chassis |

## TABLE 03

Key Specifications of Radar Target Generators Based on PXI Instrumentation and LabVIEW FPGA



# NI Services and Support

NI offers a variety of solution integration options customized to your application-specific requirements. You can use your own internal integration teams for full system control or leverage the expertise of our worldwide network of NI Partners to obtain a turnkey system.

Contact your account manager or call or email us to learn more about how NI can help you increase product quality and accelerate test timelines at (888) 280-7645 or info@ni.com.

## NI Services and Support

- Consulting and Integration
- Turnkey Solution Delivery
- Repair and Calibration
- Global Support
- Prototype and Feasibility
- Training and Certification

ni.com

ni.com/aerospace