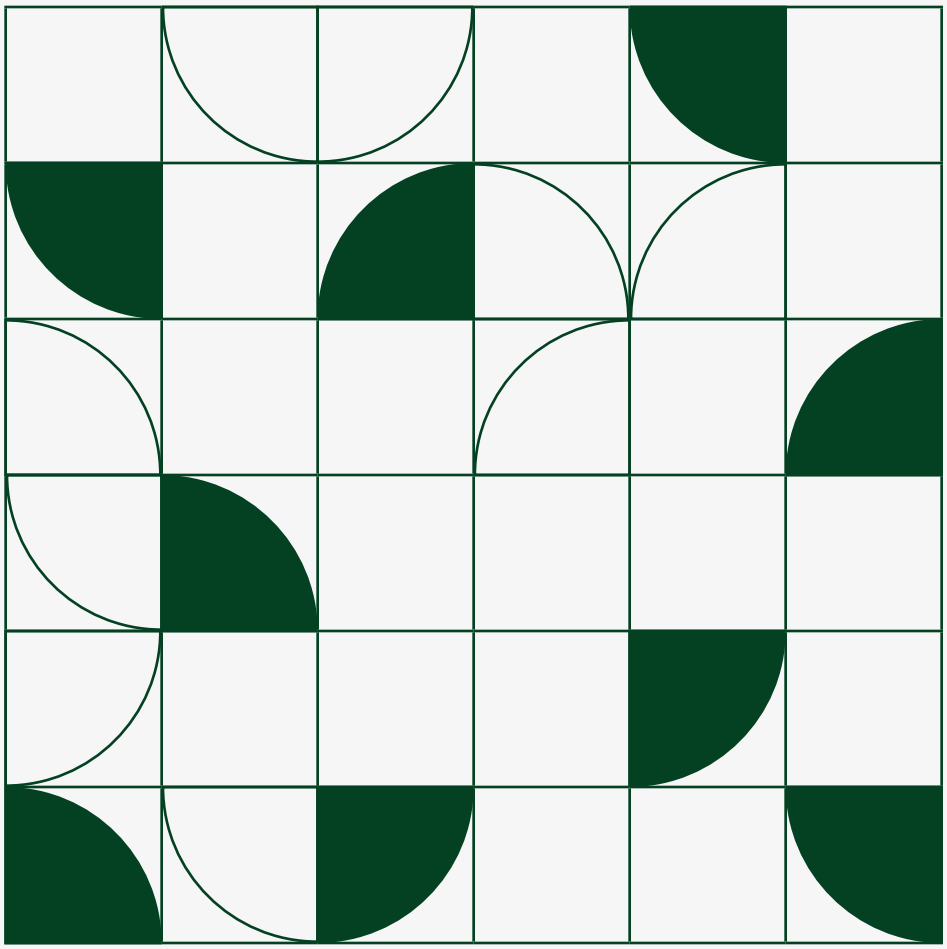
APPLICATION NOTE

Image Data Interface Test Challenges for Modern Focal Plane Array Systems



Common Imaging Detector Systems Architectures

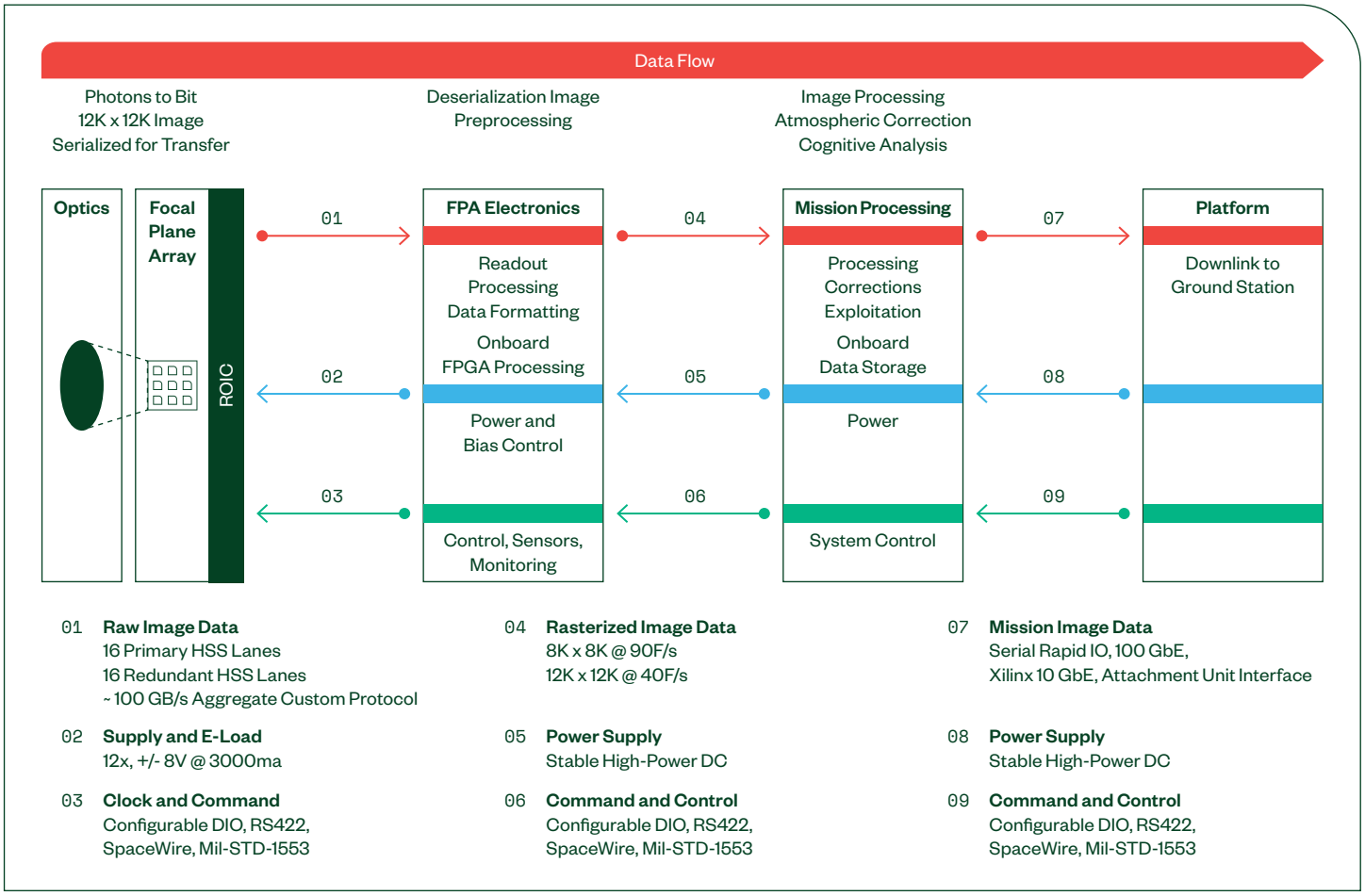


FIG 1 Common Imaging Detector System Architecture

Modern focal plane arrays are often customized to meet the unique requirements of a specific mission; however, most systems share a common overall system architecture, as shown in Figure 1. The FPA detector on the left is paired with advanced optics to capture incoming light of a specific wavelength and convert that into pixels which are then converted into analog or digital data for further processing. Often, the tightly integrated readout integrated circuit (ROIC) has three main interfaces for data, bias, and control.

The data interface shown in red can be a high-speed data bus or an analog interface to offload image data. The FPA is powered and biased from a range of power supply lines represented by the blue path on the diagram. These can have non-standard voltage and loading requirements depending on the technology of the FPA device. Additionally, the FPA has a clocking and command interface to control the device during normal and testing operation. The data, bias, and control interfaces often cascade through other subsystems or circuit card assemblies (CCAs).

The FPA electronics, sometimes called the "close-in-electronics," are responsible for controlling the FPA, supplying the bias and consuming raw frame data for correction and front-end processing. Subsystems are often developed in parallel; teams building the FPA device and FPA electronics must test interfaces before the other is ready. This presents a challenge to the FPA test engineer to emulate the digital interface functionality before it is complete.

The following sections present two approaches to test solution development and put forth the unique requirements of data interface testing while explaining an efficient solution based on NI modular FPGA-based high-speed instruments.

FPGA Evaluation Board Approach

Modern FPA testing requires moving large amounts of data through high-speed interfaces, often with some protocol customization to meet a specific mission requirement. Many FPA test initiatives leverage FPGA evaluation boards or custom-designed interface boards to handle these high-speed interfaces. Using off-the-shelf FPGA evaluation boards is beneficial, as these boards allow for incorporation of custom IP and are often less expensive than acquiring FPGA silicon separately.

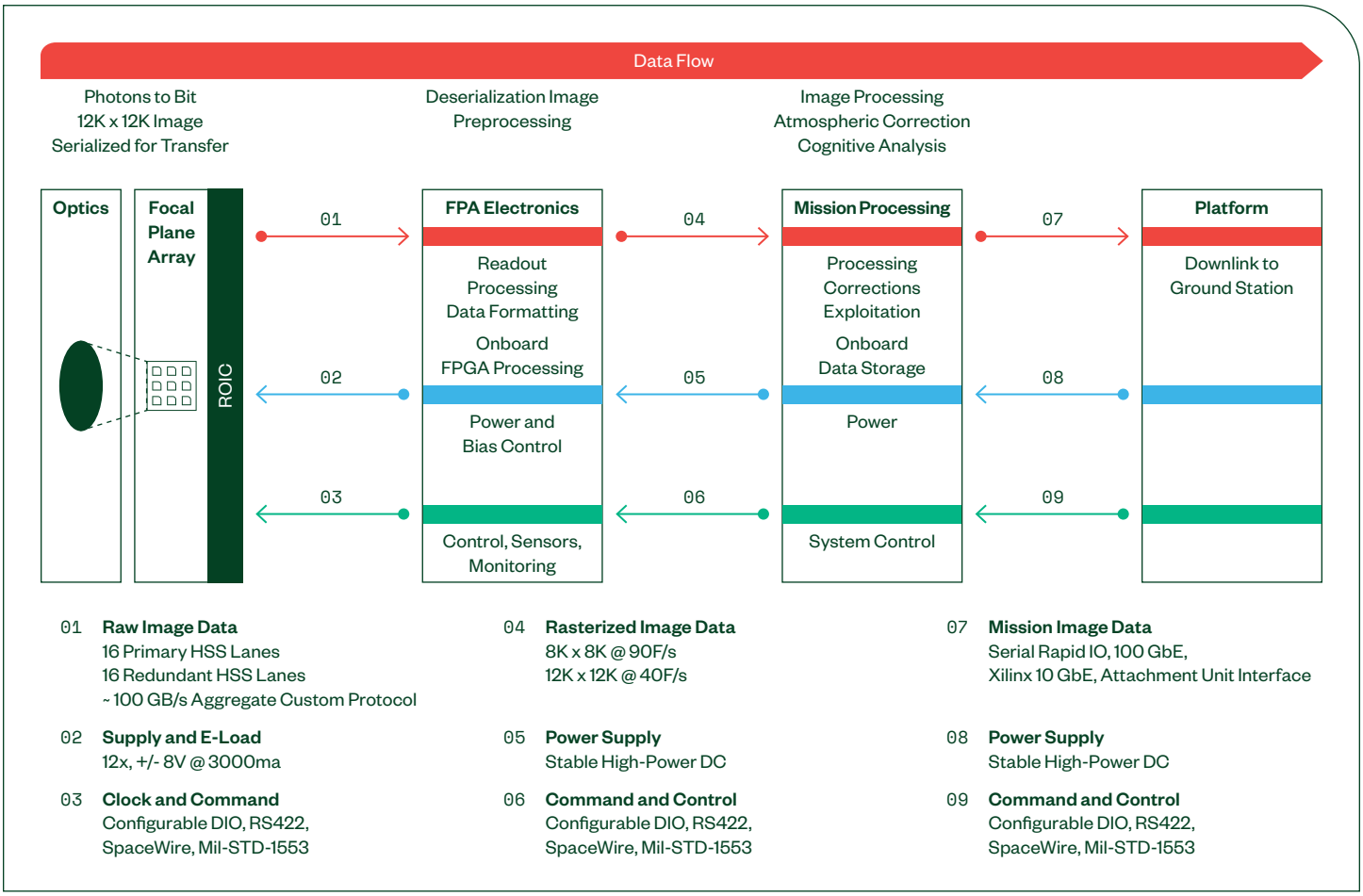
However, evaluation boards often have short product life cycles, making testers built on them a challenge to maintain long-term, adding to total test development and sustainment cost. Also, as devices age, software application updates may drop support for older devices, making obsolescence management a challenge. Additionally, in late stages of an FPA program, there is often significant risk of a tester failing and sustainment teams being unable to obtain replacement parts, forcing a late costly tester update. Lastly, evaluation boards often require the skills of a specialized FPGA design engineer familiar with the low-level software implementation tools, a skill not often associated with test engineering experts.

Modular, Standards-Based Approach

An alternative to the custom approach with FPGA evaluation boards is the NI modular solution based on the PCI express extension for instrumentation (PXIe) standard. Within the NI PXIe instrument portfolio are several options to meet both the operational longevity requirements while retaining the ability to integrate custom digital IP. The NI solution for digital interface testing is based on Flexible Reconfigurable IO (FlexRIO) technology.

FlexRIO interface modules are commercial-off-the-shelf (COTS) instruments with a fully open FPGA as well as interfaces that meet the unique requirements of common FPA configurations. FlexRIO technology, when paired with LabVIEW FPGA development tools built atop the Xilinx Vivado development platform, abstract some of the complexity of custom FPGA IP integration while maintaining a fully open user programmable experience. FlexRIO boards are often paired with a high-capacity, high-speed storage RAID to record or play back data to the various subsystems.

Example NI FlexRIO modules are highlighted in red in Figure 2. The ability to consolidate data, power, bias, and command into a single modular open software connected test system allows for efficiencies in test development, system performance, and test system longevity.



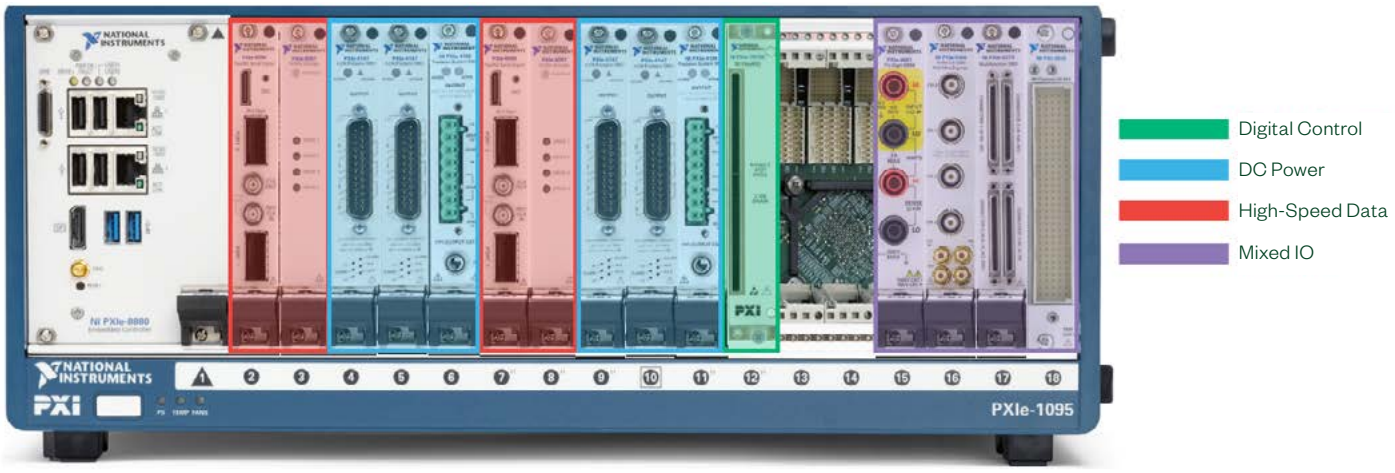


FIG 2 Common Imaging Detector Interfaces Mapped onto a PXI Express System

Parallel Subsystem Test Development

The various FPA subsystems shown in Figure 1 are often developed by different teams and sometimes even different vendors. The team developing a specific FPA device may not be able to wait for the FPA electronics system to be available to test their new design. Similarly, engineers designing FPA electronics or mission software systems are required to test systems prior to the availability of the target FPA device. Parallel subsystem development is critical to efficient development but poses a challenge to test. A critical question: how can you reduce the risk of failure at the integration stage before the rest of the system is ready?

Many engineers solve this challenge by using a customized digital interface solution to record, playback, or emulate data for the various FPA subsystems. Figure 3 illustrates the various ways NI hardware may be interfaced to test subsystems throughout the design cycle. Early-stage design may require full FPA system emulation to test mission software, whereas mid-design FPA sensor tests are often performed by recording data from an FPA device to characterize or calibrate image performance. A key benefit of the NI solution is that often the same hardware and software can be used for all five scenarios represented in Figure 3, allowing teams to standardize and share best practices and IP to accelerate development and test.

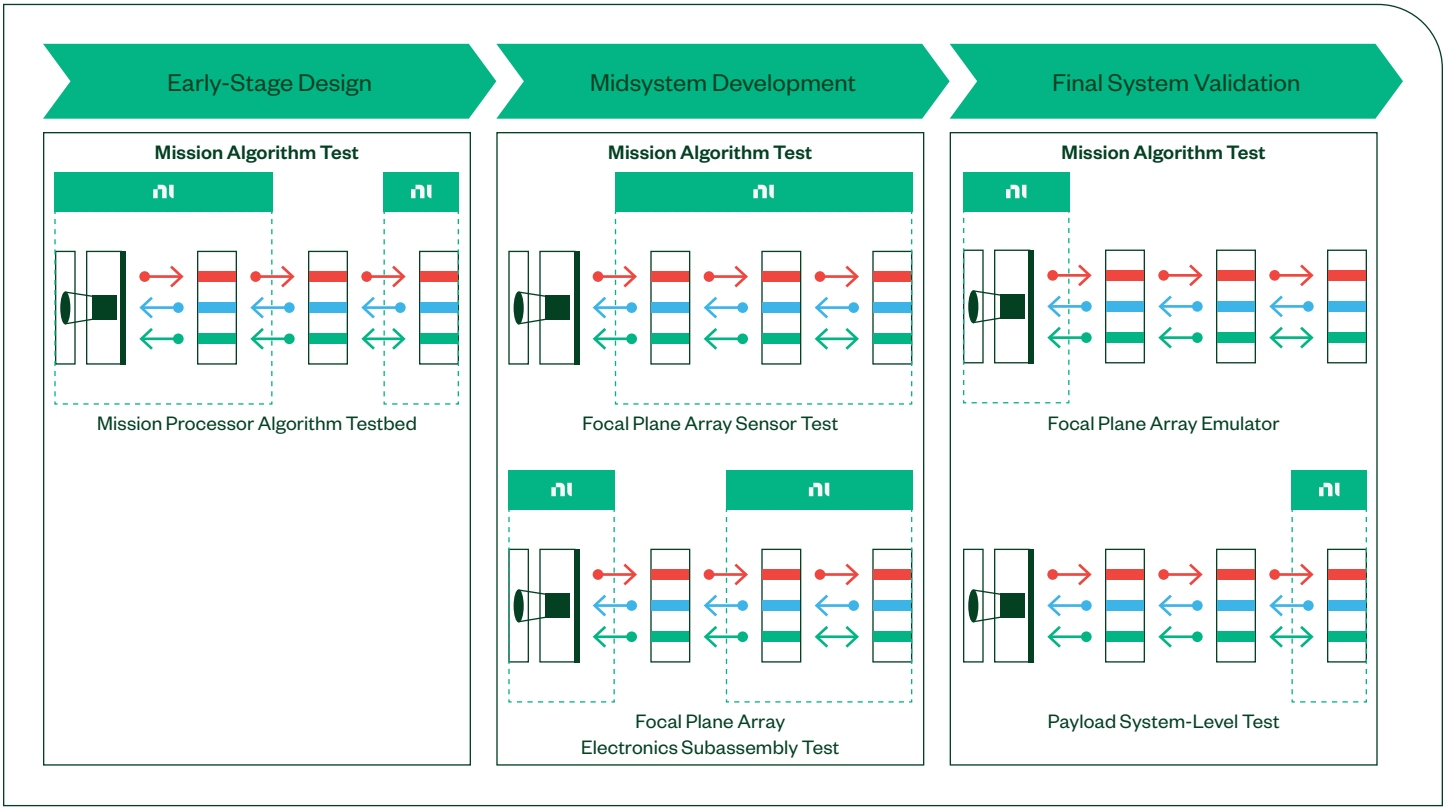


FIG 3 FPA Digital Interface Testing over the Development Cycle

Legacy Interface Challenges

The NI FlexRIO product family is a popular solution to test data interfaces for FPA subsystems. However, not all FPA interfaces are based on high-speed serial digital interfaces. Many legacy systems have analog or parallel digital interfaces. In this section, we'll discuss the unique challenges for each of these interface types and a few common PXIe solutions for each.

Analog FPA Interface Testing

Many legacy FPAs utilize analog sensors with separate discrete digitization circuitry outside of the FPA sensor or chip. The use of discrete analog and digital components requires additional test instrumentation compared with the more integrated digital ROIC FPA configurations. Analog FPA devices often require clock signals with specific timing to control scanning and digitization. The challenge with testing these types of devices is the need to coordinate and synchronize multiple instrument types such as a multichannel digitizer along with instrumentation for clock generation and frame signaling.

Popular modules for multi-channel analog FPA device test include the PXIe-5172 oscilloscope shown in Figure 4 and the PXIe-5764 digitizer when faster scan rates are required. The PCIe-5172 is a 14-bit, 8-channel, 100 MHz IBW FPGA reconfigurable oscilloscope and the PXIe-5764 is a 16-bit, 4-channel, 400 MHz IBW, 1 GS/s digitizer. It is common to pair these instruments with a FlexRIO PXIe-7972 combined with the NI-6583 digital front-end shown in Figure 5 or PXIe-6570 digital pattern instrument to handle generation of clock/frame signals on the digital interfaces. These modules can be controlled from a common bus and synchronized across the PXIe backplane for more efficient and synchronous operation.

FIG 4 PXIe-5172 FPGA-Based Multichannel Digitizer

FIG 5 PXIe-7972 FlexRIO with NI-6583 Digital IO Adapter Module

Parallel Data Interfaces

Many legacy FPAs utilize slow-speed, parallel digital input/output (DIO) interfaces, as the digitizer is integrated directly into the detector sensor or chip. These devices send digital data directly off the detector and commonly use standard logic levels such as TTL, LVTTL, or LVDS for command and control. These tend to be slower-speed devices and require parallel digital IO test hardware to capture and control of these devices. The use of FPGA-enabled FlexRIO instruments like the PXIe-7972 with a digital adapter like the NI-6583 is a common solution, as shown in Figure 5.

SerDes-Coupled Interfaces

The most modern FPA detectors are designed with SerDes-coupled interfaces integrated into the detector. These sensors often utilize standard physical layer protocols such as serial rapid IO (SRIO) or Aurora but may have some customized aspects of the protocol such as data framing changes. These changes can make interface testing a challenge. In addition, due to the high-speed nature of the interface, it is common to break the FPA into multiple segments requiring multiple high-speed serial interfaces.

By separating an FPA into segments, interfaces can operate at lower rates, simplifying cabling and synchronization. However, test systems must account for the interface segmentation and protocol customizations. Interfacing with these high-speed serial interfaces is often accomplished with the high-performance FlexRIO PXIe-6594 shown in Figure 6. The PXIe-6594 includes a fully open FPGA like all FlexRIO-based modules and includes two 4-lane QSFP+ interfaces boasting speeds up to 28 Gbps.

Being a fully customizable FPGA-based instrument, it can support almost any serial interface protocol such as 1/10/100 Gb Ethernet, Aurora, SRIO, and more. The NI FlexRIO interface hardware can integrate your custom IP or integrate third-party IP designed in LabVIEW FPGA, VHDL, and Verilog—or simply import an RTL block.

FIG 6 PXIe-6594 High-Speed Serial FlexRIO 8 Lanes, up to 28 Gbps

FPGA Software-Development Tools

When designing with Xilinx-based devices, Vivado is a popular development platform and comes with a wide range of IP blocks to pull from. FPGA evaluation boards often come with a low-level board support package which requires digital design expertise to utilize. Frequently, engineers who are expert FPGA designers aren't expert test system designers. Therefore, maintaining custom FPGA IP for test can be a challenge from an operational staffing perspective.

The NI solution to this challenge is the use of a graphical programming environment comprised of LabVIEW and LabVIEW FPGA. LabVIEW FPGA is a development framework, built atop Xilinx Vivado, that provides an easier-to-use, high-level abstracted design flow that still retains the ability to import custom FPGA IP. Figure 7 illustrates how you can take custom HDL code, import it into LabVIEW with a "component-level IP" (CLIP) integration node, and target a high-performance, FPGA-based PXIe instrument. The LabVIEW FPGA CLIP node feature allows for communication over standard digital protocols while also allowing for modification of digital interfaces as with an FPGA evaluation board.

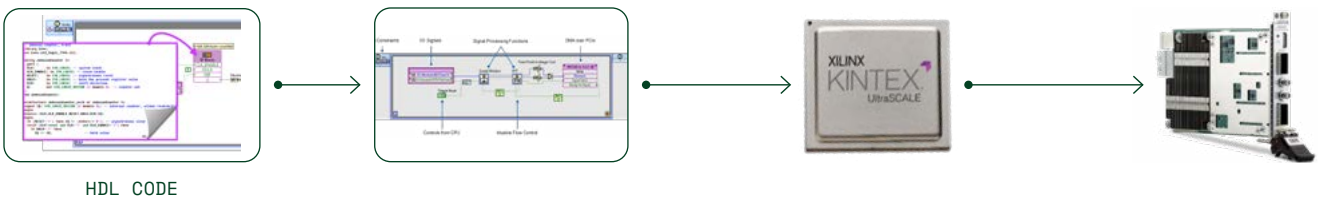


FIG 7 PXIe-7972 FlexRIO with NI-6583 Digital IO Adapter Module

One can think of LabVIEW FPGA as higher-level robust board support package that abstracts some of the most complex, expensive, and time-consuming aspects of FPGA design such as incorporating PCIe interfaces, DMA engines, peer-to-peer FIFOs, and memory mapped registers. The higher-level abstraction saves time, allowing you to focus on your IP and test challenges rather than board support infrastructure. A seemingly simple high-level block diagram can replace thousands of lines of VHDL code, vastly simplifying development and boosting productivity. For engineers who are more comfortable developing in traditional HDL languages, LabVIEW exports projects to Vivado, allowing for development with NI hardware while directly using the Xilinx tool chain.

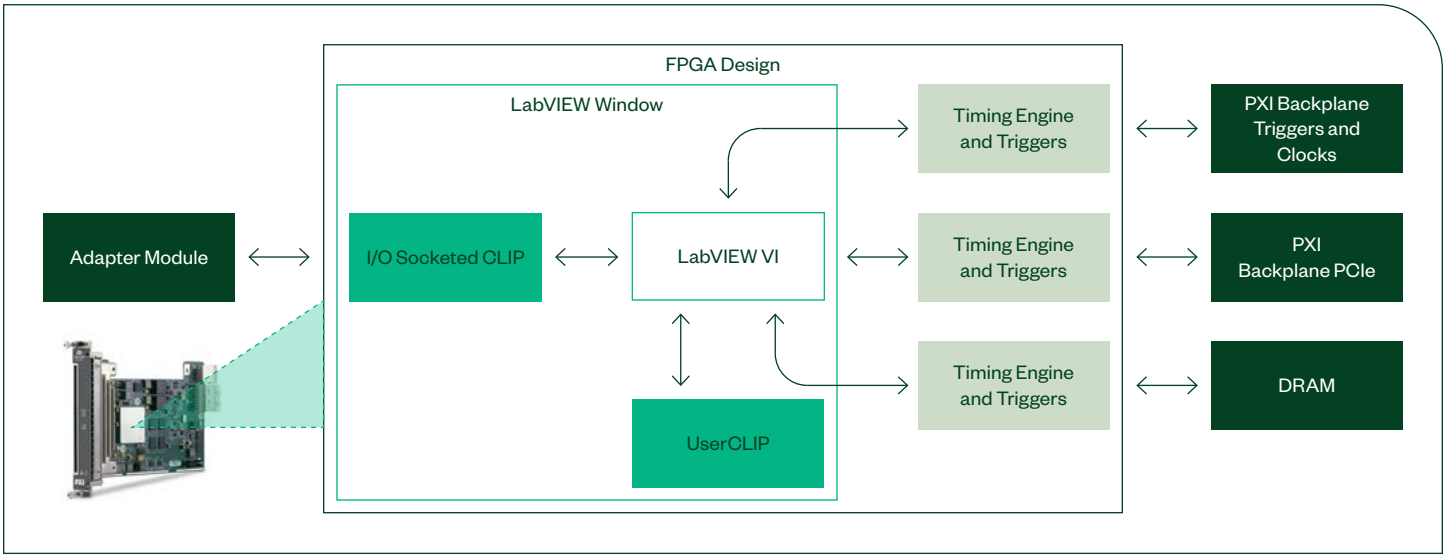


FIG 8 PXIe-7972 FlexRIO with NI-6583 Digital IO Adapter Module

Large Data File Transfer and Storage

As previously mentioned, digital FPA interface boards are often paired with a mass storage device such as an in-chassis or external RAID to store data or transmit data into one of the FPA subsystems. Due to the large file sizes recorded or played back, standard computer system memory or FPGA block RAM is not sufficient for most FPA test applications. Code must be in place on the host computer to manage data movement between the FPGA and mass storage. Having a system with data movement capability in hardware is crucial to keep up with high sustained data rates to and from FPA DUTs.

Primary considerations for the selection of a mass storage solution include data rate and capacity. Standard hard drives or solid-state drives typically can't keep up with the data rates required for FPA test. To overcome this challenge, systems often use high-performance streaming mass storage devices in a RAID 0 configuration. Two popular NI solutions are the NI RMX-8268 and PXIe-8267 for this function, as shown in Figures 9 and 10. The PXIe-8267 is conveniently integrated into the PXIe chassis; however, it is limited to 4 TB of storage, whereas the RMX-8268 is external and can be MXI cabled—and can store up to 48 TB.

FIG 9 | PXIe-8267 4 TB in-Chassis Mass Storage RAID

FIG 10 | RMX-8268 External Mass Storage RAID 24 TB SSD or 48 TB HDD

When reading and writing data to mass storage, it is best to minimize the number of times data is copied and moved within the system. Unless special provisions are implemented, standard operating system data movement commands will often push data through system memory when moving from the FPGA to mass storage resulting in multiple copy operations. Multiple copy operations can slow down system performance. A better approach is to use a "zero copy" method. Zero copy allows for data from the FPGA/mass storage to be read and written without bringing a copy into application memory. This allows background processes in the operating system to handle the data movement without added overhead.

Besides zero copy for data storage, data can be transferred by peer-to-peer (P2P) FIFO between instruments or NI FPGA devices to perform additional tasks. Peer-to-peer transfer allows for data movement between modules directly over the PXIe backplane without involving the host PC. This enables additional data paths such as FPGA processing between the digital instrument and storage, exported digital sub-streams, and so forth. The ability to perform peer-to-peer streaming and zero copy data movement is a key advantage of the NI PXIe system. To learn more about how to implement zero copy in your FPA test system, reference the articles Improving Streaming Application Performance with Zero Copy and for Peer-to-Peer implementation reference, An Introduction to Peer-to-Peer Streaming.

Conclusions

Modern focal plane arrays operate with high resolution and can have high frame rates requiring advanced high-speed data interfaces. The NI solution for high-performance, serial interface test retains the openness and flexibility of using an FPGA evaluation board, but with more built-in functionality which is important to modern FPA interface testing. The NI PXIe-based solution employs FlexRIO modules covering a range of protocols and can stream peer-to-peer and zero copy to mass storage. These advanced features enable engineers across the test engineering team to standardize and share best practices to accelerate program schedules and deliver capabilities on time with reduced cost of and improved readiness.

Links to Additional Technical Documentation

Shop High-Speed Serial Instruments

An Introduction to NI High-Speed Serial Instruments

High-Speed Serial 101