# Building a Combinatorial Circuit Using Data Flow Modeling Lab

Publish Date: Jul 23, 2010

## Overview

This lab teaches students the principle of data-flow modeling using Verilog logical operators. Students will design a combinatorial circuit that looks at a BCD input and lights up one of the LEDs on the NI DE FPGA Board when the input is divisible by 3. Additionally, students will learn about continuous assignment statements, their syntax, and the operators they support using Xilinx ISE Tools.

### 1. Building a Combinatorial Circuit Using Data Flow Modeling Lab

This is a free downloadable lab to be used with the NI DE FPGA Board, and Xilinx ISE tools. Students can begin to learn how to program an FPGA with Verilog by referring to the Building a Combinatorial Circuit Using Data Flow Modeling Lab, downloading the attached support files and completing the exercise steps.

To begin, please download the attached PDF document and .zip file.

**Software Requirements**

**Application Software:** Xilinx ISE tools

**Hardware Requirements**

**Driver:** NI Digital Electronics FPGA Board Driver Software