4.4 Incorporate Unified Structural and Functional Testing

*Improving Test Throughput with Emerging Technologies*
Testing becomes more difficult as chip densities and surface-mount techniques have advanced. The ICs themselves are constantly becoming more complex, with higher pin counts and finer pitches, while the PCBs also become much more complicated and densely packed.
Quantifying the Test Challenge

• Complex PCBs: more than 20,000 solder joints
• Even with world-class quality (<100 ppm structural faults)

More than 90% of the PCBs produced will contain at least one structural fault.

Ref: Charles Robinson and Amit Verma, Teradyne Inc., APEX 2002

A study done two years ago makes the point very dramatically. Even if a production line achieves very high quality levels, almost every complex board built will contain at least one structural fault that must be detected, diagnosed, and repaired. Thus the test strategy must include as thorough a screen for structural faults as possible.
There are many variations on this flow, but the general process is to follow the assembly process with a visual inspection, to confirm that the process is in control. Some type of structural test is usually performed, to weed out as many manufacturing problems as possible before entering the functional and system test stages. The objectives of the sequence of test steps are to detect all possible faults prior to shipping the product, and to do so as early in the flow as possible. This keeps the total cost of test low, and allows process problems to be corrected before they can become widespread.
Structural Testing

• Detect manufacturing faults – solder problems, incorrect parts, and so on
• Often generated automatically by an ATPG software tool
• Fault diagnosis is precise, if sufficient test points are available

Reduces “bone pile” – detects faults prior to functional test

Structural testing can take many forms: In-circuit testing, X-Ray, flying probe, and boundary-scan. Regardless, the aim of a structural test is to detect faults that may have occurred in the process of assembling the board. Two significant characteristics of structural testing: often a structural test can be developed automatically, and therefore rapidly, by an intelligent software tool. And second, often diagnosing a fault detected by a structural test is quick and precise. So, the aim is to be able to find as many structural faults as possible at this point in the flow, prior to functional testing.
In-circuit testing is very widely used to probe and test boards for structural faults. An ICT system conducts the tests by means of a fixture or bed-of-nails that drives and senses electrical conditions on a large number of test points simultaneously. Its effectiveness is determined by the number of available test points. But with today’s complex multi-layer boards, possibly containing BGA packaged-ICs, there are classes of structural faults that will be very difficult for an ICT system to detect. Note, too, that leaving room for ICT test points can be difficult on a crowded board: there are minimum sizes and minimum spacing rules that have to be observed, consuming valuable real estate. Furthermore, adding traces to the board to connect test points can introduce unwanted electrical interference, especially on high-speed systems.
The well-known 1149.1 standard has now been official for 14 years. It was formalized by a group of manufacturers who foresaw board test problems as chip design advanced and has proven to be a sound architecture for adding testability to PCBs. In recent years, 1149.1 has been extended to cover analog measurements, testing of high-speed LVDS channels, system-level applications, and flash and PLD programming. The IC manufacturer is responsible for adding boundary-scan logic to the chip in compliance with the specification and to disclose the added logic via a BSDL file. Accuracy of these files, once a problem area, is much improved today. We are finding that many of the more complex digital ICs contain compliant boundary-scan logic, so the opportunity to take advantage at the board level is very often present.
If the PCB is designed to support boundary-scan, then the fault types that we looked at earlier with a high-density board containing BGAs can be detected and diagnosed easily. One or more boundary-scan chains, each with a Test Access Port (TAP) are implemented on the board, giving test access to all of the I/Os on the BGAs without the need for physical contact. It is possible that ICT would still be needed for the analog circuits, but the test fixture can often be much simpler, with fewer physical test points, and therefore become less expensive and more reliable.
Boundary-Scan Applications

• Testing
  — Infrastructure – tests the scan chain
  — Interconnection nets between scan points
  — Cluster tests of non-scan nets
  — Memory connections

• On-board programming
  — CPLDs, FPGAs, serial memory devices
  — Flash memories

Even though only a small number of ICs on the board may contain boundary-scan, it is possible to achieve very high levels of test coverage for structural faults:
  • In the chain itself, the “infrastructure”
  • In the bscan interconnections
  • In various clusters of non-bscan devices
  • And in the address, data, and control signals to the memories on the board.

Also, the same bscan system, after conducting the tests, can program flash memories and PLDs on the board.

Adherence to boundary-scan DFT rules is essential but not difficult. We offer a very important DFT booklet to explain all of the details—please stop by our table to get your copy.
Visualization provides paperless diagnosis of faults found during structural test. The faults are projected on the schematic and the board layout.
Many factories today deploy their boundary-scan testing in a “stand-alone” configuration, running on a PC or laptop. But more and more, we are seeing users switch to combining bscan within other test systems, including In-Circuit Testers, flying probe systems, and functional testing. The combination with functional is particularly interesting because this allows the user to accomplish two steps in the traditional test flow in one position.
Boundary-Scan/Functional Integration

- Familiar TestStand GUI
- Custom step types for test and ISP
- Support for LabVIEW, LabWindows, C++, Visual Basic
- Sequence includes boundary-scan steps and other functional steps
Benefits of Unified Testing

• One-stop board testing and in-system programming
  – Skip the ICT step
  – Less handling of products, save floor space
• Lower cost
  – Much less capital investment
  – Significant fixture savings
  – Reduced bone-pile
• Quicker time-to-market
  – Automated test and diagnostics preparation
  – Shorter prototype debug time
  – Earlier production start
  – Faster fault localization with visualization
• Better quality
  – Predictable & known fault coverage
  – Precise diagnostics

The combination of boundary-scan and functional testing delivers important benefits to the production facility.