

NI PXIe-5622 Specifications

16-Bit IF Digitizer with Onboard Signal Processing

This document lists the specifications for the NI PXIe-5622 high-speed digitizer. Unless otherwise noted, the following conditions were used for each specification:

- Direct path filter setting
- Sample clock set to internal 150 MS/s, unlocked
- 1 V vertical range

Specifications describe the warranted, traceable product performance over temperature ranges of 0 to 55 °C, unless otherwise noted. Specifications warranted under the following conditions:

- 15 minute warm-up time at ambient temperature
- Calibration cycle maintained
- Chassis fan speed set to High
- NI-SCOPE instrument driver self-calibration performed after instrument temperature is stable

Typical values describe useful product performance beyond specifications that are not covered by warranty and do not include guardbands for measurement uncertainty or drift. Typical values may not be verified on all units shipped from the factory. Unless otherwise noted, typical values cover the expected performance of units over temperature ranges of 23 ± 5 °C with a 90% confidence level, based on measurements taken during development or production.

Nominal values (or supplemental information) describe additional information about the product that may be useful, including expected performance that is not covered under Specifications or Typical values. Nominal values are not covered by warranty.

Specifications are subject to change without notice. For the most recent product specifications, visit ni.com/manuals.



Hot Surface If the NI PXIe-5622 has been in use, the device or the shield may exceed safe handling temperatures and may cause burns. Allow the module to cool before touching the shield or removing the device from the chassis or PC. Refer to the *Environment* section for operating temperatures.

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Vertical

Analog Input (IF IN)

Specification	Value	Comments
Number of Channels	One (IF IN)	—
Impedance and Coupling		
Input Impedance	50 Ω nominal	—
Input Return Loss, Typical	<-15 dB	5 MHz to 300 MHz
Input Coupling	AC	—
Voltage Levels		
Full Scale (FS) Input Range	0.7 V _{pk-pk} (+1 dBm), 1 V _{pk-pk} (+4 dBm), 1.4 V _{pk-pk} (+7 dBm)	Dither enabled. Can overrange up to 3 dB with Dither disabled.
Maximum Input Overload	6.3 V _{pk-pk} (+20 dBm)	—

Specification	Value		Comments
Accuracy			
Resolution	16 bits		—
	Bandpass Path (187.5 MHz)	Direct Path (53 MHz)	
Absolute Amplitude Accuracy*	<±0.5 dB	<±0.4 dB	All input ranges. At center frequency of specified bands. *Specification is valid over 23 °C ±5 °C. Maximum drift of ±2 °C from last self-calibration.
Absolute Amplitude Accuracy, Typical	<±0.3 dB	<±0.25 dB	
Temperature Stability	<0.01 dB/°C	<0.02 dB/°C	All input ranges. Maximum drift of ±2 °C from last self-calibration.
Absolute Amplitude Accuracy Examples at 40 °C in the Bandpass Path			
Amplitude accuracy specification: $0.5 + 0.01 \times (40 - 23) = \pm 0.67 \text{ dB}$			
Amplitude accuracy, typical: $0.3 + 0.01 \times (40 - 23) = \pm 0.47 \text{ dB}$			
Bandwidth and Frequency Response			
	Bandpass Path (187.5 MHz)	Direct Path (53 MHz)	
Bandwidth (–3 dB), Typical	50 MHz Centered at 187.5 MHz, 3rd Nyquist Zone	3–250 MHz	Bandwidth of unequalized response.
Dither Signal, Frequency Range, Typical	100 kHz–12 MHz		Dither can be enabled. Dither disabled by default in NI-SCOPE.

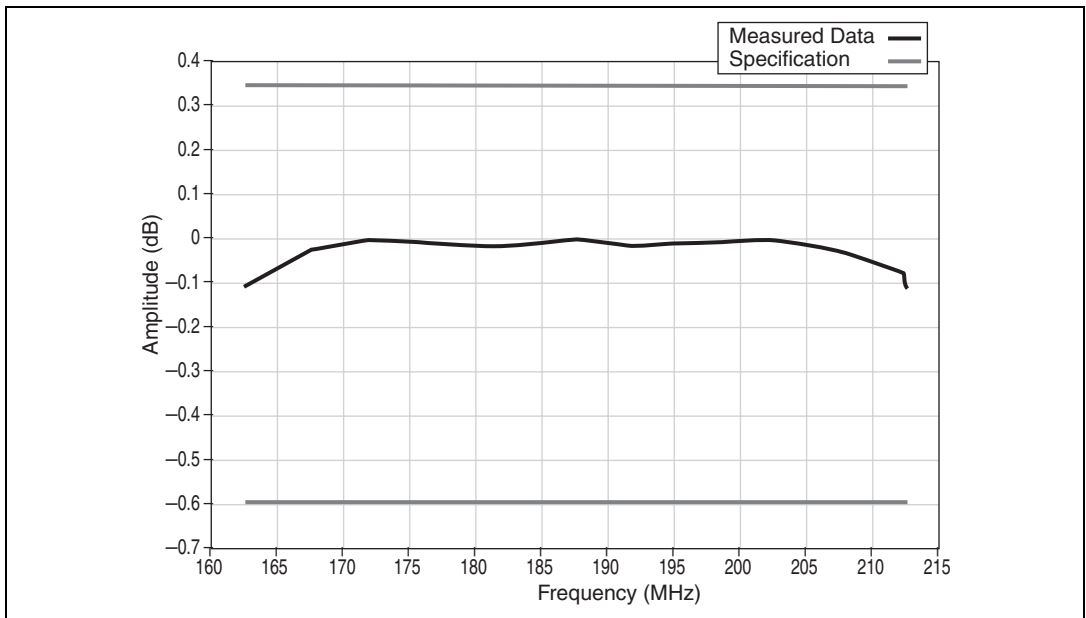


Figure 1. Equalized Amplitude Response (Bandpass Path), Using Calibration Data

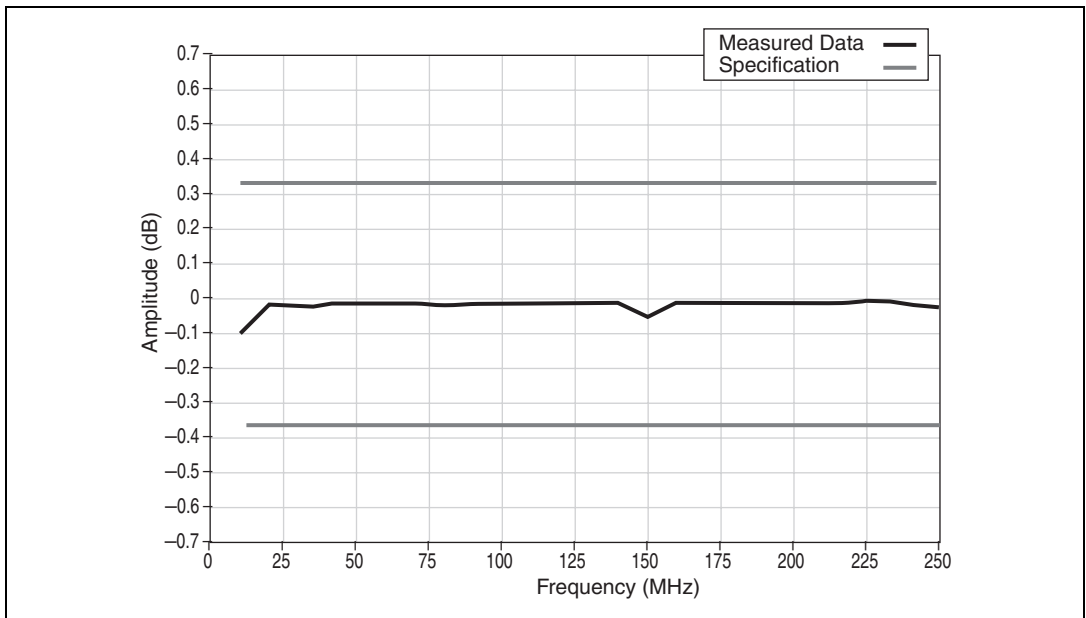


Figure 2. Equalized Amplitude Response (Direct Path), Using Calibration Data



Note The Equalized Direct Path Equalized Amplitude Response shown in Figure 2 is a composite plot of multiple segments of 40 MHz span each.

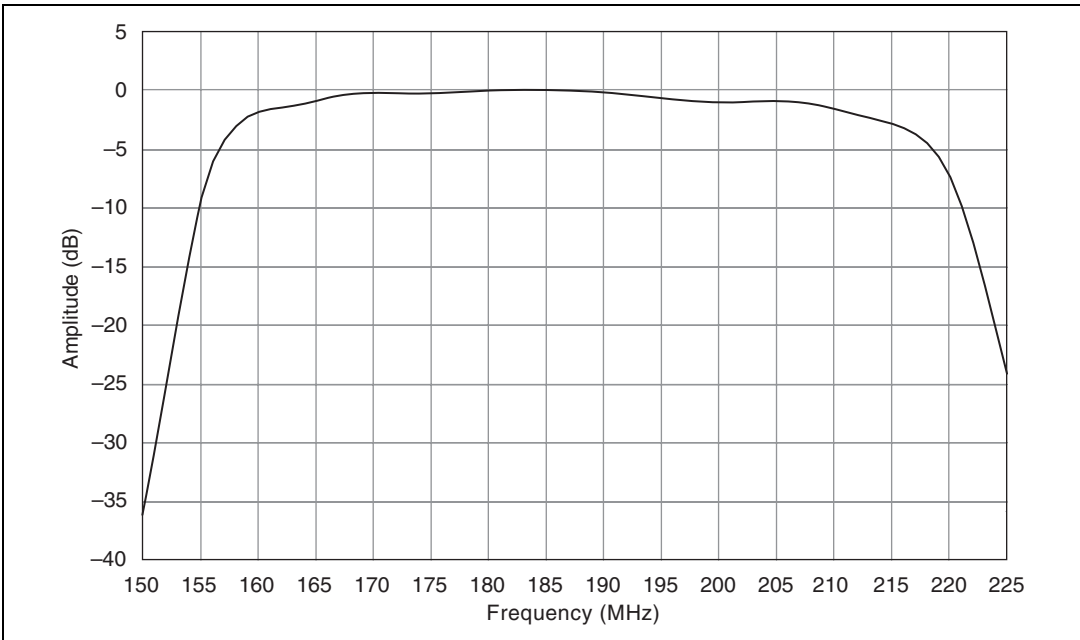


Figure 3. Unequalized Amplitude Response (Bandpass Path)

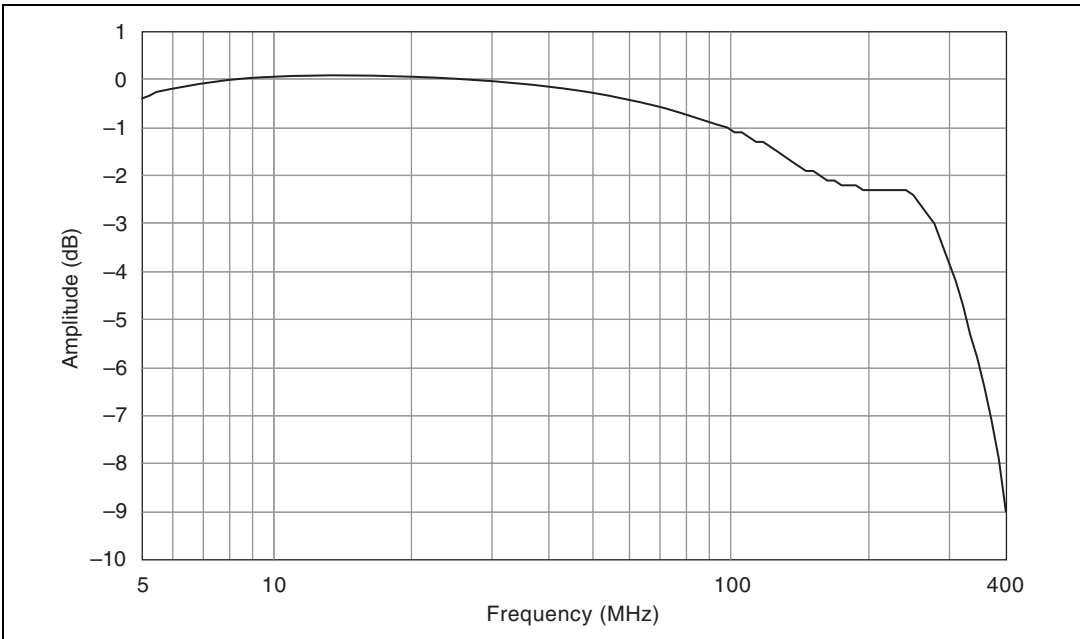


Figure 4. Unequalized Amplitude Response (Direct Path)

Specification	Value			Comments
	Bandpass Path (187.5 MHz)	Direct Path (53 MHz)		
Passband Amplitude Flatness*	< +0.35, -0.6 dB (equalized) 187.5 MHz ±25 MHz	< ±0.35 dB (equalized) 53 MHz ±19 MHz < ±0.6 dB (equalized) 10–250 MHz		* Specification valid for 1 V range. † Typical specification valid for all ranges.
Passband Amplitude Flatness, Typical†	< +0.25, -0.4 dB (equalized) < +0.7, -3.5 dB (unequalized) 187.5 MHz ±25 MHz	< ±0.25 dB (equalized) < ±0.6 dB (unequalized) 53 MHz ±19 MHz < ±0.5 dB (equalized) < ±1.8 dB (unequalized) 10–250 MHz		Equalization requires using the Digital Filter Design Toolkit to compute equalization filter coefficients. This software is not included with the NI-SCOPE driver.
	Bandwidth	Bandpass Path (187.5 MHz)	Direct Path (53 MHz)	
Passband Phase Linearity, Typical	10 MHz	±0.5°	±0.5°	All input ranges. After equalization.
	20 MHz	±1°	±1°	
	40 MHz	±1.75°	—	
	50 MHz	±2.5°	—	

Specification	Value		Comments
Spectral Characteristics (+3 dBm total power at 1 V range, Dither ON)			
	Bandpass Path (187.5 MHz)	Direct Path (53 MHz)	
Spurious-Free Dynamic Range with Harmonics (SFDR), Typical	<-76.5 dBc	<-73 dBc	Down to -10 dBFS level.
Total Harmonic Distortion (THD), Typical	<-76 dBc	<-71 dBc	Includes 2nd through 5th harmonics.
Intermodulation Distortion (IMD), Typical	<-74 dBc	<-73 dBc	Two tones, 1 MHz apart. Down to -10 dBFS level.

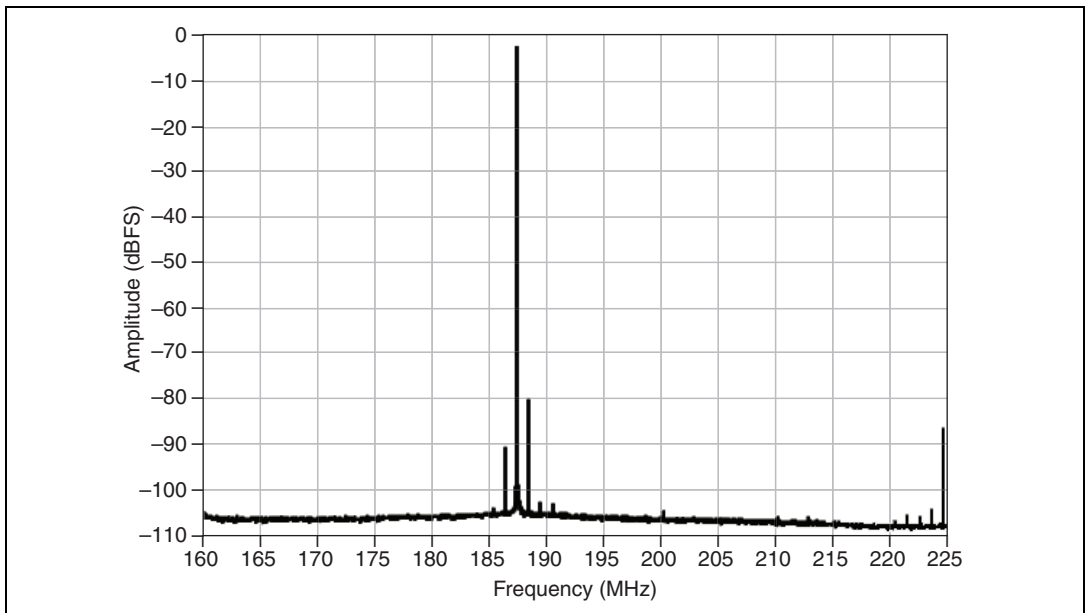


Figure 5. Single Tone Spectrum at 5.5 dBm, Bandpass Path, 4 kHz RBW

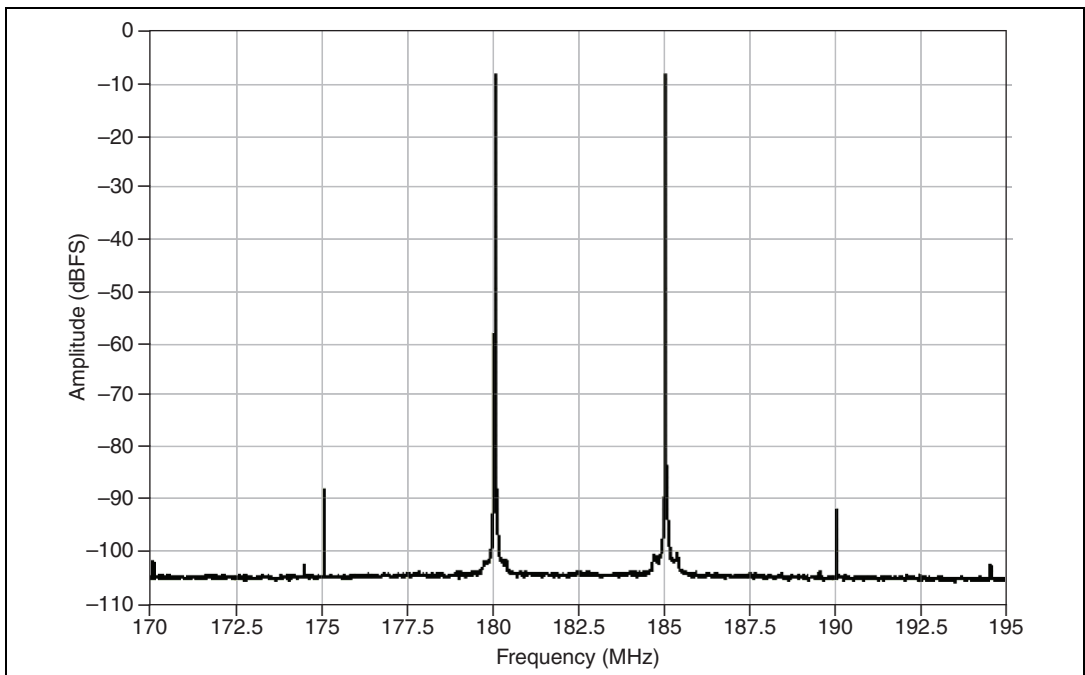


Figure 6. Two Tone Spectrum at 2 dBm Each, Bandpass Path, 4 kHz RBW

Specification	Value		Comments	
	Bandpass Path (187.5 MHz)	Direct Path (53 MHz)		
Full Bandwidth Signal-to-Noise Ratio (SNR), Typical	>66.5 dB	>67 dB	Internal VCXO at 150 MS/s	
4 MHz Bandwidth SNR, Typical	>71.5 dB	>73 dB	Sample rate 5.35 MS/s, DDC enabled (4.28 MHz bandwidth)	
		Bandpass Path (187.5 MHz)	Direct Path (53 MHz)	
SSB Phase Noise	100 Hz	<-80 dBc/Hz	<-90 dBc/Hz	Internal VCXO; unlocked.
	1 kHz	<-117 dBc/Hz	<-128 dBc/Hz	
	10 kHz and above	<-134 dBc/Hz	<-141 dBc/Hz	
SSB Phase Noise, Typical	100 Hz	<-83 dBc/Hz	<-94 dBc/Hz	
	1 kHz	<-120 dBc/Hz	<-132 dBc/Hz	
	10 kHz and above	<-140 dBc/Hz	<-144 dBc/Hz	
	Range	Value		
Average Noise Density	0.7 V/+1 dBm	<-146 dBm/Hz		Input terminated noise floor. Maintained for low-level input signals. Both filter paths.
	1 V/+4 dBm	<-143 dBm/Hz		
	1.4 V/+7 dBm	<-140 dBm/Hz		
Average Noise Density, Typical	0.7 V/+1 dBm	<-149 dBm/Hz		
	1 V/+4 dBm	<-146 dBm/Hz		
	1.4 V/+7 dBm	<-143 dBm/Hz		

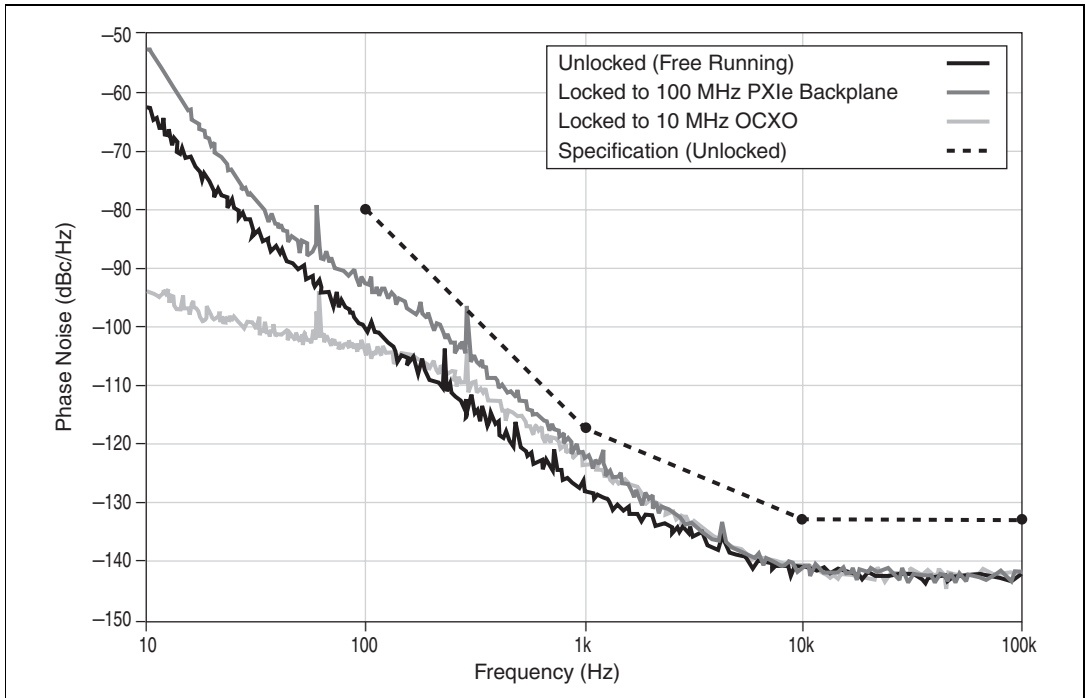


Figure 7. Phase Noise at 187 MHz, Bandpass Path, Signal Level = 3 dBm

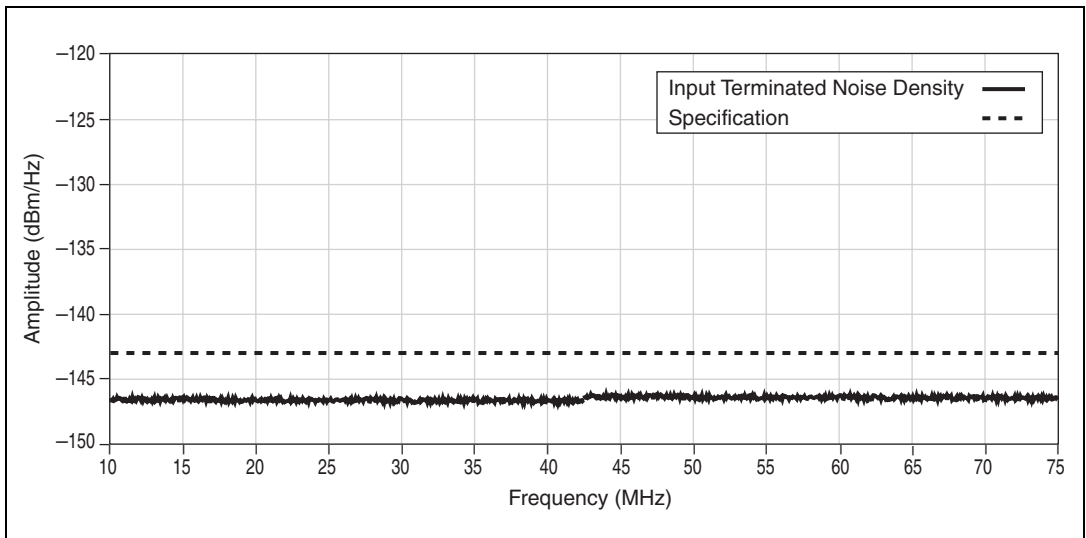


Figure 8. Noise Density (Direct Path)

Horizontal

Sample Clock

Specification	Value	Comments
Sources	Internal VCXO External CLK IN (front panel connector)	Internal VCXO can be free running or locked to a reference clock.

Internal Sample Clock (Onboard VCXO)

Specification	Value		Comments
Sample Rate	150 MS/s with decimation by N		Refer to the <i>Onboard Signal Processing (OSP)</i> section for possible N values (with and without fractional resampling.) Non-OSP decimation does not protect the acquired data from undersampling aliasing. Non-OSP decimation and OSP decimation are mutually exclusive.
Accuracy, Typical	$\pm 5 \times 10^{-6}$		—
Accuracy Over Temperature, Typical	$\pm 12 \times 10^{-6}$		0–55 °C
SSB Phase Noise of 150 MHz sample clock when exported to CLK OUT, Typical	100 Hz	<–90 dBc/Hz	Internal VCXO, unlocked
	1 kHz	<–130 dBc/Hz	
	10 kHz	<–140 dBc/Hz	
	100 kHz and above	<–150 dBc/Hz	

Phase-Locked Loop (PLL) External) Reference Clock

Specification	Value	Comments
Reference Clock Sources	CLK IN (front panel connector) PXIe 100 MHz (PXIe backplane)	Used to phase lock onboard VCXO.
Sample Clock Delay Range	± 1 Sample Clock period	Delay relative to reference clock when VCXO is locked.
Sample Clock Delay Resolution	≤ 4 ps	
Reference Clock Frequency Range	1 MHz to 100 MHz, in 1 MHz increments	—
Reference Clock Frequency Accuracy	Within $\pm 25 \times 10^{-6}$	Refer to your chassis documentation to ensure it meets this requirement.
Reference Clock Duty Cycle Tolerance, Typical	45% to 55%	—
Reference Clock Export Ports	CLK OUT (front panel connector)	—

External Sample Clock

Specification	Value
Sample Clock Frequency Range	20–150 MHz
Sample Clock Duty Cycle Tolerance, Typical	45% to 55%
Sample Clock Export Ports	CLK OUT (front panel connector)

CLK IN (Sample Clock and Reference Clock Input, Front Panel Connector)

Specification	Value
Input Impedance, Typical	50 Ω
Coupling	AC
Amplitude	Sine wave: 0.63 to 2.8 V _{pk-pk} (0 to +13 dBm) Square wave: 0.25 to 2.8 V _{pk-pk}
Maximum Input Overload	6.3 V _{pk-pk} (+20 dBm)

CLK OUT (Sample Clock and Reference Clock Output, Front Panel Connector)

Specification	Value
Output Impedance, Typical	50 Ω
Coupling	AC
Amplitude, Typical	50 Ω load: > +10 dBm 1 k Ω load: square wave, > 2 V _{pk-pk}

PFI 1 (Programmable Function Interface)

Specification	Value
Direction	Bi-directional

Trigger

Specification	Value
As an Input (Trigger)	
Destinations	Start Trigger (Acquisition Arm) Reference (Stop) Trigger Arm Reference Trigger Advance Trigger
Input Impedance	150 k Ω , nominal
Range	0–5 V, TTL compatible
Maximum Input Overload	–3.5 V to +8 V, continuous
Maximum Frequency	20 MHz
Minimum Trigger Width	>25 ns

Specification	Value
As an Output (Event)	
Sources	Start Trigger (Acquisition Arm) Reference (Stop) Trigger End of Record Done (End of Acquisition)
Output Impedance	50 Ω , nominal
Logic Type	3.3 V LVTTTL
Maximum Drive Current	± 12 mA
Maximum Frequency	25 MHz

TClk Specifications

National Instruments TClk synchronization method and the NI-TClk driver are used to align the sample clocks on any number of SMC-based modules in a chassis. For more information about TClk synchronization, refer to the *NI-TClk Synchronization Help*, which is located within the *NI High-Speed Digitizers Help*.

- Specifications are valid for any number of modules installed in one NI PXIe-1062Q chassis.
- All parameters set to identical values for each SMC-based module.
- Sample Clock set to 150 MS/s and all filters are disabled.
- For other configurations, including multichassis systems, contact NI Technical Support at ni.com/support.



Note Although you can use NI-TClk to synchronize non-identical modules, these specifications apply only to synchronizing identical modules.

Specification	Value	Comments
Intermodule SMC Synchronization Using NI-TClk for Identical Modules, Typical		
Skew	≤ 500 ps	Caused by clock and analog path delay differences. No manual adjustment performed.
Average Skew After Manual Adjustment	≤ 4 ps	For information about manual adjustment, refer to the <i>Synchronization Repeatability Optimization</i> topic in the <i>NI-TClk Synchronization Help</i> . For additional help with the adjustment process, contact NI Technical Support at ni.com/support .
Sample Clock Delay/Adjustment Resolution	≤ 4 ps	—

Waveform Specifications

Specification	Value		Comments
Onboard Memory Size	64 MB per Channel Option	256 MB per Channel Option	*Assumes 2-byte samples. In Complex data processing mode (only available when using onboard signal processing), each sample is 4 bytes, so this number is halved.
	32 megasamples per channel*	128 megasamples per channel*	
Allocated Onboard Memory per Record	Real Data	Complex Data	—
	$(Record\ Length \times 2\ bytes/S) + 480\ bytes$, rounded up to the next multiple of 128 bytes	$(Record\ Length \times 4\ bytes/S) + 960\ bytes$, rounded up to the next multiple of 128 bytes	
Minimum Record Length	1 Sample		—
Number of Pretrigger Samples	Zero up to full <i>Record Length</i>		Single-record mode and multiple-record mode.
Number of Posttrigger Samples	Zero up to full <i>Record Length</i>		Single-record mode and multiple-record mode.
Maximum Number of Records in Onboard Memory	100,000 [†]		[†] It is possible to exceed this number if you fetch records while acquiring data. For more information, refer to the <i>NI High-Speed Digitizers Help</i> .

Onboard Signal Processing (OSP)

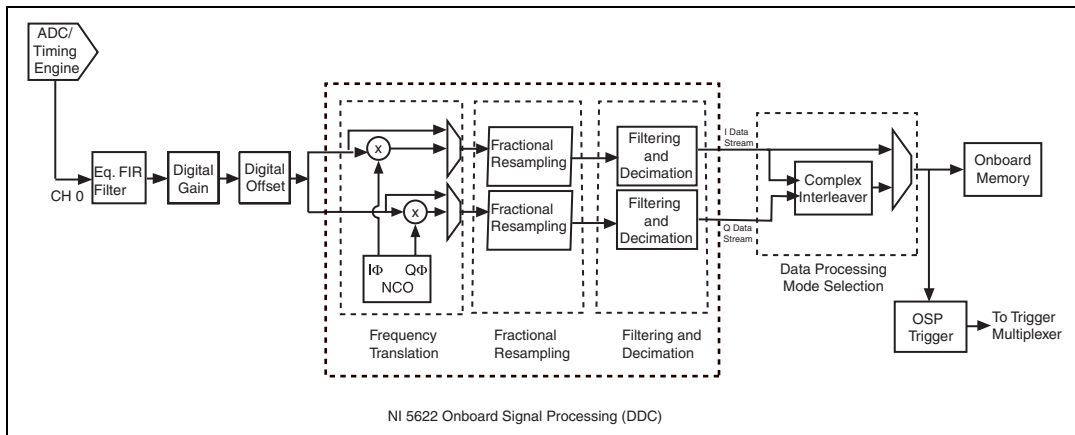


Figure 9. NI PXIe-5622 Onboard Signal Processing Block Diagram



Note To use onboard signal processing (OSP) on the NI PXIe-5622, the DDC Enabled property/attribute must be set to TRUE.

The following four OSP operations are available:

- Send one IF signal to CH 0 and perform quadrature downconversion on the signal (complex data is returned).
- Send a signal to CH 0 and perform alias-protected decimation (real data is returned).
- Send a signal to CH 0 and perform real downconversion on the signal (real data is returned).

Specification	Value	Comments
OSP General		
Number of Digital Downconverters (DDCs)	One	—
Data Processing Modes	Real (I path only) Complex (IQ)	—

Specification	Value		Comments
OSP Decimation Range	1, 2, 4, 6, 8, 10 12 to 4,096 (multiples of 4) 4,096 to 8,192 (multiples of 8) 8,192 to 16,384 (multiples of 16)		OSP decimation protects acquired data from high-frequency aliasing within the ADC Nyquist zone, whereas non-OSP decimation does not. Non-OSP decimation and OSP decimation are mutually exclusive.
	Fractional resampling enabled: 2 to 16,384 to 48 bits of precision		
Sample Rate Range, OSP Enabled	Internal Sample Clock Timebase	External Sample Clock Timebase	For sample rates less than 9.155 kS/s, use an external sample clock or perform additional software decimation.
	9.155 kS/s to 75 MS/s with fractional resampling; or to 150 MS/s without fractional resampling.	Sample Clock Timebase/OSP Decimation Fractional resampling not available.	
Bandwidth	Real Flat Bandwidth $= 0.4 \times \text{Sample Rate}$ Complex Flat Bandwidth $= 0.8 \times \text{Sample Rate}$		Example: Complex bandwidth is 60 MHz with a complex sample rate of 75 MS/s. Using a decimation rate of 1 (sample rate of 150 MS/s with internal clock) bypasses the filters in the OSP block.
Digital Gain and Offset			
Digital Gain and Offset Resolution	18 bits		—
Digital Gain Range	-1.5 to +1.5 Values < 1 attenuate user data		—
Digital Offset	$(-0.4 \times \text{Vertical Range})$ to $(+0.4 \times \text{Vertical Range})$		Applied after Digital Gain.

Specification	Value		Comments
Output	$(ADC\ Data \times Digital\ Gain) + Digital\ Offset$		$(-0.5 \times Vertical\ Range) \leq Output \leq (+0.5 \times Vertical\ Range)$
Numerically-Controlled Oscillator (NCO)			
Frequency Range	Internal Sample Clock Timebase	External Sample Clock Timebase	Undersampling can be used for carrier frequencies $>75\text{ MHz}$.
	0 MHz to 75 MHz	0 Hz to $(0.5 \times Sample\ Clock\ Timebase)$	
Frequency Resolution	533 nHz	Sample Clock Timebase / 2^{48}	—
I and Q Phase Resolution	0.0055°		—
Digital Performance			
Maximum NCO Spur	$<-100\text{ dBFS}$		—
Decimating Filter Passband Ripple	$<0.1\text{ dB}$		Passband is from 0 to $(0.4 \times IQ\ Rate)$.
Decimating Filter Out-of-Band Suppression	$>80\text{ dB}$		Stopband suppression from $(0.6 \times IQ\ Rate)$.

Specification	Value				Comments
IF Demodulation Typical Performance: Modulation Error Ratio (MER)					
	Bandpass Path Carrier Frequency: 187.5 MHz		Direct Path Carrier Frequency: 20 MHz		
	Reference Clocks: Internal (Unlocked)	Reference Clocks: PXIe Chassis	Reference Clocks: Internal (Unlocked)	Reference Clocks: PXIe Chassis	
GSM Physical Layer ¹	50 dB	59 dB	48 dB	62 dB	For the Bandpass Path, the NI PXIe-5673 is the signal source. For the Direct path, the NI PXI-5441 is the signal source. In the <i>Unlocked</i> specification, both source and receiver use internal clocks and are not locked to any external reference. In the <i>PXIe-Chassis</i> specification, both source and receiver are locked to the PXIe 100 MHz (or PXI 10 MHz) chassis backplane clock.
W-CDMA Physical Layer ²	47 dB	50 dB	39 dB	58 dB	
DVB Physical Layer ³	46 dB	48 dB	40 dB	56 dB	
20 MSymbols/s QAM ⁴	43 dB	44 dB	37 dB	49 dB	
26 MSymbols/s QAM ⁵	39 dB	37 dB	36 dB	40 dB	
34 MSymbols/s QAM ⁶	38 dB	37 dB	38 dB	37 dB	
¹ Typical. MSK modulation, 270.833 kSymbols/s, 1024 Symbols, Gaussian, BT = 0.3 ² Typical. QPSK modulation, 3.84 MSymbols/s, 1024 Symbols, root raised cosine, alpha = 0.22 ³ Typical. 32 QAM modulation, 6.92 MSymbols/s, 1024 Symbols, root raised cosine, alpha = 0.15 ⁴ Typical. 64 QAM modulation, 20 MSymbols/s, 1024 Symbols, root raised cosine, alpha = 0.15 ⁵ Typical. 64 QAM modulation, 26.09 MSymbols/s, 1024 Symbols, root raised cosine, alpha = 0.15 ⁶ Typical. 64 QAM modulation, 34.78 MSymbols/s, 1024 Symbols, root raised cosine, alpha = 0.15. Note: In this case, Direct Path data is at a Center Frequency of 35 MHz using the NI PXIe-5450 as the source.					

Calibration

Specification	Value
Self-calibration	Calibrates absolute amplitude accuracy.
External Calibration	Calibrates absolute and relative (flatness) amplitude accuracy, VCXO accuracy.
External Calibration Interval	1 year
Warm-Up Time	15 minutes

Power

Specification	Value	Comments
Maximum Power Consumption		
+3.3 VDC	1.75 A	At highest operating temperature.
+12 VDC	2.25 A	
Total Power	32.8 W	

Software

Specification	Value
Driver Software	NI-SCOPE 3.5 or later. NI-SCOPE is an IVI-compliant driver that allows you to configure, control, and calibrate the NI PXIe-5622. NI-SCOPE provides application programming interfaces for many development environments.
Application Software	NI-SCOPE provides programming interfaces, documentation, and examples for the following application development environments: <ul style="list-style-type: none"> • LabVIEW • LabWindows™/CVI™ • Measurement Studio • Microsoft Visual C/C++ • Microsoft Visual Basic
Interactive Soft Front Panel and Configuration	The NI-SCOPE Soft Front Panel 2.9 or later supports interactive control of the NI PXIe-5622. The NI-SCOPE Soft Front Panel is included on the NI-SCOPE CD.
Test Panel	National Instruments Measurement & Automation Explorer (MAX) provides Test Panels with basic resource ID configuration. MAX is included on the NI-SCOPE CD.

Environment



Note To ensure that the NI PXIe-5622 cools effectively, follow the guidelines in the *Maintain Forced Air Cooling Note to Users* included in the NI PXIe-5622 kit. The NI PXIe-5622 is intended for indoor use only.

Specification	Value
Operating Temperature	0 °C to +55 °C in all NI PXI Express chassis.
Storage Temperature	–20 °C to +70 °C. Meets IEC 60068-2-1 and IEC-60068-2-2.
Operating Relative Humidity	10% to 90%, noncondensing. Meets IEC 60068-2-56.
Storage Relative Humidity	5% to 95%, noncondensing. Meets IEC 60068-2-56.

Specification	Value
Operating Shock	30 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.
Storage Shock	50 g, half-sine, 11 ms pulse. Meets IEC 60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.
Operating Vibration	5 Hz to 500 Hz, 0.31 g _{rms} . Meets IEC 60068-2-64.
Storage Vibration	5 Hz to 500 Hz, 2.46 g _{rms} . Meets IEC 60068-2-64. Test profile exceeds requirements of MIL-PRF-28800F, Class 3.
Altitude	0–2,000 m (at 25 °C ambient temperature)
Pollution Degree	2

Safety, Electromagnetic Compatibility, and CE Compliance

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note For the standards applied to assess the EMC of this product, refer to the *Online Product Certification* section.



Note For EMC compliance, operate this device with RG223/U or equivalent shielded cable. Operate this product according to the documentation.

CE Compliance

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）



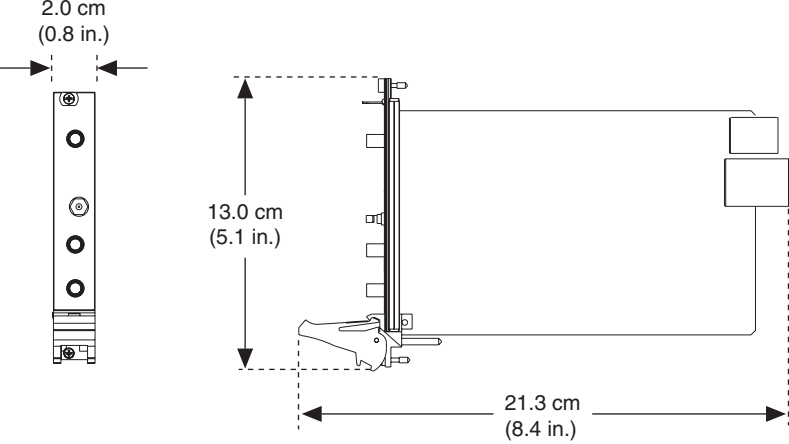
中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Physical

Front Panel Connectors

Label	Function	Connector Type
IF IN	Analog Input	SMA jack
PFI 1	PFI 1 Bi-directional Connector	SMB jack
CLK IN	Sample Clock Input and Reference Clock Input	SMA jack
CLK OUT	Sample Clock Output and Reference Clock Output	SMA jack
LEDs		
ACCESS	The ACCESS LED indicates the status of the PCIe bus and the interface from the NI PXIe-5622 to the controller.	
ACTIVE	The ACTIVE LED indicates the status of the onboard acquisition hardware of the NI PXIe-5622.	

Dimensions and Weight

Dimensions	<p>3U, One slot, PXI/cPCI Module, PXIe compatible 21.6 × 2.0 × 13.0 cm (8.5 × 0.8 × 5.1 in.)</p>  <p>The diagram illustrates the dimensions of the module. The front view shows a width of 2.0 cm (0.8 in.). The side view shows a height of 13.0 cm (5.1 in.) and a depth of 21.3 cm (8.4 in.). The module is a 3U, one-slot PXI/cPCI module, PXIe compatible.</p>
Weight	400 g (14.1 oz)

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At ni.com/support you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

A Declaration of Conformity (DoC) is our claim of compliance with the Council of the European Communities using the manufacturer's declaration of conformity. This system affords the user protection for electronic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification. If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at ni.com/support and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, contact your local branch office:

Australia 1800 300 800, Austria 43 662 457990-0,
Belgium 32 (0) 2 757 0020, Brazil 55 11 3262 3599,
Canada 800 433 3488, China 86 21 5050 9800,
Czech Republic 420 224 235 774, Denmark 45 45 76 26 00,
Finland 358 (0) 9 725 72511, France 01 57 66 24 24,
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