

IEEE 488.2 Controller Chip

Drop-In Replacement for NEC μ PD7210

NAT7210

Pin-compatible with NEC μ PD7210
 Software-compatible with NEC μ PD7210 or TI TMS9914A controller chips
 Low power consumption
 Meets all IEEE 488.2 requirements
 Bus line monitoring
 Preferred implementation of requesting service
 Does not send messages when there are no listeners
 Performs all IEEE 488.1 interface functions SH1, AH1, T5 or TE5, L3 or LE3, SR1, RL1, PP1, PP2, DC1, DT1, C1, C2, C3, C4, C5
 Reduces driver overhead
 Does not lose a data byte if ATN is asserted while transmitting data
 Static interrupt status bits that do not clear when read

Programmable data transfer rate (T1 delays of 350 ns, 500 ns, 1.1 μ s, and 2 μ s)
 Internal timer interrupt
 Automatic EOS and/or NL message detection
 Direct memory access (DMA)
 Automatically processes IEEE 488 commands and reads undefined commands
 Programmable compatible with bus transceivers (TI, National Semiconductor, Motorola, and Intel)
 TTL-compatible CMOS device
 Programmable clock rate up to 20 MHz



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Overview

The NAT7210 is a 40-pin DIP drop-in replacement part for the NEC μ PD7210. The NAT7210 is 100 percent register and pin-compatible with the NEC μ PD7210 on power up and has additional features present on the NAT4882 IEEE 488.2 controller chip. Thus, the NAT7210 can perform all the interface functions defined by the ANSI/IEEE Standard 488.1-1987 and meets the additional requirements and recommendations of ANSI/IEEE Standard 488.2-1987. The NAT7210 performs complete IEEE 488 talker, listener, and controller functions.

On power up, the NAT7210 contains the complete register set of the NEC μ PD7210, but is capable of complete IEEE 488.2 controller functionality through software. An instrument developer can take advantage of IEEE 488.2 with minimal software modifications, yet retain the 40-pin hardware configuration. The default clock input is 8 MHz; however, other input values up to 20 MHz are software-selectable in the NAT7210 for increased performance. The NAT7210 can also switch to the TI 9914 register-compatible mode with a software command.

IEEE 488 instrument manufacturers looking for alternatives to existing NEC μ PD7210 chip suppliers and/or planning to upgrade their designs to IEEE 488.2 without hardware changes should consider using the NAT7210. Because the NAT7210 can accept faster clock inputs, performance increases without many firmware changes.

General

The NAT7210 manages the IEEE 488 bus. You program the IEEE 488 bus by writing control words into the appropriate registers. CPU-readable status registers supply operational feedback. The NAT7210 mode determines the function of these registers. When in 7210 mode, the registers resemble the μ PD7210 register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. In this mode, the NAT7210 is completely pin-compatible with the NEC μ PD7210. When in 9914A mode, the registers resemble the TMS9914A register set with additional registers that supply extra functionality and IEEE 488.2 compatibility. Figure 2 shows the key components of the NAT7210.

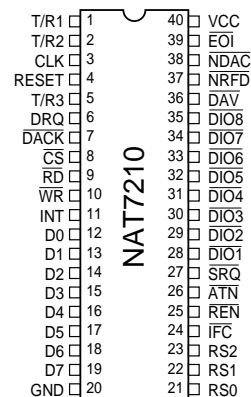


Figure 1. NAT7210 Pin Configuration

Ordering Information

NAT7210 ASICNAT7210BPD
 NAT7210 reference manual320744-01
 NAT7210 sample kit.....776730-11

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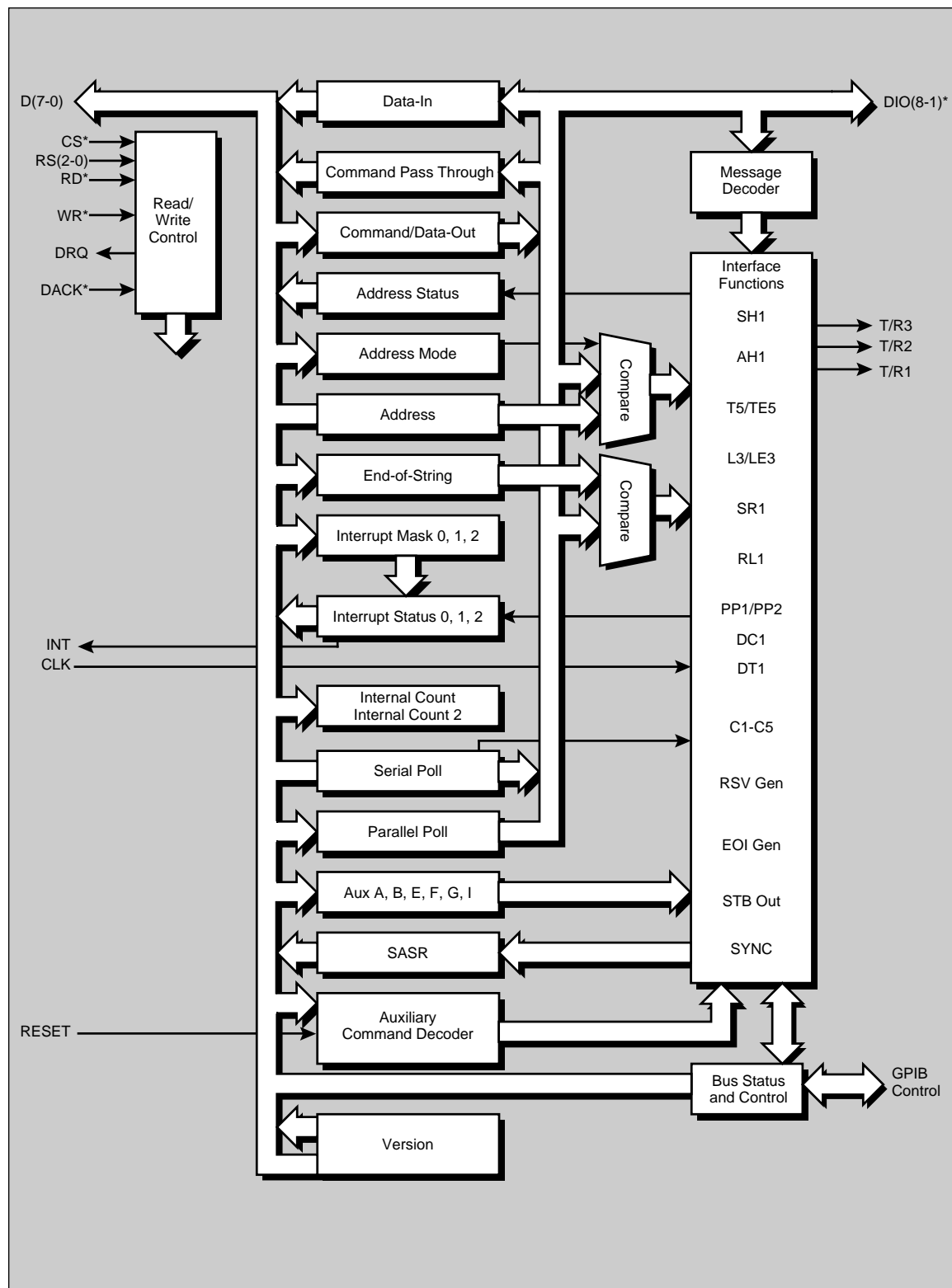


Figure 2. NAT7210 Block Diagram

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Pin Descriptions

The following table describes the NAT7210 pins. For more information refer to the NAT7210 reference manual available at www.ni.com

Pin Identification

Pin No.	Mnemonic	Type	Description
19, 18, 17, 16, 15, 14, 13, 12	D(7-0)	I/O'	Bidirectional 3-state data bus transfers commands, data, and status between the NAT7210 and the CPU
23, 22, 21	RS(2-0)	I'	The register selects determine which register to access during a read or write operation
8	CS*	I	Chip select gives access to the register selected by a read or write operation and the register selects RS(2-0)
9	RD*	I	With the read input, you can place the contents of the register that RS(2-0) and CS* selects onto the data bus D(7-0)
10	WR*	I'	The write input latches the contents of the data bus D(7-0) into the register that RS(2-0) selects
7	DACK*	I'	The DMA acknowledge signal selects the DIR or CDOR for the current read or write cycle
6	DRQ	O	The DMA Request output asserts to request a DMA acknowledge cycle
3	CLK	I	The CLK input can be up to 20 MHz
4	RESET	I	Asserting the reset input places the NAT7210 in an initial, idle state
11	INT	O'	The Interrupt output asserts when one of the unmask interrupt conditions is true
24	IFC*	I/O'	Bidirectional control line initializes the IEEE 488 interface functions
25	REN*	I/O'	Bidirectional control line selects either remote or local control of devices
26	ATN*	I/O'	Bidirectional control line indicates whether data on the DIO lines is an interface or device-dependent message
27	SRQ*	I/O'	Bidirectional control line requests service from the Controller
35, 34, 33, 32, 31, 30, 29, 28	DIO(8-1)*	I/O'	8-bit bidirectional IEEE 488 data bus
36	DAV*	I/O'	Handshake line indicates that the data on the DIO(8-1)* lines is valid
37	NRFD*	I/O'	Handshake line indicates that the device is ready for data
38	NDAC*	I/O'	Handshake line indicates the completion of a message reception
39	EOI*	I/O'	Bidirectional control line indicates the last byte of a data message or executes a parallel poll
1	T/R1	O	Talk Enable controls the direction of the IEEE 488 data transceiver
5	T/R3	O	These pins are the input/output control for the IEEE 488 transceivers
2	T/R2	O	
40	VCC	-	Power pin +5 V ($\pm 5\%$)
20	GND	-	Ground pin - 0 V

*The pin contains an internal pull-up resistor of 25 to 100 k Ω .

* Active low.

Table 1. NAT7210 APD Pin Configuration

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Drop-In Replacement for NEC μ PD7210

7210 Mode Registers

In 7210 mode, the NAT7210 registers include all the NEC μ PD7210 registers plus two types of additional registers – extra auxiliary registers and paged-in registers. You write the extra auxiliary registers the same as standard μ PD7210 auxiliary registers. Upon issuing an auxiliary page-in command, the paged-in registers appear at the same offsets as existing μ PD7210 registers. At the end of the next CPU access, the chip pages out the paged-in registers. The following table lists all the registers in the 7210 mode register set.

For programming information, refer to the NAT7210 reference manual available at www.ni.com

7210 Register Set

Register	PAGE-IN	A(2-0)	WR*	RD*	CS*	DAK*
Data-in	U	0 0 0	1	0	0	1
Data-in	X	X X X	1	0	X	0
Command/data-out	U	0 0 0	0	1	0	1
Command/data-out	X	X X X	0	1	X	0
Interrupt status 1	U	0 0 1	1	0	0	1
Interrupt mask 1	U	0 0 1	0	1	0	1
Interrupt status 2	U	0 1 0	1	0	0	1
Interrupt mask 2	U	0 1 0	0	1	0	1
Serial Poll status	N	0 1 1	1	0	0	1
Serial Poll mode	N	0 1 1	0	1	0	1
Version	P	0 1 1	1	0	0	1
Internal counter 2	P	0 1 1	0	1	0	1
Address status	U	1 0 0	1	0	0	1
Address mode	U	1 0 0	0	1	0	1
Command pass through	N	1 0 1	1	0	0	1
Auxiliary mode	U	1 0 1	0	1	0	1
Source/acceptor status [†]	P	1 0 1	1	0	0	1
Address 0	N	1 1 0	1	0	0	1
Address	N	1 1 0	0	1	0	1
Interrupt status 0 [†]	P	1 1 0	1	0	0	1
Interrupt mask 0 [†]	P	1 1 0	0	1	0	1
Address 1	N	1 1 1	1	0	0	1
End-of-string	N	1 1 1	0	1	0	1
Bus status [†]	P	1 1 1	1	0	0	1
Bus control [†]	P	1 1 1	0	1	0	1

Notes for the Page-In column

U = The page-in auxiliary command does not affect the register.

N = The register offset is always valid except for immediately after a page-in auxiliary command.

P = The register is valid only immediately after a page-in auxiliary command.

The '†' symbol denotes features (such as registers and auxiliary commands) that are not available in the μ PD7210 or TMS9914A.

9914 Mode Registers

In 9914 mode, the NAT7210 registers consist of all the TI TMS9914A registers and two types of additional registers – newly defined registers and paged-in registers. The NAT7210 maps the newly defined registers into the unused portion of the 9914 address space. Each paged-in register appears at offset two immediately after you issue an auxiliary page-in command and remains there until you either page another register into the same space or issue a reset. The following table lists all the registers in the 9914 register set. See the NAT7210 reference manual available at www.ni.com for more information.

9914 Register Set

Register	Page In	RS(2-0)	WR*	RD*	CS*	DAK*
Interrupt status 0	U	0 0 0	1	0	0	1
Interrupt mask 0	U	0 0 0	0	1	0	1
Interrupt status 1	U	0 0 1	1	0	0	1
Interrupt mask 1	U	0 0 1	0	1	0	1
Address status	U	0 1 0	1	0	0	1
Interrupt mask 2 [†]	P	0 1 0	0	1	0	1
End-of-string [†]	P	0 1 0	0	1	0	1
Bus control [†]	P	0 1 0	0	1	0	1
Accessory [†]	P	0 1 0	0	1	0	1
Bus status	U	0 1 1	1	0	0	1
Auxiliary command	U	0 1 1	0	1	0	1
Interrupt status 2 [†]	P	1 0 0	1	0	0	1
Address	U	1 0 0	0	1	0	1
Serial poll status [†]	P	1 0 1	1	0	0	1
Serial poll mode	U	1 0 1	0	1	0	1
Command pass thru	U	1 1 0	1	0	0	1
Parallel poll	U	1 1 0	0	1	0	1
Data-in	U	1 1 1	1	0	0	1
Data-in	U	X X X	1	0	X	0
Command/data-out	U	1 1 1	0	1	0	1
Command/data-out	U	X X X	0	1	X	0

Notes for the Page-In column

U = Page-in auxiliary commands do not affect the register offset.

P = The register offset is valid only after a page-in auxiliary command.

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DC Characteristics

T_A 0 to 70 °C; $V_{CC} = 5\text{ V} \pm 5\%$

Parameter	Symbol	Limits		Unit	Test Condition
		Min	Max		
Voltage input low	V_{IL}	-0.5	+0.8	V	
Voltage input high	V_{IH}	+2.0	V_{CC}	V	
Voltage output low	V_{OL}	0	0.4	V	
Voltage output high	V_{OH}	+2.4	V_{CC}	V	
Input/output leakage current		-10	+10	μ A	without internal pull up
Input/output leakage current		-200	+200	μ A	with internal pull up
Supply current			45	mA	
Output current low					
All pins except T/R1	I_{OL}	2		mA	$V_{OL} = 0.4\text{ V}$
T/R1	I_{OL}	4		mA	$V_{OL} = 0.4\text{ V}$
Input current low/high	I_{IL}		-0.5	mA	
Output current high	I_{OH}	-1		mA	$V_{OH} = V_{CC} - 0.5\text{ V}$
Supply voltage	V_{CC}	4.75	5.25	V	

Capacitance

T_A 0 to 70 °C; $V_{CC} = 5\text{ V} \pm 5\%$

Parameter	Symbol	Limits		Unit	Test Condition
		Min	Max		
Input capacitance	C_{in}		10	pF	
Output capacitance	C_{out}		10	pF	
I/O capacitance	$C_{I/O}$		10	pF	

Absolute Maximum Ratings

Property	Range
Supply voltage, V_{CC}	-0.5 to +6.0 V
Input voltage, V_I	-0.5 to $V_{CC} + 0.5$
Operating temperature, T_{OPR}	0 to +70 °C
Storage temperature, T_{STG}	-40 to +125 °C

Comment – exposing the device to stresses above those listed could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC Characteristics

T_A 0 to 70 °C; $V_{CC} = 5\text{ V} \pm 5\%$

Parameter	Symbol	Limits		Unit	Test Condition
		Min	Max		
Address hold from $\overline{RD} \uparrow, \overline{WR} \uparrow$	t_{AH}	0		ns	
Address setup to $\overline{RD} \downarrow, \overline{WR} \downarrow$	t_{AS}	0		ns	
Data float from $\overline{RD} \uparrow$	t_{DF}		25	ns	
Data delay from $\overline{RD} \downarrow$	t_{DR}		80	ns	$\overline{DACK} = 0$
DRQ unassertion	t_{DU}		25	ns	
Data delay from $\overline{RD} \downarrow$	t_{RD}		85	ns	$\overline{CS} = 0$
RD recovery width	t_{RR}	120		ns	
RD pulse width	t_{RW}	85		ns	
Data setup to $\overline{WR} \uparrow$	t_{WS}	60		ns	
Data hold from $\overline{WR} \uparrow$	t_{WH}	0		ns	

Timing Waveforms

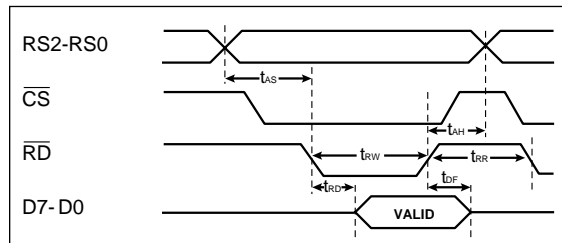


Figure 3. CPU Read

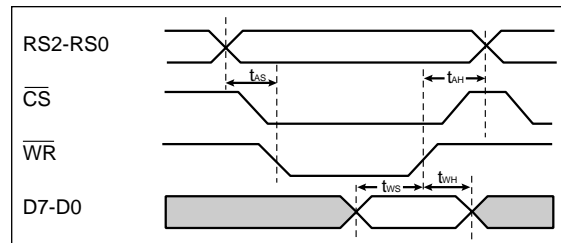


Figure 5. CPU Write

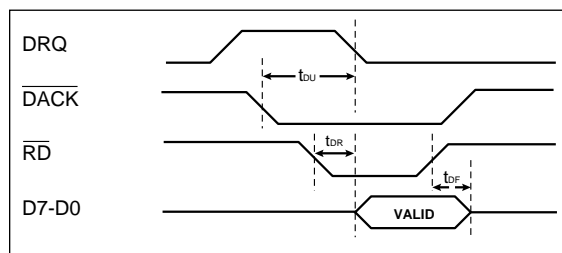


Figure 4. DMA Read

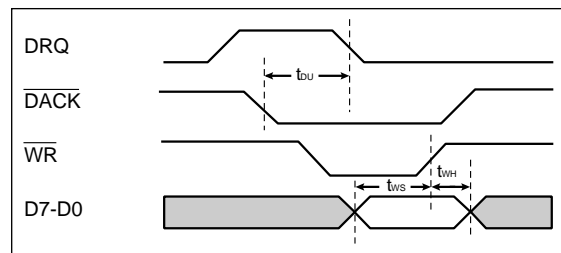


Figure 6. DMA Write

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Source Handshake

Parameter	Symbol	Limits (ns)		Test Condition
		Min	Max	
$\overline{\text{NDAC}} \uparrow$ to $\overline{\text{DAV}} \uparrow$	t_{ND}		40	
$\overline{\text{NDAC}} \uparrow$ to $\overline{\text{INT}} \uparrow$ or $\overline{\text{DRQ}} \uparrow$	t_{NI}		40	INT (DIIE Bit = 1) DRQ (DMAO Bit = 1)
$\overline{\text{WR}} \uparrow$ to $\overline{\text{DAV}} \downarrow$	t_{WD}	2,000	2,125	2 μ s T1 (8 MHz, 50% duty)
$\overline{\text{WR}} \uparrow$ to $\overline{\text{DAV}} \downarrow$	t_{WD}	1,125	1,250	1.1 μ s T1 (8 MHz, 50% duty)
$\overline{\text{WR}} \uparrow$ to $\overline{\text{DAV}} \downarrow$	t_{WD}	500	625	500 ns T1 (8 MHz, 50% duty)
$\overline{\text{WR}} \uparrow$ to $\overline{\text{DAV}} \downarrow$	t_{WD}	375	500	350 ns T1 (8 MHz, 50% duty)

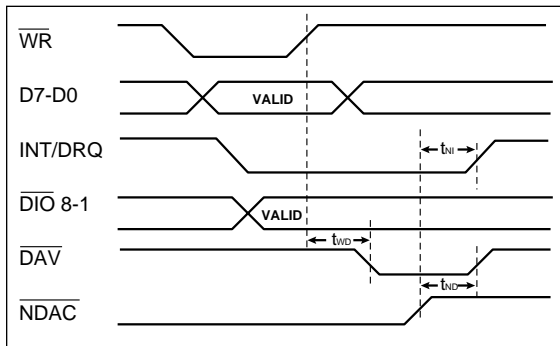


Figure 7. Source Handshake

Acceptor Handshake

Parameter	Symbol	Limits (ns)		Test Condition
		Min	Max	
$\overline{\text{DAV}} \downarrow$ to $\overline{\text{NDAC}} \uparrow$	t_{DD}		225	8 MHz 50% duty
$\overline{\text{DAV}} \uparrow$ to $\overline{\text{NDAC}} \downarrow$	t_{DF}		20	
$\overline{\text{DAV}} \downarrow$ to $\overline{\text{INT}} \uparrow$ or $\overline{\text{DRQ}} \uparrow$	t_{DI}		116	INT (DIIE Bit = 1), DRQ (DMAI Bit = 1) 8 MHz, 50% duty
$\overline{\text{DAV}} \downarrow$ to $\overline{\text{NRFD}} \downarrow$	t_{DR}		25	
$\overline{\text{RD}} \uparrow$ to $\overline{\text{NRFD}} \uparrow$	t_{NR}		30	Read of DIR, not in Holdoff state

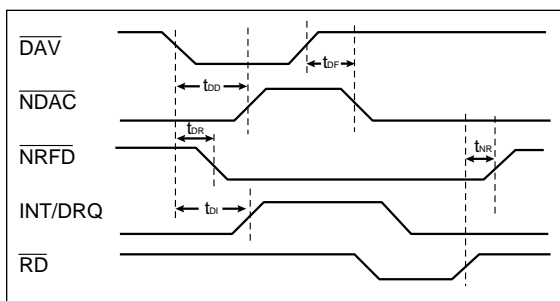


Figure 8. Acceptor Handshake

Response to ATN

Parameter	Symbol	Limits (ns)		Test Condition
		Min	Max	
$\overline{\text{ATN}} \uparrow$ to $\overline{\text{NRFD}} \downarrow$	t_{AF}		35	Acceptor handshake Holdoff
$\overline{\text{ATN}} \downarrow$ to $\overline{\text{NDAC}} \downarrow$	t_{AN}		35	AIDS \rightarrow ANRS
$\overline{\text{ATN}} \downarrow$ to $\overline{\text{TE}} \downarrow$	t_{AT}		30	TACS \rightarrow TADS

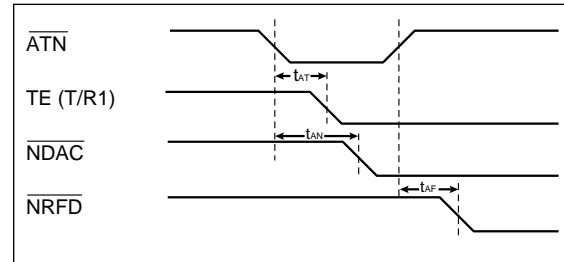


Figure 9. Response to WATN

Parallel Poll

Parameter	Symbol	Limits (ns)		Test Condition
		Min	Max	
$\overline{\text{EOI}} \downarrow$ to $\overline{\text{DIO}} \text{ valid}$	t_{ED}		90	PPSS \rightarrow PPAS
$\overline{\text{EOI}} \downarrow$ to $\overline{\text{TE}} \uparrow$	t_{ET}		25	PPSS \rightarrow PPAS
$\overline{\text{EOI}} \uparrow$ to $\overline{\text{TE}} \downarrow$	t_{TE}		25	PPAS \rightarrow PPSS

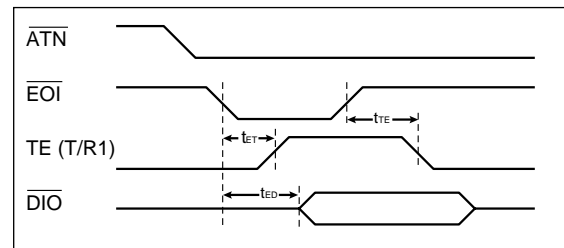


Figure 10. Parallel Poll

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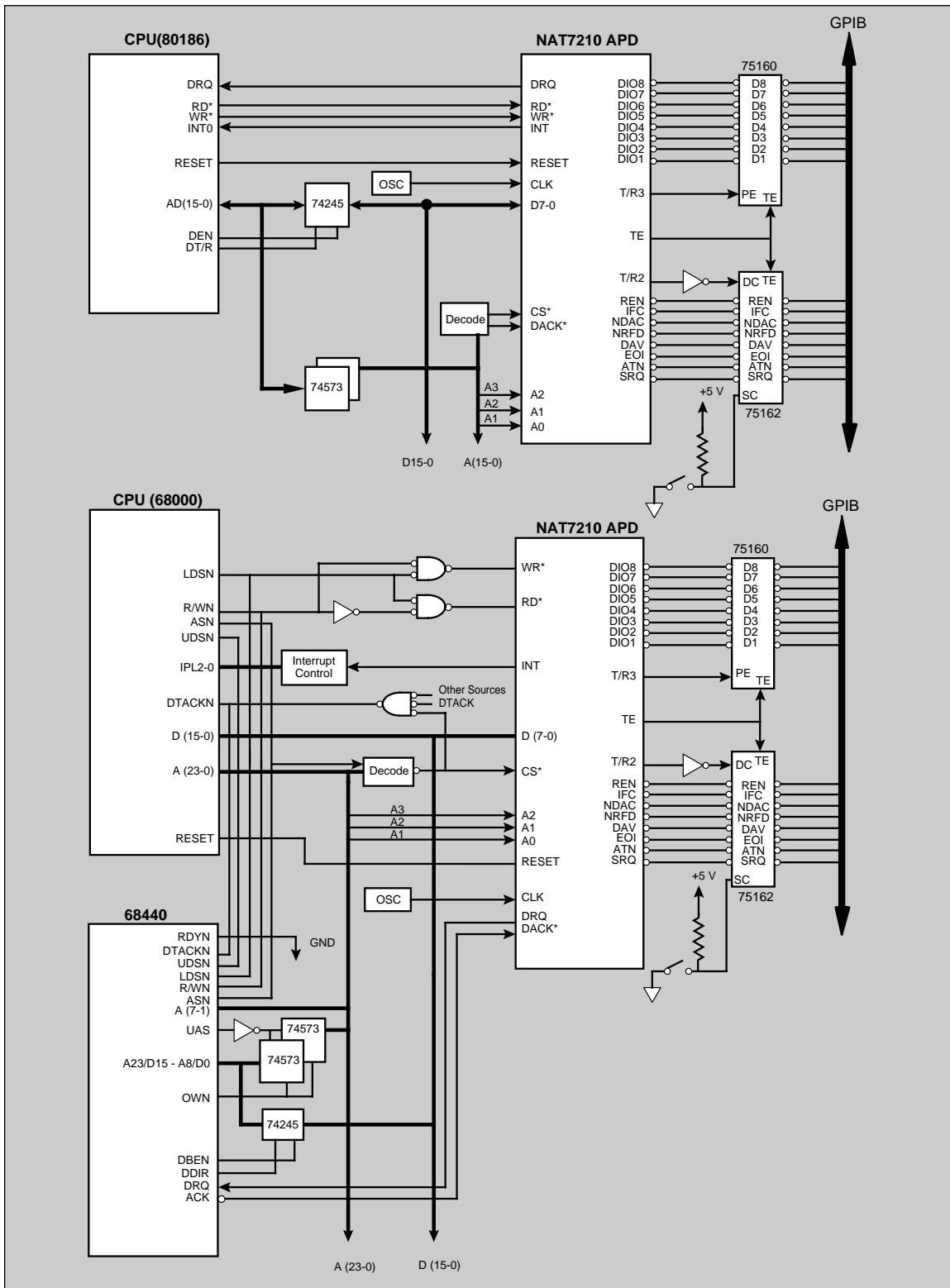


Figure 11. Typical CPU Systems with NAT7210 APD

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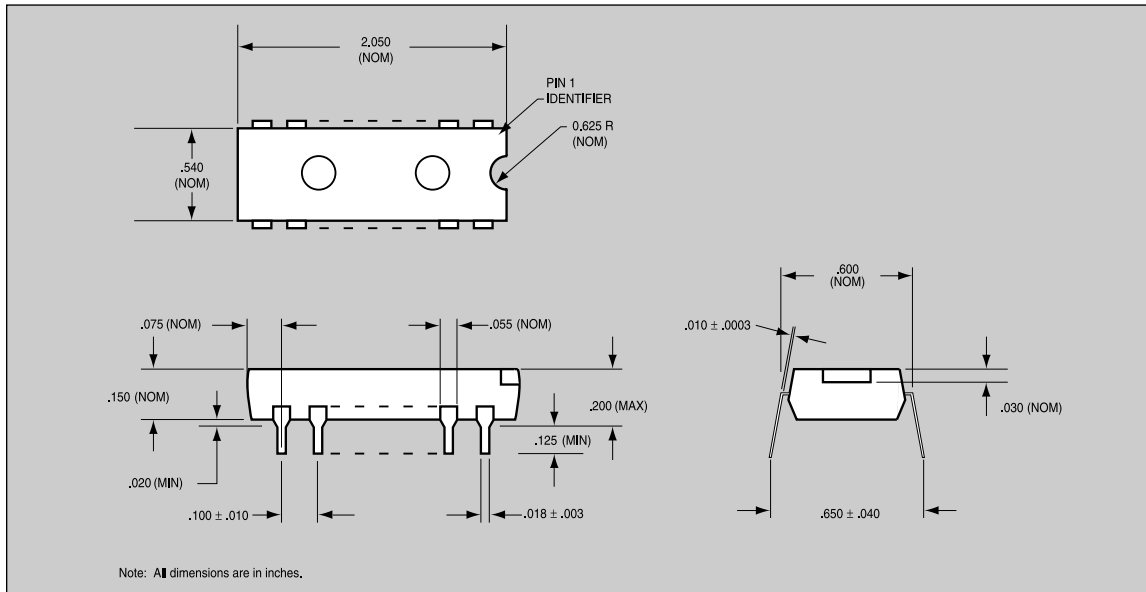


Figure 12. Mechanical Data 40-pin Plastic DIP

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