Worldwide Technical Support and Product Information

ni.com

Worldwide Offices
Visit ni.com/niglobal to access the branch office websites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

National Instruments Corporate Headquarters
11500 North Mopac Expressway  Austin, Texas 78759-3504  USA  Tel: 512 683 0100

For further support information, refer to the NI Services appendix. To comment on NI documentation, refer to the NI website at ni.com/info and enter the Info Code feedback.

© 2018 National Instruments. All rights reserved.
Legal Information

Limited Warranty
This document is provided "as is" and is subject to being changed, without notice, in future editions. For the latest version, refer to ni.com/manuals. NI reviews this document carefully for technical accuracy; however, NI MAKES NO EXPRESS OR IMPLIED WARRANTIES AS TO THE ACCURACY OF THE INFORMATION CONTAINED HEREIN AND SHALL NOT BE LIABLE FOR ANY ERRORS.

NI warrants that its hardware products will be free of defects in materials and workmanship that cause the product to fail to substantially conform to the applicable NI published specifications for one (1) year from the date of invoice.

For a period of ninety (90) days from the date of invoice, NI warrants that (i) its software products will perform substantially in accordance with the applicable documentation provided with the software and (ii) the software media will be free from defects in materials and workmanship.

If NI receives notice of a defect or non-conformance during the applicable warranty period, NI will, in its discretion: (i) repair or replace the affected product, or (ii) refund the fees paid for the affected product. Repaired or replaced Hardware will be warranted for the remainder of the original warranty period or ninety (90) days, whichever is longer. If NI elects to repair or replace the product, NI may use new or refurbished parts or products that are equivalent to new in performance and reliability and are at least functionally equivalent to the original part or product.

You must obtain an RMA number from NI before returning any product to NI. NI reserves the right to charge a fee for examining and testing Hardware not covered by the Limited Warranty.

This Limited Warranty does not apply if the defect of the product resulted from improper or inadequate maintenance, installation, repair, or calibration (performed by a party other than NI); unauthorized modification; improper environment; use of an improper hardware or software key; improper use or operation outside of the specification for the product; improper voltages; accident, abuse, or neglect; or a hazard such as lightning, flood, or other act of nature.

THE REMEDIES SET FORTH ABOVE ARE EXCLUSIVE AND THE CUSTOMER'S SOLE REMEDIES, AND SHALL APPLY EVEN IF SUCH REMEDIES FAIL OF THEIR ESSENTIAL PURPOSE.

EXCEPT AS EXPRESSLY SET FORTH HEREIN, PRODUCTS ARE PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND AND NI DISCLAIMS ALL WARRANTIES, EXPRESSED OR IMPLIED, WITH RESPECT TO THE PRODUCTS, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, TITLE OR NON-INFRINGEMENT, AND ANY WARRANTIES THAT MAY ARISE FROM USAGE OF TRADE OR COURSE OF DEALING. NI DOES NOT WARRANT, GUARANTEE, OR MAKE ANY REPRESENTATIONS REGARDING THE USE OF OR THE RESULTS OF THE USE OF THE PRODUCTS IN TERMS OF CORRECTNESS, ACCURACY, RELIABILITY, OR OTHERWISE. NI DOES NOT WARRANT THAT THE OPERATION OF THE PRODUCTS WILL BE UNINTERRUPTED OR ERROR FREE.

In the event that you and NI have a separate signed written agreement with warranty terms covering the products, then the warranty terms in the separate agreement shall control.

Copyright
Under the copyright laws, this publication may not be reproduced or transmitted in any form, electronic or mechanical, including photocopying, recording, storing in an information retrieval system, or translating, in whole or in part, without the prior written consent of National Instruments Corporation.

National Instruments respects the intellectual property of others, and we ask our users to do the same. NI software is protected by copyright and other intellectual property laws. Where NI software may be used to reproduce software or other materials belonging to others, you may use NI software only to reproduce materials that you may reproduce in accordance with the terms of any applicable license or other legal restriction.

End-User License Agreements and Third-Party Legal Notices
You can find end-user license agreements (EULAs) and third-party legal notices in the following locations:

- Notices are located in the <National Instruments>_Legal Information and <National Instruments>_Shared\MDF\Legal\license directories.
- EULAs are located in the <National Instruments>_Shared\MDF\Legal\license directory.
- Review <National Instruments>_Legal Information.txt for information on including legal information in installers built with NI products.

U.S. Government Restricted Rights
If you are an agency, department, or other entity of the United States Government ("Government"), the use, duplication, reproduction, release, modification, disclosure or transfer of the technical data included in this manual is governed by the Restricted Rights provisions under Federal Acquisition Regulation 52.227-14 for civilian agencies and Defense Federal Acquisition Regulation Supplement Section 252.227-7014 and 252.227-7015 for military agencies.

Trademarks
Refer to the NI Trademarks and Logo Guidelines at ni.com/trademarks for more information on National Instruments trademarks.

ARM, Keil, and µVision are trademarks or registered of ARM Ltd or its subsidiaries.

LEGO, the LEGO logo, WEDO, and MINDSTORMS are trademarks of the LEGO Group.

TETRIX by Pitsco is a trademark of Pitsco, Inc.

FIELDBUS FOUNDATION™ and FOUNDATION™ are trademarks of the Fieldbus Foundation.
About This Manual

The PXIe-1084 Series User Manual describes the features of the PXIe-1084 chassis and contains information about configuring the chassis, installing the modules, and operating the chassis.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- PICMG EXP.0 R1.0 CompactPCI Express Specification, PCI Industrial Computers Manufacturers Group
- PCI Express Base Specification, Revision 1.1, PCI Special Interest Group
- PXI-5 PXI Express Hardware Specification, Revision 2.0, PXI Systems Alliance
Getting Started

This chapter describes the key features of the PXIe-1084 chassis and lists the kit contents and optional equipment you can order from National Instruments.

Unpacking

Carefully inspect the shipping container and the chassis for damage. Check for visible damage to the metal work. Check to make sure all handles, hardware, and switches are undamaged. Inspect the inner chassis for any possible damage, debris, or detached components. If damage appears to have been caused during shipment, file a claim with the carrier. Retain the packing material for possible inspection and/or reshipment.

What You Need to Get Started

The PXIe-1084 chassis kit contains the following items:

☐ PXIe-1084 chassis
☐ Filler panels
☐ PXIe-1084 Safety, Environmental, and Regulatory Information
☐ Software media with PXI Platform Services 17.5 or newer
☐ Chassis number labels

⚠️ Note ⚠️ You will also need an AC power cable, sold separately. Refer to Table 1-1 for more information about AC power cables.
Chapter 1  Getting Started

Table 1-1. AC Power Cables

<table>
<thead>
<tr>
<th>Power Cable</th>
<th>Plug Types</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard 120 V (USA)</td>
<td>ANSI C73.11/NEMA 5-15-P</td>
</tr>
<tr>
<td>Switzerland 220 V</td>
<td>SEV 6534-2</td>
</tr>
<tr>
<td>Australia 240 V</td>
<td>AS C112</td>
</tr>
<tr>
<td>Universal Euro 230 V</td>
<td>CEE (7), II, IV, VII</td>
</tr>
<tr>
<td>United Kingdom 230 V</td>
<td>BS 1363</td>
</tr>
<tr>
<td>Japan 100 V</td>
<td>JIS 8303</td>
</tr>
</tbody>
</table>

If you are missing any of the items listed in Table 1-1, or if you have the incorrect AC power cable, contact National Instruments.

Key Features

The PXIe-1084 chassis combines a high-performance 18-slot PXI Express backplane with a power supply and a structural design that has been optimized for maximum usability in a wide range of applications. The PXIe-1084 chassis fully complies with the PXI-5 PXI Express Hardware Specification.

The key features of the PXIe-1084 chassis include the following:

High Performance for Instrumentation Requirements

- Up to 500 MB/s (single direction) per PXI Express slot dedicated bandwidth (x1 Gen-2 PCI Express).
- 58 W per slot cooling meets increased PXI Express cooling requirements. Refer to the PXIe-1084 Specifications for more details.
- Low-jitter internal 10 MHz reference clock for PXI/PXI Express slots with ± 25 ppm stability
- Low-jitter internal 100 MHz reference clock for PXI Express slots with ± 25 ppm stability
- Quiet operation for 0 to 30 °C at 34.4 dBA
- Variable speed fan controller optimizes cooling and acoustic emissions
- Complies with PXI and CompactPCI Specifications
High Reliability
• 0 to 50 °C temperature range
• Power supply, temperature, and fan monitoring
• Field replaceable fans

Additional, Optional Features
• Timing and Synchronization Upgrade
  – Rear panel CLK10 I/O connectors
  – High-density trigger ports for sharing multiple triggers between chassis
  – Remote power inhibit control and chassis monitoring
  – USB 3.0 port
• Front and rear rack-mount kits
• EMC filler panels
• Slot blockers for improved cooling performance
• Factory installation services
• Replacement fan kit
Chapter 1  Getting Started

Chassis Description

Figures 1-1 and 1-2 show the key features of the PXIe-1084 chassis front and back panels. Figure 1-1 shows the front view of the chassis. Figure 1-2 shows the rear view of the chassis.

Refer to Figure 2-2, PXIe-1084 Chassis Vents, for chassis vent locations.

Figure 1-1. Front View of the PXIe-1084 Chassis

1 System Controller Expansion Slot
2 Backplane Connectors
3 Removable Feet
4 PXI Express Hybrid Peripheral Slots (17x)
5 PXI Express System Controller Slot
6 Status LED
7 Power Inhibit Switch
8 DIP Switch
9 Chassis Carry Handle

Figure 1-2. Rear View of the PXIe-1084 Chassis

1 Timing and Synchronization Upgrade
2 Rear Panel Power Supply LED
3 Power Supply
4 Universal AC Input
5 Earth Ground Terminal
6 Fan Module
Optional Equipment

Contact National Instruments to order the following options for the PXIe-1084 chassis.

Timing and Synchronization
An optional timing and synchronization accessory available from National Instruments provides trigger routing capability, connectors for 10 MHz reference clock input and output, and remote chassis monitoring and inhibit control.

EMC Filler Panels
EMC filler panel kits are available from National Instruments.

Slot Blockers
PXI Slot Blocker kits are available from National Instruments for improved thermal performance when all slots are not used.

Replacement Fan Kit
A fan kit is available from National Instruments, includes both side and PXI module fan assemblies.

Rack Mount Kits
Rack mounting kits are available from National Instruments that can accommodate a variety of rack depths.

PXIe-1084 Backplane Overview
This section provides an overview of the backplane features for the PXIe-1084 chassis.

Interoperability with CompactPCI
The design of the PXIe-1084 chassis provides you the flexibility to use the following devices in a single PXI Express chassis:

- PXI Express compatible products
- CompactPCI Express compatible 2-Link system controller products
- CompactPCI Express compatible Type-2 peripheral products
- PXI peripheral products modified to fit in a hybrid slot
- Standard CompactPCI peripheral products modified to fit in a hybrid slot
System Controller Slot

The system controller slot is Slot 1 of the chassis and is a 2-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. It has three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane connects the system slot to two PCI Express switches using two Gen-2 x4 PCI Express links. These switches distribute PCI Express connections to the peripheral slots and to three PCI Express-to-PCI bridges to provide a PCI bus to the hybrid peripheral slots.

System slot link 1 is a Gen-2 x4 PCI Express link to PCI Express switch 1, providing a nominal bandwidth of 2 GB/s (single direction) between the system controller and PCI Express switch 1. PXI Express peripheral slots 2 to 10 are connected to PCI Express switch 1 with Gen-2 x1 PCI Express links and are downstream of system slot link 1. The PCI Express-to-PCI bridge 1 is connected to PCI Express switch 1 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 2 to 7.

System slot link 2 is a Gen-2 x4 PCI Express link to PCI Express switch 2, providing a nominal bandwidth of 2 GB/s (single direction) between the system controller slot and PCI Express switch 2. PXI Express peripheral slots 11 to 18 are connected to PCI Express switch 2 with Gen-2 x1 PCI Express links and are downstream of system slot link 2. The PCI Express-to-PCI bridge 2 is connected to PCI Express switch 2 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 8 to 13. The PCI Express-to-PCI bridge 3 is also connected to PCI Express switch 2 and provides a 32-bit, 33 MHz PCI bus for hybrid peripheral slots 14 to 18.

The system controller slot also has connectivity to some PXI features such as: PXI_CLK10, PXI Trigger Bus, and PXI Local Bus.

By default, the system controller will control the power supply with the PS_ON# signals. A logic low on this line will turn the power supply on.

**Note** The chassis Inhibit Mode must be set to Default mode for the system controller to control the power supply. Refer to the Inhibit Mode section of Chapter 2, Installation and Configuration, for details about configuring Inhibit Mode.
Hybrid Peripheral Slots

The chassis provides seventeen (17) hybrid peripheral slots as defined by the PXI-5 PXI Express Hardware Specification: slots 2 to 18. A hybrid peripheral slot can accept the following peripheral modules:

- A PXI Express peripheral with x8, x4, or x1 PCI Express link through a switch to the system slot. Each PXI Express peripheral slot can link up to a Gen-2 x1 PCI Express, providing a maximum nominal single-direction bandwidth of 500 MB/s.
- A CompactPCI Express Type-2 Peripheral with x8, x4, or x1 PCI Express link through a switch to the system slot.
- A hybrid-compatible PXI Peripheral module that has been modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2. Refer to the PXI Express Specification for details. The PXI Peripheral communicates through the backplane’s 32-bit PCI bus.
- A CompactPCI 32-bit peripheral on the backplane’s 32-bit PCI bus.

The hybrid peripheral slots provide full PXI Express functionality and 32-bit PXI functionality except for PXI Local Bus. The hybrid peripheral slot only connects to PXI Local Bus 6 left and right.

**Figure 1-3. PXIe-1084 PCI Express Backplane Diagram**
Chapter 1  Getting Started

PXI Local Bus
The PXI backplane local bus is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right.

The backplane routes PXI Local Bus 6 between all slots. Local bus signals may range from high-speed TTL signals to analog signals as high as 42 V.

Initialization software uses the configuration information specific to each adjacent peripheral module to evaluate local bus compatibility.

PXI Trigger Bus
All slots on the same PXI bus segment share eight PXI trigger lines. You can use these trigger lines in a variety of ways. For example, you can use triggers to synchronize the operation of several different PXI peripheral modules. Modules can pass triggers to one another, allowing precisely timed responses to asynchronous external events the system is monitoring or controlling.

The PXI trigger lines from adjacent PXI trigger bus segments can be routed in either direction across the PXI trigger bridges through buffers. This allows you to send trigger signals to, and receive trigger signals from, every slot in the chassis. Static trigger routing (user-specified line and directional assignments) can be configured through Measurement & Automation Explorer (MAX). Dynamic routing of triggers (automatic line assignments) is supported through certain National Instruments drivers like NI-DAQmx.

Note  Although any trigger line may be routed in either direction, it cannot be routed in more than one direction at a time.

With the Timing and Synchronization upgrade, PXI trigger lines can also be routed to I/O ports on the rear of the chassis. This allows you to send trigger signals to, and receive trigger signals from, devices in other chassis. National Instruments drivers such as NI-DAQmx must be used to route triggers between chassis dynamically; routing triggers between chassis using static routes defined in MAX is not supported.

*Figure 1-4. PXI Trigger Bus Connectivity Diagram*
System Reference Clock
The PXIe-1084 chassis supplies PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 independently driven to each peripheral slot.

Figure 1-5. Chassis Reference Clock Architecture

Note Dotted line connections are only available with the Timing and Synchronization upgrade

An independent buffer (having a source impedance matched to the backplane and a skew of less than 250 ps between slots) drives PXI_CLK10 to each slot. You can use this common reference clock signal to synchronize multiple modules in a measurement or control system.

An independent buffer drives PXIe_CLK100 to each peripheral slot. These clocks are matched in skew to less than 100 ps. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_CLK100 so that when there is no peripheral or a peripheral that does not connect to PXIe_CLK100, there is no clock being driven on the pair to that slot.

An independent buffer drives PXIe_SYNC100 to each peripheral slot. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_SYNC100 so that when there is no peripheral or a peripheral that does not connect to PXIe_SYNC100, there is no SYNC100 signal being driven on the pair to that slot.

The backplane uses a 100 MHz Voltage-Controlled Crystal Oscillator (VCXO) to directly create PXIe_CLK100 and does a divide-by-10 to create PXI_CLK10. Onboard logic synthesizes PXIe_SYNC100 from these two signals with the timing relationship shown in the following figure.
This architecture has the advantage that PXI_CLK10 and PXIe_CLK100 are always sourced from the same reference oscillator, and therefore it is impossible to lose PXI_CLK10 or PXIe_CLK100 by disconnecting a reference provided on any of the supported inputs. For the same reason, it is also impossible for a runt pulse or glitch to occur on these lines as references are switched in and out, protecting the integrity of digital circuitry operating on these clocks.

A feature of this architecture is that the phase noise performance of PXI_CLK10 and PXIe_CLK100 is fixed beyond the bandwidth of the PLL loop on the backplane, regardless of the quality of reference used. This is advantageous if a reference with poor phase noise performance is used, but it also means that supplying a high end, low phase noise reference will not greatly improve PXI_CLK10 or PXIe_CLK100.

10 MHz Input Reference

Several options are available to synchronize the system to an external clock:

- Drive a clock from an external source through the 10 MHz REF IN SMA on the rear of the chassis (Timing and Synchronization upgrade only).
- Connect a high-density trigger cable from the Trig Port 1/10 MHz Ref Out port of another chassis to the Trig Port 0/10 MHz REF IN port of this chassis (Timing and Synchronization upgrade only).

When an external clock is detected on any of these inputs, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots. Refer to the PXIe-1084 Specifications for the specification information for an external clock provided on the PXI_CLK10_IN pin of the rear panel SMA.
If an external clock is present more than one of these inputs, the signal is selected according to Table 1-2.

Table 1-2. Backplane External Clock Input Truth Table

<table>
<thead>
<tr>
<th>Rear 10 MHz REF IN SMA Connector</th>
<th>Trig Port 0/ 10 MHz REF IN Port</th>
<th>Backplane PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 MHz clock present</td>
<td>—</td>
<td>Phase-locked to Rear 10 MHz REF IN SMA</td>
</tr>
<tr>
<td>No clock present</td>
<td>10 MHz clock present</td>
<td>Phase-locked to Trig Port 0/10 MHz REF IN Port</td>
</tr>
<tr>
<td>No clock present</td>
<td>No clock present</td>
<td>Backplane generates its own clocks</td>
</tr>
</tbody>
</table>

10 MHz Output Reference

By default, a copy of the backplane’s PXI_CLK10 is exported to the 10 MHz REF OUT SMA connector as well as the Trig Port 1/10 MHz REF OUT port on the rear of the chassis. These clocks are driven by independent buffers. Refer to the PXIe-1084 Specifications for the specification information for the 10 MHz REF OUT signal on the rear SMA connector. This feature is only available with the Timing and Synchronization upgrade.
Installation and Configuration

This chapter describes how to prepare and operate the PXIe-1084 chassis.

Before connecting the chassis to a power source, read this chapter and the Read Me First: Safety and Electromagnetic Compatibility document included with your kit.

Safety Information

⚠️ **Cautions** Before undertaking any troubleshooting, maintenance, or exploratory procedure, carefully read the following caution notices.

Protection equipment may be impaired if equipment is not used in the manner specified.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

- **Chassis Grounding**—The chassis requires a connection from the premise wire safety ground to the chassis ground. The earth safety ground must be connected during use of this equipment to minimize shock hazards. Refer to the [Connecting the Safety Ground](#) section for instructions on connecting safety ground.

- **Live Circuits**—Operating personnel and service personnel must not remove protective covers when operating or servicing the chassis. Adjustments and service to internal components must be undertaken by qualified service technicians. During service of this product, the mains connector to the premise wiring must be disconnected. Dangerous voltages may be present under certain conditions; use extreme caution.

- **Explosive Atmosphere**—Do not operate the chassis in conditions where flammable gases are present. Under such conditions, this equipment is unsafe and may ignite the gases or gas fumes.

- **Part Replacement**—Only service this equipment with parts that are exact replacements, both electrically and mechanically. Contact National Instruments for replacement part information. Installation of parts with those that are not direct replacements may cause harm to personnel operating the chassis. Furthermore, damage or fire may occur if replacement parts are unsuitable.

- **Modification**—Do not modify any part of the chassis from its original condition. Unsuitable modifications may result in safety hazards.
Chapter 2  Installation and Configuration

Chassis Cooling Considerations

The PXIe-1084 Series chassis is designed to operate on a bench or in an instrument rack. You must adhere to the cooling clearances as outlined in the following section.

Providing Adequate Clearance

The module and power supply exhaust vents for the PXIe-1084 are on the top of the chassis. The module intake vents are on the rear of the chassis. The vent locations are shown in Figure 2-2, PXIe-1084 Chassis Vents.

Adequate clearance between the chassis and surrounding equipment, heat generating devices, and air flow blockages must be maintained to ensure proper cooling. Minimum cooling clearances are shown in Figure 2-1, PXIe-1084 Chassis Minimum Cooling Clearances. For rack mount applications adequate forced air ventilation is required. For benchtop applications additional cooling clearances may be required for optimal air flow and reduced hot air recirculation to the air inlet fans.

⚠️ Caution  Failure to provide these clearances may result in undesired thermal-related issues with the chassis or modules.

To aid in thermal health monitoring for either rack or benchtop use you can monitor the chassis intake temperatures in Measurement & Automation Explorer (MAX) to ensure the temperatures do not exceed the ratings in the Operating Environment section of the PXIe-1084 Specifications.

Additionally, many PXI modules provide temperature values you can monitor to ensure critical temperatures are not exceeded. Increasing chassis clearances, ventilation, reducing external ambient temperatures, and removing nearby heat sources are all options for improving overall chassis thermal performance.
Figure 2-1. PXIe-1084 Chassis Minimum Cooling Clearances

Dimensions are in inches (millimeters)

1.75 (44.45)

4.00 (101.60)
Chapter 2 Installation and Configuration

Figure 2-2. PXIe-1084 Chassis Vents

Note The side exhaust vent (not shown) is located on the left side of the chassis.
Chassis Ambient Temperature Definition

The chassis fan control system uses ambient intake air temperatures for controlling fan speeds when in Auto mode. These temperatures may be higher than ambient room temperature depending on surrounding equipment and/or blockages. Ensure ambient intake temperatures do not exceed the ratings in the Operating Environment section of the PXIe-1084 Specifications. The module and side ambient intake temperatures can be monitored in National Instruments Measurement and Automation Explorer (MAX).

Setting Fan Speed

The PXIe-1084 chassis supports multiple fan operating modes. Refer to the Fan Mode section for more information.

Installing Filler Panels

To maintain proper module cooling performance, install filler panels (provided with the chassis) in unused or empty slots. Secure with the captive mounting screws provided.

Installing Slot Blockers

The cooling performance of the chassis can be improved by installing optional slot blockers. Refer to the National Instruments website at ni.com/info and enter the Info Code slotblocker for more information about slot blockers.
Chapter 2  Installation and Configuration

Rack Mounting

Rack mount applications require optional rack mount kits available from National Instruments. Refer to the instructions supplied with the rack mount kits to install your PXIe-1084 chassis in an instrument rack.

**Note**  You may want to remove the feet or carrying handle from the PXIe-1084 chassis when rack mounting.

**Figure 2-3.** PXIe-1084 Rack Mount Kit Components

| 1 | Front Rack Mount |
| 2 | Rear Rack Mount |
Connecting the Safety Ground

⚠️ **Caution** The PXIe-1084 chassis are designed with a three-position IEC 60320 C14 inlet for the U.S. that connects the ground line to the chassis ground. For proper grounding, a suitable cordset must be used to connect this inlet to an appropriate earth safety ground.

If your power outlet does not have an appropriate ground connection, you must connect the premise safety ground to the chassis grounding screw located on the rear panel. Refer to Figure 1-2, *Rear View of the PXIe-1084 Chassis*, to locate the chassis grounding screw.

To connect the safety ground, complete the following steps:

1. Connect a 16 AWG (1.3 mm) wire to the chassis grounding screw (#8-32 SEMS) using a grounding lug. The wire must have green insulation with a yellow stripe or must be noninsulated (bare).

2. Attach the opposite end of the wire to permanent earth ground using toothed washers or a toothed lug.

Connecting to a Power Source

⚠️ **Cautions** Do not install modules prior to performing the following power-on test.

To completely remove power, you must disconnect all power cords.

Attach input power through the rear AC inlet using the appropriate AC power cable supplied. Refer to Figure 1-2, *Rear View of the PXIe-1084 Chassis*, to locate the AC inlet.

The Power Inhibit switch allows you to power on the chassis or place it in standby mode. With an empty chassis in Default Mode, press down the Power Inhibit button and hold it down for four seconds. Observe that all fans become operational and the front panel LED is a steady green. Pressing and holding the Power Inhibit button again for four seconds will return the chassis to standby.
Installing a PXI Express System Controller

This section contains general installation instructions for installing a PXI Express system controller in a PXIe-1084 chassis. Refer to your PXI Express system controller user manual for specific instructions and warnings. To install a system controller, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the system controller. The AC power cord grounds the chassis and protects it from electrical damage while you install the system controller.

2. Install the system controller into the system controller slot (slot 1, indicated by the red card guides) by first placing the system controller PCB into the front of the card guides (top and bottom). Slide the system controller to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-4.

Figure 2-4. Installing a PXI Express System Controller

| 1 | System Controller Front Panel Mounting Screws (4x) |
| 2 | PXI Express System Controller |
| 3 | Injector/Ejector Handle |
| 4 | PXIe Chassis |
3. When you begin to feel resistance, pull up on the injector/ejector handle to seat the system controller fully into the chassis frame. Secure the system controller front panel to the chassis using the system controller front-panel mounting screws.

4. Connect the keyboard, mouse, and monitor to the appropriate connectors. Connect devices to ports as required by your system configuration.

5. Power on the chassis. Verify that the system controller boots. If the system controller does not boot, refer to your system controller user manual.

You can place CompactPCI, CompactPCI Express, PXI, or PXI Express modules in other slots depending on the slot type.
Chapter 2 Installation and Configuration

Installing Peripheral Modules

This section contains general installation instructions for installing a peripheral module in a PXIe-1084 chassis. Refer to your peripheral module user manual for specific instructions and warnings. To install a module, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the module. The AC power cord grounds the chassis and protects it from electrical damage while you install the module.
2. Ensure that the chassis is powered off.
3. Install a module into a chassis slot by first placing the module card PCB into the front of the card guides (top and bottom), as shown in Figure 2-5. Slide the module to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-5.
4. When you begin to feel resistance, push up on the injector/ejector handle to fully seat the module into the chassis frame. Secure the module front panel to the chassis using the module front-panel mounting screws.

Figure 2-5. Installing PXI, PXI Express, or CompactPCI Peripheral Modules
LED Indicators

The following tables describe the front and rear panel LED states. Refer to Figure 1-1, *Front View of the PXIe-1084 Chassis* and Figure 1-2, *Rear View of the PXIe-1084 Chassis* for LED locations. Figure 2-6 shows the Status LED.

**Figure 2-6. Status LED**

![Status LED](image)

1 Status LED

| Table 2-1. Front Panel Status LED States |
|-------------------------------|--------------------------------------|
| **LED** | **State** | **Description** |
| Status LED | Off | Chassis is powered off. |
|  | Steady green | Chassis is powered on, and operating normally. |
|  | Steady red | Indicates temperature is out of range, or an internal chassis fault has occurred. |

| Table 2-2. Rear Panel Power Supply LED States |
|-------------------------------|--------------------------------------|
| **LED** | **State** | **Description** |
| Power Supply LED | Off | Power supply is unplugged or in standby. |
|  | Steady green | Main power is active and power supply is operating normally. |
|  | Blinking red | Power supply is operating outside of specification. |
|  | Steady red | Power supply has failed. |
DIP Switches

The backplane has a DIP switch that may be used to control chassis behavior. Refer to Figure 1-1, *Front View of the PXIe-1084 Chassis* for the backplane DIP switch location.

DIP switch #1 (first from the bottom) controls the chassis fan mode. When this switch is in the off (right) position, **Auto** mode is selected. When this switch is in the on (left) position, **High** mode is selected. The chassis fan mode may also be set through software. Refer to the *Fan Mode* section for more information.

DIP switch #2 (second from the bottom) controls the chassis Inhibit Mode. When this switch is in the off (right) position, **Default** mode is selected. When this switch is in the on (left) position, **Manual** mode is selected.

*Note* The chassis Inhibit Mode may also be set through software. Refer to the *Inhibit Mode* section for more information.

**Figure 2-7. Backplane DIP Switches**

<table>
<thead>
<tr>
<th>Location</th>
<th>Switch</th>
<th>State</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>FAN</td>
<td>Off (Right)</td>
<td>Set chassis fan mode to Auto. Refer to the <em>Fan Mode</em> section for information.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On (Left)</td>
<td>Set chassis fan mode to High.</td>
</tr>
<tr>
<td>2</td>
<td>PWR</td>
<td>Off (Right)</td>
<td>Set chassis inhibit mode to <strong>Default</strong>. Refer to the <em>Inhibit Mode</em> section for information.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On (Left)</td>
<td>Set chassis inhibit mode to <strong>Manual</strong>.</td>
</tr>
</tbody>
</table>
Inhibit Mode

The PXIe-1084 chassis supports operation in two inhibit modes. **Default** mode is used when normal power inhibit button functionality is desired. In **Default** mode, when a system controller is installed in Slot 1 of the chassis, the user can press the power inhibit button to power on the chassis.

**Note** In **Default** mode, you can also power on the chassis without a system controller installed in slot 1. To power on the chassis from standby, press and hold the power inhibit button for 4 seconds. To power off the chassis, again press and hold the power inhibit button for 4 seconds.

**Manual** mode is used when you would like to manually control the inhibit state of the chassis. In **Manual** mode, driving the Remote Inhibit signal high or floating it will cause the chassis to be powered on. Driving the Remote Inhibit signal low or shorting it to ground will cause main power to be inhibited.

**Note** The Timing and Synchronization upgrade is required for access to the Remote Inhibit signal. Without this upgrade, a chassis in **Manual** mode will always be powered on when AC power is connected.

Inhibit Mode Selection

The chassis Inhibit Mode can be selected using Measurement & Automation Explorer (MAX). Refer to the **Inhibit Mode Configuration in MAX** section for more information.

Alternatively, the chassis Inhibit Mode on the PXIe-1084 chassis can be selected using a DIP switch on the backplane. Refer to the **DIP Switches** section for more information about the DIP switch. Refer to Figure 1-1, *Front View of the PXIe-1084 Chassis* for the location of this switch.

**Note** The DIP switch must be in the Default position for software configuration in MAX to work. If the DIP switch is in the Manual position, the Inhibit Mode will be Manual regardless of the software setting.
Fan Mode

The PXIe-1084 chassis operates in two main fan modes.

In **Auto** mode, the speed of the chassis fans is determined by chassis intake air temperature. Select **Auto** mode for improved acoustic performance.

In **High** mode, the speed of the chassis fans is fixed at high speed regardless of chassis intake air temperature. Select **High** mode for maximum cooling performance.

Cooling Profiles

Both fan modes are available within the 38 W and 58 W cooling profiles.

- **38 W cooling profile**—Supports NI modules up to 38 W max power dissipation
- **58 W cooling profile**—Supports NI modules up to 58 W max power dissipation

Fan Mode Selection

The chassis fan mode can be selected using Measurement & Automation Explorer (MAX). Refer to the **Fan Configuration in MAX** section for more information.

Alternatively, the fan mode on the PXIe-1084 chassis is selected using a DIP switch on the backplane. Refer to the **DIP Switches** section for more information about the DIP switch. Refer to Figure 1-1, *Front View of the PXIe-1084 Chassis* for the location of this switch.

⚠️ **Note** The DIP switch must be in the Auto position for software configuration in MAX to work. If the DIP switch is in the High position, the chassis Fan Mode will be High regardless of the software setting.

PXI_CLK10 Rear Panel Connectors

With the Timing and Synchronization upgrade, there are two SMA connectors on the rear of the chassis for PXI_CLK10. The connectors are labeled 10 MHz REF IN and OUT. You can use them for supplying the backplane with PXI_CLK10 or routing the backplane’s PXI_CLK10 to another chassis. Refer to the **System Reference Clock** section of Chapter 1, *Getting Started*, for details about these signals.
High Density Triggers

With the Timing and Synchronization upgrade, the PXIe-1084 supports routing PXI triggers between chassis using a pair of high-density trigger connectors on the rear of the chassis.

The following table shows the pinout of the high-density trigger connector.

**Table 2-4. High-Density Trigger Connector Pinout**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal, Top Port</th>
<th>Signal Bottom Port</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Trig(0)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Logic Ground</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Trig(4)</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Trig(1)</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Logic Ground</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Trig(5)</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Trig(2)</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Logic Ground</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Trig(6)</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>10 MHz Ref In +</td>
<td>10 MHz Ref Out +</td>
</tr>
<tr>
<td>11</td>
<td>Logic Ground</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>10 MHz Ref In -</td>
<td>10 MHz Ref Out -</td>
</tr>
<tr>
<td>13</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Trig(3)</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>SCL</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>SDA</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Logic Ground</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Presence Detect</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>Trig(7)</td>
<td></td>
</tr>
</tbody>
</table>
Routing triggers between chassis requires using a National Instruments API such as NI-DAQmx. You can target the individual pins of each trigger port as sources or destinations for PXI triggers to or from a PXI module. If the chassis are connected to the same host via MXI, then targeting these pins is not necessary; you can specify a source device in one chassis and a destination device in another chassis and the software will make the necessary trigger routes automatically.

**Caution**  The high-density trigger ports are not HDMI interfaces. Do not connect the high-density trigger ports on the PXIe-1084 to the HDMI interface of another device. NI is not liable for any damage resulting from such signal connections.

**Caution**  Off-the-shelf HDMI cables may be used to connect adjacent chassis. However, since off-the-shelf cables may be of varying quality, for best performance use NI recommended cables available at ni.com.

**Caution**  For proper operation, the Port 1/Ref Out port of one chassis must be cabled to Port 0/Ref In of the adjacent chassis. Do not connect Port 0/Ref In to Port 0/Ref In of another chassis. Do not connect Port 1/Ref Out to Port 1/Ref Out of another chassis. While no damage will occur in either of these configurations, the trigger routing capabilities will not be functional.

**Note**  Triggers may be routed either direction out of either trigger port.
Remote Inhibit and Chassis Monitoring

With the Timing and Synchronization upgrade, the PXIe-1084 chassis supports remote voltage monitoring and inhibiting through a female 15-pin connector on the rear panel. Table 2-5 shows the pinout of the 15-pin connector.

**Table 2-5. Remote Inhibit and Chassis Monitoring Connector Pinout**

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Logic Ground</td>
</tr>
<tr>
<td>2</td>
<td>+5 V</td>
</tr>
<tr>
<td>3</td>
<td>Fault (Active High)</td>
</tr>
<tr>
<td>4</td>
<td>+3.3 V</td>
</tr>
<tr>
<td>5</td>
<td>Inhibit (Active Low)</td>
</tr>
<tr>
<td>6</td>
<td>+12V</td>
</tr>
<tr>
<td>7</td>
<td>Key</td>
</tr>
<tr>
<td>8</td>
<td>-12 V</td>
</tr>
<tr>
<td>9</td>
<td>Logic Ground</td>
</tr>
<tr>
<td>10</td>
<td>PFI3</td>
</tr>
<tr>
<td>11</td>
<td>PFI2</td>
</tr>
<tr>
<td>12</td>
<td>Logic Ground</td>
</tr>
<tr>
<td>13</td>
<td>PFI1</td>
</tr>
<tr>
<td>14</td>
<td>PFI0</td>
</tr>
<tr>
<td>15</td>
<td>Logic Ground</td>
</tr>
</tbody>
</table>

PFI / INHIBIT / VOLTAGE MON
Chapter 2  Installation and Configuration

You can use a digital voltmeter to ensure all voltage levels in the chassis are within the allowable limits. Referring to Table 2-5, connect one lead of the voltmeter to a supply pin on the 15-pin remote voltage monitoring connector on the rear panel. Connect the reference lead of the voltmeter to one of the ground pins. Compare each voltage reading to the values listed in Table 2-6.

**Caution**  When connecting digital voltmeter probes to the rear 15-pin connector, care must be taken not to short the probe leads together.

**Note**  Use the rear-panel 15-pin connector to check voltages only. Do *not* use the connector to supply power to external devices.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Supply</th>
<th>Acceptable Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>+5 V</td>
<td>4.75 V to 5.25 V</td>
</tr>
<tr>
<td>4</td>
<td>+3.3 V</td>
<td>3.135 V to 3.465 V</td>
</tr>
<tr>
<td>6</td>
<td>+12 V</td>
<td>11.4 V to 12.6 V</td>
</tr>
<tr>
<td>8</td>
<td>-12 V</td>
<td>-12.6 V to -11.4 V</td>
</tr>
<tr>
<td>1, 9, 12, 15</td>
<td>Logic Ground</td>
<td>0 V</td>
</tr>
</tbody>
</table>

If the voltages fall within the specified ranges, the chassis complies with the CompactPCI voltage-limit specifications.

The Inhibit signal may be used to manually control the inhibit state of the chassis when the inhibit mode is set to Manual. See the *Inhibit Mode* section for more information. Refer to the *PXIe-1084 Specifications* for the input requirements of the Inhibit signal.

The Fault signal is used to indicate when a fault condition is detected on the chassis. The definition of this signal is shown in Table 2-7. Refer to the *PXIe-1084 Specifications* for the voltage specifications of the Fault signal.

<table>
<thead>
<tr>
<th>State</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>Chassis is operating normally</td>
</tr>
<tr>
<td>High</td>
<td>An abnormal operating condition has been detected.</td>
</tr>
</tbody>
</table>
Examples of abnormal operating conditions include but are not limited to: intake or exhaust temperature outside of chassis operating range, a chassis fan has failed, or a chassis voltage is outside its specified operating range.

The four Programmable Function Interface (PFI) lines may be used to route triggers to/from PXI modules in the chassis. Routing triggers to the PFI lines requires using an NI API such as NI-DAQmx. You can target the individual PFI lines as sources or destinations for PXI triggers to or from a PXI module. Refer to the PXIe-1084 Specifications for the input and output specifications of the PFI lines.

**USB Port**

With the Timing and Synchronization upgrade, the PXIe-1084 has a single USB 3.0 Type A port on the rear of the chassis. Table 2-8 lists and describes the USB 3.0 connector signals.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal Name</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VBUS</td>
<td>Cable Power (+5 V)</td>
</tr>
<tr>
<td>2</td>
<td>Data-</td>
<td>USB Data-</td>
</tr>
<tr>
<td>3</td>
<td>Data+</td>
<td>USB Data+</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>5</td>
<td>StdA_SSRX-</td>
<td>USB Data Receive-</td>
</tr>
<tr>
<td>6</td>
<td>StdA_SSRX+</td>
<td>USB Data Receive+</td>
</tr>
<tr>
<td>7</td>
<td>GND DRAIN</td>
<td>Ground</td>
</tr>
<tr>
<td>8</td>
<td>StdA_SSTX-</td>
<td>USB Data Transmit-</td>
</tr>
<tr>
<td>9</td>
<td>StdA_SSTX+</td>
<td>USB Data Transmit+</td>
</tr>
</tbody>
</table>

The PXIe-1084 chassis uses a Texas Instruments TUSB7340 USB 3.0 Host Controller as the interface for the rear USB port.

**Note** Drivers for this device are required for Windows 7 and are available for download at www.ti.com/lit/zip/sllc423.
Chapter 2  Installation and Configuration

PXI Express System Configuration with MAX

The PXI Platform Services software included with your chassis automatically identifies your PXI Express system components to generate a `pxiesys.ini` file. You can configure your entire PXI system and identify PXI-1 chassis through Measurement & Automation Explorer (MAX), included with your system controller. PXI Platform Services creates the `pxiesys.ini` and `pxisys.ini` file, which define your PXI system parameters.

Note The configuration steps for single or multiple-chassis systems are the same.

MAX provides the following chassis information:

- Asset information, such as serial number or part number
- Chassis number
- Voltages, temperatures, and fan speeds
- Fan and cooling settings
- Number and type of power supplies
- Slot details
- Chassis self-test
- Firmware Update
Figure 2-9. Chassis Settings in MAX
Chapter 2  Installation and Configuration

Trigger Configuration in MAX

PXI Platform Services provides an interface to route and reserve triggers so dynamic routing, through drivers such as DAQmx, avoids double-driving and potentially damaging trigger lines. For more information about routing and reserving PXI triggers, refer to KnowledgeBase 3TJDOND8 at ni.com/support.

Each chassis has one or more trigger buses, each with eight lines numbered 0 through 7 that can be reserved and routed statically or dynamically. Static reservation pre-allocates a trigger line to prevent its configuration by a user program. Dynamic reservation/routing/deallocation is on the fly within a user program based upon National Instruments APIs such as NI-DAQmx.

NI recommends dynamic reservations and routing are used whenever possible. If static reservations are required, static reservation of trigger lines can be implemented by the user in MAX through the Triggers tab. Reserved trigger lines will not be used by PXI modules dynamically configured by programs such as NI-DAQmx. This prevents the instruments from double-driving the trigger lines, possibly damaging devices in the chassis. In the default configuration, trigger lines on each bus are independent. For example, if trigger line 3 is asserted on trigger bus 0, by default it will not be automatically asserted on any other trigger bus.

Complete the following steps to reserve these trigger lines in MAX.
1. In the Configuration tree, click on the PXI chassis branch you want to configure.
2. Then, in the right-hand pane, toward the bottom, click on the Triggers tab.
3. Select which trigger lines you would like to statically reserve.
4. Click the Save button.

Figure 2-10. Trigger Configuration in MAX
PXI Trigger Bus Routing

Some National Instruments chassis, including the PXIe-1084, have the capability to route triggers from one bus to others within the same chassis using the Trigger Routing tab in MAX, as shown in Figure 2-10.

**Note** Selecting any non-disabled routing automatically reserves the line in all trigger buses being routed to. If you are using NI-DAQmx, it will reserve and route trigger lines for you, so you won’t have to route trigger lines manually.

Complete the following steps to configure trigger routings in MAX:

1. In the Configuration tree, select the chassis in which you want to route trigger lines.
2. In the right-hand pane, select the Trigger Routing tab near the bottom.
3. For each trigger line, select *Away from Bus 1*, *Away from Bus 2*, or *Away from Bus 3* to route triggers on that line in the described direction, or select Dynamic for the default behavior with no manual routing.
4. Click the Save button.

Inhibit Mode Configuration in MAX

You can configure inhibit mode behavior using software settings in MAX. The PXIe-1084 supports both Default and Manual inhibit modes. Refer to the Inhibit Mode section for more information about these modes.

Complete the following steps to change the chassis inhibit mode in MAX:

1. In the Configuration tree, select the PXI chassis you want to configure.
2. In the right-hand pane, click on the Settings tab.
3. In the Power Supplies group, select the desired Inhibit Mode using the drop-down menus.
4. Click the Save button.
Chapter 2  Installation and Configuration

Fan Configuration in MAX

You can configure fan behavior using software settings in MAX.

The PXIe-1084 supports both Auto and High fan modes for both the 38 W and 58 W cooling profiles. Refer to the Fan Mode section for more information on these modes.

The user may also select a Manual fan mode. In this mode, the user may manually set the fan speeds to achieve the desired performance.

Note  Chassis software will automatically select the cooling profile and fan mode required to support the modules in the chassis. You can not set fan speeds or power settings lower than the minimum level necessary to maintain required cooling levels.

Complete the following steps to change the fan settings in MAX.
1. In the Configuration tree, click on the PXI chassis you want to configure.
2. In the right-hand pane, click on the Settings tab.
3. In the Fans group, select the desired Mode and Cooling Profile using the drop-down menus.
4. Click the Save button. Shortly after clicking the Save button, you should see the fan speeds change.

Using System Configuration and Initialization Files

The PXI Express specification allows many combinations of PXI Express chassis and system modules. To assist system integrators, the manufacturers of PXI Express chassis and system modules must document the capabilities of their products. The minimum documentation requirements are contained in .ini files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these .ini files.

The capability documentation for the PXIe-1084 chassis is contained in the chassis.ini file on the software media that comes with the chassis. The information in this file is combined with information about the system controller to create a single system initialization file called pxisys.ini (PXI System Initialization). The system controller manufacturer either provides a pxisys.ini file for the particular chassis model that contains the system controller or provides a utility that can read an arbitrary chassis.ini file and generate the corresponding pxisys.ini file. System controllers from NI provide the pxisys.ini file for the PXIe-1084 chassis, so you should not need to use the chassis.ini file. Refer to the documentation provided with the system controller or to ni.com/support for more information on pxisys.ini and chassis.ini files.

Device drivers and other utility software read the pxisys.ini file to obtain system information. The device drivers should have no need to directly read the chassis.ini file. For detailed information regarding initialization files, refer to the PXI Express specification at www.pxisa.org.
Maintenance

This chapter describes basic maintenance procedures you can perform on the PXIe-1084 chassis.

⚠️ **Caution**  Disconnect all power cables prior to servicing a PXIe-1084 chassis.

Service Interval

Clean dust from the chassis exterior (and interior) as needed, based on the operating environment. Periodic cleaning increases reliability.

Preparation

The information in this section is designed for use by qualified service personnel. Read the *Read Me First: Safety and Electromagnetic Compatibility* document included with your kit before attempting any procedures in this chapter.

⚠️ **Caution**  Many components within the chassis are susceptible to static discharge damage. Service the chassis only in a static-free environment. Observe standard handling precautions for static-sensitive devices while servicing the chassis. *Always* wear a grounded wrist strap or equivalent while servicing the chassis.

Cleaning

Cleaning procedures consist of exterior and interior cleaning of the chassis. Refer to your module user documentation for information on cleaning the individual CompactPCI or PXI Express modules.

⚠️ **Caution**  *Always* disconnect the AC power cables before cleaning or servicing the chassis.
Chapter 3  Maintenance

Interior Cleaning
Use a dry, low-velocity stream of air to clean the interior of the chassis. Use a soft-bristle brush for cleaning around components.

Exterior Cleaning
Clean the exterior surfaces of the chassis with a dry lint-free cloth or a soft-bristle brush. If any dirt remains, wipe with a cloth moistened in a mild soap solution. Remove any soap residue by wiping with a cloth moistened with clear water. Do not use abrasive compounds on any part of the chassis.

⚠️ Cautions  Avoid getting moisture inside the chassis during exterior cleaning, especially through the top vents. Use just enough moisture to dampen the cloth.

Do not wash the front- or rear-panel connectors or switches. Cover these components while cleaning the chassis.

Do not use harsh chemical cleaning agents; they may damage the chassis. Avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Connecting Safety Ground
Refer to the Connecting the Safety Ground section of Chapter 2, Installation and Configuration.

Connecting to Power Source
Refer to the Connecting to a Power Source section of Chapter 2, Installation and Configuration.
Installing Replacement Fan Assemblies

This section describes how to remove and install fan assemblies in the PXIe-1084 chassis.

![Caution](image-url) Disconnect all power cables and wait at least 30 seconds prior to replacing fan assemblies.

Replacing the PXI Module Fan Assembly

Before attempting to replace the rear module fan assembly, verify that there is adequate clearance behind the chassis. Disconnect the power cable from the power supply on the back of the chassis. Wait at least 30 seconds for the supply’s internal power to dissipate.

Follow these steps to remove the fan assembly:

1. Using a Phillips screwdriver, remove the eight #6-32 mounting screws and #8-32 ground screw that attach the fan panel to the chassis.
2. Remove rear chassis feet.
3. With internal fan harness still connected, carefully pull and rotate fan assembly from rear cavity of chassis. Use caution when removing the fan assembly to avoid damaging the fan wire harness.
4. Disconnect fan harness from the internal chassis receptacle as shown in Figure 3-2.

Follow these steps to install a new fan assembly:

1. Angle the fan assembly to install the fan harness plug into the internal chassis receptacle. Use care to avoid damaging the fan harness or receptacle.
2. Connect the internal fan harness and install fan assembly into rear cavity of chassis as shown in Figure 3-2, Internal Fan Harness. Use caution when installing the fan panel assembly to avoid pinching or damaging the wire harness.
3. Replace chassis feet.
4. Using a Phillips screwdriver, tighten the eight #6-32 mounting screws and #8-32 ground screw into the rear of the chassis. To meet Shock and Vibration specifications listed in the PXIe-1084 Specifications, tighten screws to 1.3 N·m (11.5 in·lb) of torque.
Chapter 3  Maintenance

Figure 3-1. Replacing Rear Fan Module

![Diagram of Rear Fan Module Replacement]

1. Fan Harness Plug
2. PXIe-1084 Chassis
3. PXI Module Fan Assembly
4. Rear Chassis Feet (2x)
5. Mounting Screws (8x)

Figure 3-2. Internal Fan Harness

![Diagram of Internal Fan Harness]

1. Fan Receptacle
2. Fan Harness Plug
Replacing the Side Fan Assembly

Before attempting to replace the side fan assembly, verify that there is adequate clearance to the side of the chassis. Disconnect the power cable from the power supply on the back of the chassis. Wait at least 30 seconds for the power supply’s internal power to dissipate.

Complete the following steps to remove the side fan assembly:

1. Using a Phillips screwdriver, remove the four mounting screws that attach the side fan cover.
2. Remove side fan cover from chassis.
3. Using a Phillips screwdriver, remove the two mounting screws that hold the side fan assembly onto the chassis.
4. Locate side fan assembly harness in internal chassis cavity and disconnect the fan from the chassis receptacle. Use caution when removing the fan assembly to avoid damaging the internal wire harness.
5. Pull side fan assembly straight from chassis and remove.

Complete the following steps to install a new side fan assembly.

1. Plug side fan assembly plug into internal chassis fan receptacle.
2. Set side fan assembly into chassis side fan cavity. Use caution when placing wire harness into chassis to avoid damaging the internal or fan wire harness.
3. Using a Phillips screwdriver, hand tighten two side assembly mounting screws. Use the side fan cutout to pull clear extra cable from chassis side panels to prevent pinching.
4. Place all extra cable into chassis side fan cavity.
5. Using a Phillips screwdriver, tighten the four side fan cover mounting screws to the chassis. To meet Shock and Vibration specifications listed in the PXIe-1084 Specifications, tighten screws to 0.8 N · m (6.7 in · lb) of torque.
Figure 3-3. Replacing Side Fan Assembly

<table>
<thead>
<tr>
<th></th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Chassis Side Fan Cavity</td>
</tr>
<tr>
<td>2</td>
<td>Side Fan Assembly</td>
</tr>
<tr>
<td>3</td>
<td>Side Fan Cover</td>
</tr>
<tr>
<td>4</td>
<td>Side Fan Cover Mounting Screws (4x)</td>
</tr>
</tbody>
</table>
Pinouts

This appendix describes the connector pinouts for the PXIe-1084 chassis backplane.

Table A-1 shows the XP1 Connector Pinout for the System Controller slot.
Table A-2 shows the XP2 Connector Pinout for the System Controller slot.
Table A-3 shows the XP3 Connector Pinout for the System Controller slot.
Table A-4 shows the XP4 Connector Pinout for the System Controller slot.
Table A-5 shows the P1 Connector Pinout for the Hybrid peripheral slots.
Table A-6 shows the XP3 Connector Pinout for the Hybrid peripheral slots.
Table A-7 shows the XP4 Connector Pinout for the Hybrid peripheral slots.

For more detailed information, refer to the PXI-5 PXI Express Hardware Specification, Revision 2.0. Contact the PXI Systems Alliance for a copy of the specification.
## System Controller Slot Pinouts

### Table A-1. XP1 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pins</th>
<th>Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>GND</td>
</tr>
<tr>
<td>B</td>
<td>12V</td>
</tr>
<tr>
<td>C</td>
<td>12V</td>
</tr>
<tr>
<td>D</td>
<td>GND</td>
</tr>
<tr>
<td>E</td>
<td>5V</td>
</tr>
<tr>
<td>F</td>
<td>3.3V</td>
</tr>
<tr>
<td>G</td>
<td>GND</td>
</tr>
</tbody>
</table>

### Table A-2. XP2 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>cd</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2PETp1</td>
<td>2PETn1</td>
<td>GND</td>
<td>2PERp1</td>
<td>2PERn1</td>
<td>GND</td>
<td>2PETp2</td>
<td>2PETn2</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>2PETp3</td>
<td>2PETn3</td>
<td>GND</td>
<td>2PERp3</td>
<td>2PERn3</td>
<td>GND</td>
<td>2PETp2</td>
<td>2PETn2</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>2PETp4</td>
<td>2PETn4</td>
<td>GND</td>
<td>2PERp4</td>
<td>2PERn4</td>
<td>GND</td>
<td>2PETp5</td>
<td>2PETn5</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>2PETp6</td>
<td>2PETn6</td>
<td>GND</td>
<td>2PERp6</td>
<td>2PERn6</td>
<td>GND</td>
<td>2PETp5</td>
<td>2PETn5</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>2PETp7</td>
<td>2PETn7</td>
<td>GND</td>
<td>2PERp7</td>
<td>2PERn7</td>
<td>GND</td>
<td>2PETp8</td>
<td>2PETn8</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>2PETp9</td>
<td>2PETn9</td>
<td>GND</td>
<td>2PERp9</td>
<td>2PERn9</td>
<td>GND</td>
<td>2PETp8</td>
<td>2PETn8</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>2PETp10</td>
<td>2PETn10</td>
<td>GND</td>
<td>2PERp10</td>
<td>2PERn10</td>
<td>GND</td>
<td>2PETp11</td>
<td>2PETn11</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>2PETp12</td>
<td>2PETn12</td>
<td>GND</td>
<td>2PERp12</td>
<td>2PERn12</td>
<td>GND</td>
<td>2PETp11</td>
<td>2PETn11</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>2PETp13</td>
<td>2PETn13</td>
<td>GND</td>
<td>2PERp13</td>
<td>2PERn13</td>
<td>GND</td>
<td>2PETp14</td>
<td>2PETn14</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>2PETp15</td>
<td>2PETn15</td>
<td>GND</td>
<td>2PERp15</td>
<td>2PERn15</td>
<td>GND</td>
<td>2PETp14</td>
<td>2PETn14</td>
<td>GND</td>
</tr>
</tbody>
</table>
Table A-3. XP3 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>cd</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>PWR_OK</td>
<td>PS_ON#</td>
<td>GND</td>
<td>LINKCAP</td>
<td>PWRBTN#</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>SMBDAT</td>
<td>SMBCLK</td>
<td>GND</td>
<td>RSVD</td>
<td>RSVD</td>
<td>GND</td>
<td>RSVD</td>
<td>RSVD</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>RSV</td>
<td>PERST#</td>
<td>GND</td>
<td>2RefClk+</td>
<td>2RefClk-</td>
<td>GND</td>
<td>1RefClk+</td>
<td>1RefClk-</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>1PETp0</td>
<td>1PETn0</td>
<td>GND</td>
<td>1PERp0</td>
<td>1PERn0</td>
<td>GND</td>
<td>1PETp1</td>
<td>1PETn1</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>1PETp2</td>
<td>1PETn2</td>
<td>GND</td>
<td>1PERp2</td>
<td>1PERn2</td>
<td>GND</td>
<td>1PERp1</td>
<td>1PERn1</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>1PETp3</td>
<td>1PETn3</td>
<td>GND</td>
<td>1PERp3</td>
<td>1PERn3</td>
<td>GND</td>
<td>1PETp4</td>
<td>1PETn4</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>1PETp5</td>
<td>1PETn5</td>
<td>GND</td>
<td>1PERp5</td>
<td>1PERn5</td>
<td>GND</td>
<td>1PERp4</td>
<td>1PERn4</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>1PETp6</td>
<td>1PETn6</td>
<td>GND</td>
<td>1PERp6</td>
<td>1PERn6</td>
<td>GND</td>
<td>1PETp7</td>
<td>1PETn7</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>2PETp0</td>
<td>2PETn0</td>
<td>GND</td>
<td>2PERp0</td>
<td>2PERn0</td>
<td>GND</td>
<td>1PERp7</td>
<td>1PERn7</td>
<td>GND</td>
</tr>
</tbody>
</table>

Table A-4. XP4 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>GA4</td>
<td>GA3</td>
<td>GA2</td>
<td>GA1</td>
<td>GA0</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>5Vaux</td>
<td>GND</td>
<td>SYSEN#</td>
<td>WAKE#</td>
<td>ALERT#</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>PXI_TRIG3</td>
<td>PXI_TRIG4</td>
<td>PXI_TRIG5</td>
<td>GND</td>
<td>PXI_TRIG6</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>PXI_TRIG2</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_STAR</td>
<td>PXI_TRIG10</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>PXI_TRIG1</td>
<td>PXI_TRIG0</td>
<td>RSV</td>
<td>GND</td>
<td>PXI_TRIG7</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>PXI_LBR6</td>
<td>GND</td>
</tr>
</tbody>
</table>
# Hybrid Slot Pinouts

## Table A-5. P1 Connector Pinout for the Hybrid Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>GND</td>
<td>5V</td>
<td>REQ64#</td>
<td>ENUM#</td>
<td>3.3V</td>
<td>5V</td>
<td>GND</td>
</tr>
<tr>
<td>24</td>
<td>GND</td>
<td>AD[1]</td>
<td>5V</td>
<td>V(I/O)</td>
<td>AD[0]</td>
<td>ACK64#</td>
<td>GND</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>SERR#</td>
<td>GND</td>
<td>3.3V</td>
<td>PAR</td>
<td>C/BE[1]#</td>
<td>GND</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>3.3V</td>
<td>IPMB_SCL</td>
<td>IPMB SDA</td>
<td>GND</td>
<td>PERR#</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>DEVSEL#</td>
<td>GND</td>
<td>V(I/O)</td>
<td>STOP#</td>
<td>LOCK#</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>3.3V</td>
<td>FRAME#</td>
<td>IRDY#</td>
<td>BD_SEL#</td>
<td>TRDY#</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>C/BE[3]#</td>
<td>IDSEL</td>
<td>AD[23]</td>
<td>GND</td>
<td>AD[22]</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>REQ#</td>
<td>GND</td>
<td>3.3V</td>
<td>CLK</td>
<td>AD[31]</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>BRSVP1A5</td>
<td>BRSVP1B5</td>
<td>RST#</td>
<td>GND</td>
<td>GNT#</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>IPMB_PWR</td>
<td>HEALTHY#</td>
<td>V(I/O)</td>
<td>INTP</td>
<td>INTS</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>INTA#</td>
<td>INTB#</td>
<td>INTC#</td>
<td>5V</td>
<td>INTD#</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>TCK</td>
<td>5V</td>
<td>TMS</td>
<td>TDO</td>
<td>TDI</td>
<td>GND</td>
</tr>
<tr>
<td>1</td>
<td>GND</td>
<td>5V</td>
<td>-12V</td>
<td>TRST#</td>
<td>+12V</td>
<td>5V</td>
<td>GND</td>
</tr>
</tbody>
</table>
### Table A-6. XP3 Connector Pinout for the Hybrid Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>cd</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PXIe_CLK100+</td>
<td>PXIe_CLK100-</td>
<td></td>
<td>PXIe_SYNC100+</td>
<td>PXIe_SYNC100-</td>
<td></td>
<td>PXIe_DSTARC+</td>
<td>PXIe_DSTARC-</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>PRSNT#</td>
<td>PWREN#</td>
<td></td>
<td>PXIe_DSTARB+</td>
<td>PXIe_DSTARB-</td>
<td></td>
<td>PXIe_DSTARA+</td>
<td>PXIe_DSTARA-</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>SMBDAT</td>
<td>SMBCLK</td>
<td></td>
<td>RSV</td>
<td>RSV</td>
<td></td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>MPWRGD*</td>
<td>PERST#</td>
<td></td>
<td>RSV</td>
<td>RSV</td>
<td></td>
<td>GND</td>
<td>1RefClk+</td>
<td>1RefClk-</td>
</tr>
<tr>
<td>5</td>
<td>1PETp0</td>
<td>1PETn0</td>
<td></td>
<td>1PERp0</td>
<td>1PERn0</td>
<td></td>
<td>GND</td>
<td>1PETp1</td>
<td>1PETn1</td>
</tr>
<tr>
<td>6</td>
<td>1PETp2</td>
<td>1PETn2</td>
<td></td>
<td>1PERp2</td>
<td>1PERn2</td>
<td></td>
<td>GND</td>
<td>1PERp1</td>
<td>1PERn1</td>
</tr>
<tr>
<td>7</td>
<td>1PETp3</td>
<td>1PETn3</td>
<td></td>
<td>1PERp3</td>
<td>1PERn3</td>
<td></td>
<td>GND</td>
<td>1PETp4</td>
<td>1PETn4</td>
</tr>
<tr>
<td>8</td>
<td>1PETp5</td>
<td>1PETn5</td>
<td></td>
<td>1PERp5</td>
<td>1PERn5</td>
<td></td>
<td>GND</td>
<td>1PETp4</td>
<td>1PERn4</td>
</tr>
<tr>
<td>9</td>
<td>1PETp6</td>
<td>1PETn6</td>
<td></td>
<td>1PERp6</td>
<td>1PERn6</td>
<td></td>
<td>GND</td>
<td>1PETp7</td>
<td>1PETn7</td>
</tr>
<tr>
<td>10</td>
<td>RSV</td>
<td>RSV</td>
<td></td>
<td>RSV</td>
<td>RSV</td>
<td></td>
<td>GND</td>
<td>1PERp7</td>
<td>1PERn7</td>
</tr>
</tbody>
</table>

### Table A-7. XP4 Connector Pinout for the Hybrid Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>GA4</td>
<td>GA3</td>
<td>GA2</td>
<td>GA1</td>
<td>GA0</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>5Vaux</td>
<td>GND</td>
<td>SYSEN#</td>
<td>WAKE#</td>
<td>ALERT#</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>12V</td>
<td>12V</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>3.3V</td>
<td>3.3V</td>
<td>3.3V</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>PXI_TRIG3</td>
<td>PXI_TRIG4</td>
<td>PXI_TRIG5</td>
<td>PXI_TRIG5</td>
<td>GND</td>
<td>PXI_TRIG6</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>PXI_TRIG2</td>
<td>GND</td>
<td>ATNLED</td>
<td>PXI_STAR</td>
<td>PXI_CLK10</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>PXI_TRIG1</td>
<td>PXI_TRIG0</td>
<td>ATNSW#</td>
<td>GND</td>
<td>PXI_TRIG7</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_LBL6</td>
<td>PXI_LBR6</td>
<td>GND</td>
</tr>
</tbody>
</table>
NI Services

National Instruments provides global services and support as part of our commitment to your success. Take advantage of product services in addition to training and certification programs that meet your needs during each phase of the application life cycle; from planning and development through deployment and ongoing maintenance.

To get started, register your product at ni.com/myproducts.

As a registered NI product user, you are entitled to the following benefits:

• Access to applicable product services.
• Easier product management with an online account.
• Receive critical part notifications, software updates, and service expirations.

Log in to your National Instruments ni.com User Profile to get personalized access to your services.

Services and Resources

• **Maintenance and Hardware Services**—NI helps you identify your systems’ accuracy and reliability requirements and provides warranty, sparing, and calibration services to help you maintain accuracy and minimize downtime over the life of your system. Visit ni.com/services for more information.
  - **Warranty and Repair**—All NI hardware features a one-year standard warranty that is extendable up to five years. NI offers repair services performed in a timely manner by highly trained factory technicians using only original parts at a National Instruments service center.
  - **Calibration**—Through regular calibration, you can quantify and improve the measurement performance of an instrument. NI provides state-of-the-art calibration services. If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

• **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.
Appendix B  NI Services

• **Training and Certification**—The NI training and certification program is the most effective way to increase application development proficiency and productivity. Visit [ni.com/training](http://ni.com/training) for more information.
  – The Skills Guide assists you in identifying the proficiency requirements of your current application and gives you options for obtaining those skills consistent with your time and budget constraints and personal learning preferences. Visit [ni.com/skills-guide](http://ni.com/skills-guide) to see these custom paths.
  – NI offers courses in several languages and formats including instructor-led classes at facilities worldwide, courses on-site at your facility, and online courses to serve your individual needs.

• **Technical Support**—Support at [ni.com/support](http://ni.com/support) includes the following resources:
  – **Self-Help Technical Resources**—Visit [ni.com/support](http://ni.com/support) for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at [ni.com/forums](http://ni.com/forums). NI Applications Engineers make sure every question submitted online receives an answer.
  – **Software Support Service Membership**—The Standard Service Program (SSP) is a renewable one-year subscription included with almost every NI software product, including NI Developer Suite. This program entitles members to direct access to NI Applications Engineers through phone and email for one-to-one technical support, as well as exclusive access to online training modules at [ni.com/self-paced-training](http://ni.com/self-paced-training). NI also offers flexible extended contract options that guarantee your SSP benefits are available without interruption for as long as you need them. Visit [ni.com/ssp](http://ni.com/ssp) for more information.

• **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer’s declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting [ni.com/certification](http://ni.com/certification).

For information about other technical support options in your area, visit [ni.com/services](http://ni.com/services), or contact your local office at [ni.com/contact](http://ni.com/contact).

You also can visit the Worldwide Offices section of [ni.com/niglobal](http://ni.com/niglobal) to access the branch office websites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.
Glossary

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Prefix</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>pico</td>
<td>10^{-12}</td>
</tr>
<tr>
<td>n</td>
<td>nano</td>
<td>10^{-9}</td>
</tr>
<tr>
<td>µ</td>
<td>micro</td>
<td>10^{-6}</td>
</tr>
<tr>
<td>m</td>
<td>milli</td>
<td>10^{-3}</td>
</tr>
<tr>
<td>k</td>
<td>kilo</td>
<td>10^{3}</td>
</tr>
<tr>
<td>M</td>
<td>mega</td>
<td>10^{6}</td>
</tr>
<tr>
<td>G</td>
<td>giga</td>
<td>10^{9}</td>
</tr>
<tr>
<td>T</td>
<td>tera</td>
<td>10^{12}</td>
</tr>
</tbody>
</table>

Symbols

° Degrees.
≥ Equal or greater than.
≤ Equal or less than.
% Percent.

A

A Amperes.
AC Alternating current.
ANSI American National Standards Institute.
Auto Automatic fan speed control.
AWG American Wire Gauge.
Glossary

B

backplane An assembly, typically a printed circuit board, with connectors and signal paths that bus the connector pins.

C

Celsius.

cfm Cubic feet per minute.


cm Centimeters.

CompactPCI An adaptation of the Peripheral Component Interconnect (PCI) Specification 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. It uses industry standard mechanical components and high-performance connector technologies to provide an optimized system intended for rugged applications. It is electrically compatible with the PCI Specification, which enables low-cost PCI components to be utilized in a mechanical form factor suited for rugged environments.

CSA Canadian Standards Association.

D
daisy-chain A method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus.

DC Direct current.

DoC Declaration of Conformity.

E
efficiency Ratio of output power to input power, expressed as a percentage.

EIA Electronic Industries Association.
<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMC</td>
<td>Electromagnetic Compatibility.</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic Interference.</td>
</tr>
<tr>
<td>F</td>
<td>Federal Communications Commission.</td>
</tr>
<tr>
<td>fill panel</td>
<td>A blank module front panel used to fill empty slots in the chassis.</td>
</tr>
<tr>
<td>g</td>
<td>(1) grams; (2) a measure of acceleration equal to 9.8 m/s².</td>
</tr>
<tr>
<td>GPIB</td>
<td>General Purpose Interface Bus (IEEE 488).</td>
</tr>
<tr>
<td>gRMS</td>
<td>A measure of random vibration. The root mean square of acceleration levels in a random vibration test profile.</td>
</tr>
<tr>
<td>hr</td>
<td>Hours.</td>
</tr>
<tr>
<td>Hz</td>
<td>Hertz; cycles per second.</td>
</tr>
<tr>
<td>IEC</td>
<td>International Electrotechnical Commission; an organization that sets international electrical and electronics standards.</td>
</tr>
<tr>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers.</td>
</tr>
<tr>
<td>I&lt;sub&gt;MP&lt;/sub&gt;</td>
<td>Mainframe peak current.</td>
</tr>
<tr>
<td>in.</td>
<td>Inches.</td>
</tr>
<tr>
<td>inhibit</td>
<td>To turn off.</td>
</tr>
</tbody>
</table>
Glossary

J

jitter  A measure of the small, rapid variations in clock transition times from their nominal regular intervals. Units: seconds RMS.

K

kg  Kilograms.

km  Kilometers.

L

lb  Pounds.

LED  Light emitting diode.

line regulation  The maximum steady-state percentage that a DC voltage output will change as a result of a specified change in input AC voltage (step change from 90 to 132 VAC or 180 to 264 VAC).

load regulation  The maximum steady-state percentage that a DC voltage output will change as a result of a step change from no-load to full-load output current.

M

m  Meters.

MHz  Megahertz. One million Hertz; one Hertz equals one cycle per second.

mi  Miles.

ms  Milliseconds.

MTBF  Mean time between failure.

MTTR  Mean time to repair.
N

NEMA National Electrical Manufacturers Association.

NI National Instruments.

P

power supply shuttle A removable module that contains the chassis power supply.

PXI PCI eXtensions for Instrumentation.

PXI_CLK10 10 MHz PXI system reference clock.

R

RH Relative humidity.

RMS Root mean square.

S

s Seconds.

skew Deviation in signal transmission times.

slot blocker An assembly installed into an empty slot to improve the airflow in adjacent slots.

SMA SubMiniature version A connector; a commonly used coaxial connector.

standby The backplane is unpowered (off), but the chassis is still connected to AC power mains.

System controller A module configured for installation in Slot 1 of a PXI chassis. This device is unique in the PXI system in that it performs the system controller functions, including clock sourcing and arbitration for data transfers across the backplane. Installing such a device into any other slot can damage the device, the PXI backplane, or both.
system reference clock  A 10 MHz clock, also called PXI_CLK10, that is distributed to all peripheral slots in the chassis, as well as a BNC connector on the rear of chassis labeled 10 MHz REF OUT. The system reference clock can be used for synchronization of multiple modules in a measurement or control system. The 10 MHz REF IN and OUT BNC connectors on the rear of the chassis can be used to synchronize multiple chassis to one reference clock. The PXI backplane specification defines implementation guidelines for PXI_CLK10.

T
TTL  Transistor-transistor logic.

U
UL  Underwriter’s Laboratories.

V
V  Volts.
VAC  Volts alternating current.
V_{pp}  Peak-to-peak voltage.

W
W  Watts.
Index

A
AC power cables (table), 1-2

B
backplane
  hybrid peripheral slots, 1-7
  interoperability with CompactPCI, 1-5
overview, 1-5
PXI local bus, routing, 1-8
system controller slot, 1-6
system reference clock, 1-9
trigger bus, 1-8

C
cables, power (table), 1-2
chassis ambient temperature definitions, 2-4
chassis cooling considerations
  ambient temperature definitions, 2-4
  clearances, 2-2
chassis initialization file, 2-23
clearances for chassis cooling, 2-2
CompactPCI
  interoperability with PXIe-1084
  backplane, 1-5
configuration. See installation, configuration, and operation
cooling
  filler panel installation, 2-5
  slot blocker installation, 2-5

E
EMC filler panel kit, 1-5

F
fan module, replacing, 1-5
filler panel installation, 2-5

G
ground, connecting, 2-6

H
High Density Triggers, 2-14
hybrid peripheral slots, description, 1-7
hybrid slot pinouts
  P1 connector (table), A-3, A-4
  XP3 connector (table), A-5
  XP4 connector (table), A-5

I
IEC 320 inlet, 2-7
installation, configuration, and operation
  chassis initialization file, 2-23
  connecting safety ground, 2-6
  filler panel installation, 2-5
  installing a PXI Express system
    controller, 2-7
  peripheral module installation, 2-9
  PXI Express configuration in MAX, 2-19
  rack mounting, 2-5
  site considerations, 2-2
  slot blocker installation, 2-5
  testing power up, 2-7
  unpacking the PXIe-1084, 1-1
interoperability with CompactPCI, 1-5

K
key features, 1-2
kit contents, 1-1

L
LED indicators, 2-10
  front panel LED states (table), 2-10, 2-11
Index

M
maintenance of PXIe-1084 chassis, 3-1
cleaning
  exterior cleaning, 3-2
  interior cleaning, 3-2
preparation, 3-1
service interval, 3-1
static discharge damage (caution), 3-1

O
optional equipment, 1-5

P
peripheral module installation, 2-9
pinouts, A-1
power cables (table), 1-2
power supply
  connecting to, 2-7
  replacing
    connecting safety ground, 3-2
    connecting to power source, 3-2
power up, testing, 2-7
PXI Express configuration in MAX, 2-19
PXI Express system controller, 2-7
PXI local bus, routing, 1-8
PXIe-1084 backplane
  hybrid peripheral slots, 1-7
  interoperability with CompactPCI, 1-5
  overview, 1-5
  PXI local bus, routing, 1-8
  system controller slot, 1-6
  system reference clock, 1-9
  trigger bus, 1-8
PXIe-1084 chassis
  installation. See installation, configuration, and operation
  key features, 1-2
  maintenance. See maintenance of
    PXIe-1084 chassis
  optional equipment, 1-5
  rack mounting, 2-5
  safety ground, connecting, 2-6
  unpacking, 1-1

R
rack mounting, 2-5
  kit, 1-5

S
safety and caution notices, 2-1
safety ground, connecting, 2-6
service interval, 3-1
slot blocker
  installation, 2-5
  kit, 1-5
static discharge damage (caution), 3-1
system controller slot
  description, 1-6
  pinouts
    XP1 connector (table), A-2
    XP2 connector (table), A-2
    XP3 connector (table), A-3
system reference clock, 1-9

T
testing power up, 2-7
trigger bus, 1-8

U
unpacking the PXIe-1084 chassis, 1-1