The NI 5782 is an analog dual-input, dual-output, intermediate-frequency (IF) transceiver adapter module designed to work with your NI FlexRIO™ FPGA module. The NI 5782 features two analog input (AI) channels with 14-bit sample rates of up to 250 MS/s. The NI 5782 also has two analog output (AO) channels with 16-bit sample rates of up to 500 MS/s when using both AO channels, or up to 1 GS/s when using only one AO channel.

This document contains signal information and specifications for the NI 5782R, which is composed of an NI FlexRIO FPGA module and the NI 5782 adapter module. This document also contains tutorial sections that demonstrate how to acquire data using a LabVIEW FPGA example VI and how to create and run your own LabVIEW project with the NI 5782R.

Note  NI 5782R refers to the combination of your NI 5782 adapter module and your NI FlexRIO FPGA module. NI 5782 refers to your NI 5782 adapter module only.

Caution  The protection provided by the NI 5782R can be impaired if it is used in a manner not described in this document.

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Before configuring your NI 5782R, you must install the appropriate software and hardware. Refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications* for installation instructions. Figure 1 shows an example of a properly connected NI FlexRIO device.

**Electromagnetic Compatibility Guidelines**

This product was tested and complies with the regulatory requirements and limits for electromagnetic compatibility (EMC) as stated in the product specifications. These requirements and limits are designed to provide reasonable protection against harmful interference when the product is operated in its intended operational electromagnetic environment.

This product is intended for use in industrial locations. There is no guarantee that harmful interference will not occur in a particular installation, when the product is connected to a test object, or if the product is used in residential areas. To minimize the potential for the product to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this product in strict accordance with instructions in the product documentation.

Furthermore, any changes or modifications to the product not expressly approved by National Instruments could void your authority to operate it under your local regulatory rules.

**Caution** To ensure the specified EMC performance, you must install PXI EMC Filler Panels (National Instruments part number 778700-01) in adjacent chassis slots. For more information about installing PXI EMC filler panels in your system, refer to the *Appendix B: Installing EMI Controls* section of this document.

**Caution** To ensure the specified EMC performance, operate this product only with shielded cables and accessories.

**Caution** This product is sensitive to electrostatic discharge (ESD). To ensure the specified EMC performance, follow the programming instructions listed at the end of the *Using Your NI 5782R with a LabVIEW FPGA Example VI* and *Creating a LabVIEW Project and Running a VI on an FPGA Target* sections of this document.
Caution To ensure the specified EMC performance, the length of all I/O cables must be no longer than 30 m (100 ft).

How to Use Your NI FlexRIO Documentation Set

Refer to Figure 2 and Table 1 for information about how to use your NI FlexRIO documentation set.

**Figure 2.** How to Use Your NI FlexRIO Documentation Set

INFILL Diagram with boxes and arrows connecting them.

- INSTALL Hardware and Software
- CONNECT Signals and Learn About Your Adapter Module
- LEARN About LabVIEW FPGA Module
- Are You New to LabVIEW FPGA Module?
  - Yes → LabVIEW FPGA Module Help
  - No → NI FlexRIO Help
- PROGRAM Your NI FlexRIO System in LabVIEW FPGA Module
- LabVIEW Examples
Front Panel and Connector Pinouts

Table 2 shows the front panel connector and signal descriptions for the NI 5782. Refer to Appendix A: Specifications for additional signal information.

Caution To avoid permanent damage to the NI 5782, disconnect all signals connected to the NI 5782 before powering down the module, and connect signals only after the adapter module has been powered on by the NI FlexRIO FPGA module.

Caution Connections that exceed any of the maximum ratings of any connector on the NI 5782R can damage the device and the chassis. NI is not liable for any damage resulting from such signal connections. For the maximum input and output ratings for each signal, refer to Appendix A: Specifications.
Table 2. NI 5782 Front Panel Connectors

<table>
<thead>
<tr>
<th>Device Front Panel</th>
<th>Connector</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>AUX I/O</td>
<td>Refer to Table 3 for the signal list and descriptions.</td>
</tr>
<tr>
<td></td>
<td>CLK IN</td>
<td>50 Ω single-ended (SE) external Reference or Sample Clock input.</td>
</tr>
<tr>
<td></td>
<td>TRIG</td>
<td>Trigger input channel.</td>
</tr>
<tr>
<td></td>
<td>AI 0</td>
<td>50 Ω SE analog input (AI) channel 0.</td>
</tr>
<tr>
<td></td>
<td>AI 1</td>
<td>50 Ω SE AI channel 1.</td>
</tr>
<tr>
<td></td>
<td>AO 0</td>
<td>50 Ω SE analog output (AO) channel 0.</td>
</tr>
<tr>
<td></td>
<td>AO 1</td>
<td>50 Ω SE AO channel 1.</td>
</tr>
</tbody>
</table>
AUX I/O Connector

Table 3. NI 5782 AUX I/O Connector Pin Assignments

<table>
<thead>
<tr>
<th>AUX I/O Connector</th>
<th>Pin</th>
<th>Signal</th>
<th>Signal Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>1</td>
<td>DIO Port 0 (Bit 0)</td>
<td>Bidirectional single-ended (SE) digital I/O (DIO) data channel.</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>GND</td>
<td>Ground reference for signals.</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>DIO Port 0 (Bit 1)</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>DIO Port 0 (Bit 2)</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>GND</td>
<td>Ground reference for signals.</td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>DIO Port 0 (Bit 3)</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>DIO Port 1 (Bit 0)</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>8</td>
<td>GND</td>
<td>Ground reference for signals.</td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>DIO Port 1 (Bit 1)</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>DIO Port 1 (Bit 2)</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>11</td>
<td>GND</td>
<td>Ground reference for signals.</td>
</tr>
<tr>
<td></td>
<td>12</td>
<td>DIO Port 1 (Bit 3)</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>13</td>
<td>PFI 0</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>NC</td>
<td>No connect.</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>PFI 1</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>16</td>
<td>PFI 2</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
<tr>
<td></td>
<td>17</td>
<td>GND</td>
<td>Ground reference for signals.</td>
</tr>
<tr>
<td></td>
<td>18</td>
<td>+5V</td>
<td>+5 V power (10 mA maximum).</td>
</tr>
<tr>
<td></td>
<td>19</td>
<td>PFI 3</td>
<td>Bidirectional SE DIO data channel.</td>
</tr>
</tbody>
</table>

⚠️ **Caution** The AUX I/O connector accepts a standard, third-party HDMI cable, but the AUX I/O port is not an HDMI interface. Do not connect the AUX I/O port on the NI 5782 into the HDMI port of another device. NI is not liable for any damage resulting from such signal connections.
Block Diagram

Figure 3 shows the NI 5782 block diagram and signal flow to and from the NI 5782 component-level intellectual property (CLIP) by way of the adapter module and the corresponding NI 5782 Multiple Sample CLIP in LabVIEW FPGA.

**Figure 3. NI 5782 Connector Signals and NI 5782 CLIP Signal Block Diagram**

---

NI 5782 Adapter Module

- **AUX I/O**
- **Bus Transceiver**

**Internal Reference Clock**

**Switch**

**Clock Synthesizer**

**Switch**

**AD9512**

**Sample Clock**

**ADC Interface**

**DAC Interface**

**Analog Front End**

**Switch**

**Clock Buffer**

**SPI Engine**

- **Interface with:**
  - AD9512
  - ADCs
  - DACs
  - Switches
  - Analog front end (FE)

**Data Clock**

**Sample Clock**

**AI 0 Data N**

**AI 0 Data N-1**

**AI 1 Data N**

**AI 1 Data N-1**

**AO 0 Data N**

**AO 0 Data N-1**

**AO 0 Data N-3**

**AO 1 Data N**

**AO 1 Data N-1**

**AO 1 Data N-2**

**AO 1 Data N-3**

**Trigger Input**

**DIO Port 0 Rd Data <0..3>,**

**DIO Port 1 Rd Data <0..3>,**

**DIO Port 0 Wr Data <0..3>,**

**DIO Port 1 Wr Data <0..3>,**

**PRI <0..3> Rd Data**

**PRI <0..3> Wr Data**

**PRI <0..3> Write Enable**

**PRI <0..3> Write Enable**

---

NI 5782R User Manual and Specifications | © National Instruments | 7
NI 5782 Component-Level Intellectual Property (CLIP)

The LabVIEW FPGA Module includes component-level intellectual property (CLIP) for HDL IP integration. NI FlexRIO devices support two types of CLIP: user-defined and socketed.

- **User-defined CLIP** allows you to insert HDL IP into an FPGA target, enabling VHDL code to communicate directly with an FPGA VI.
- **Socketed CLIP** provides the same IP integration functionality of the user-defined CLIP, but also allows the CLIP to communicate directly with circuitry external to the FPGA. Adapter module socketed CLIP allows your IP to communicate directly with both the FPGA VI and the external adapter module connector interface.

The following figure shows the relationship between an FPGA VI and CLIP.

**Figure 4. CLIP and FPGA VI Relationship**

![Diagram showing the relationship between an FPGA VI and CLIP](image-url)
The NI 5782 ships with socketed CLIP items that add module I/O to the LabVIEW project. The NI 5782 ships with the following CLIP items:

1. **NI 5782 Multiple Sample CLIP**—The analog input channels generate two samples per clock cycle at a clock rate that is half the sample rate. The analog output channels generate four samples per clock cycle at a clock rate that is one quarter of the sample rate. The AI default sample rate is 250 MHz, and the AO default sample rate is 500 MHz. The default clock rate for this CLIP is 125 MHz. You can set a lower sample rate by using an external Sample Clock.

   This CLIP presents the data to the diagram in a decelerated format. The ADC data lands at half the rate as the ADC clock. The DAC data must be presented in four time samples per clock on each channel.

   This CLIP provides access to two AI channels, two AO channels, eight bidirectional DIO channels, four bidirectional PFI channels, and an input clock selector that can be configured to use one of the following settings:
   - Internal Sample Clock
   - Internal Sample Clock locked to an external Reference Clock through the CLK IN connector
   - External Sample Clock through the CLK IN connector
   - Internal Sample Clock locked to an external Reference Clock through IoModSyncClock
   - External Sample Clock through IoModSyncClock

   This CLIP also contains an engine to program the CLK chip, ADCs, and DACs, either through predetermined settings for an easier instrument setup, or through a raw SPI address and data signals for a more advanced setup. The NI 5782 Multiple Sample CLIP is the default CLIP.

2. **NI 5782 Single Sample CLIP**—The analog input channels generate one sample per clock cycle and the analog output channels generate two samples per clock cycle. The default clock rate for the Multiple Sample CLIP is 250 MHz. The Sample Clock rates of AI (250 MHz) and AO (500 MHz) are the same as Multiple Sample CLIP. You can set lower sample rates with the external Sample Clock.

   This CLIP presents the data to the diagram at a clock rate such that the ADC data lands at the same rate as the ADC clock. However, the DAC data must be presented in two time samples per clock on each channel.

   This CLIP provides access to two AI channels, two AO channels, eight bidirectional DIO channels, four bidirectional PFI channels, and an input clock selector that can be configured to use one of the following settings:
   - Internal Sample Clock
   - Internal Sample Clock locked to an external Reference Clock through the CLK IN connector
   - External Sample Clock through the CLK IN connector
– Internal Sample Clock locked to an external Reference Clock through IoModSyncClock
– External Sample Clock through IoModSyncClock

This CLIP also contains an engine to program the CLK chip, ADCs, and DACs, either through predetermined settings for an easier instrument setup, or through a raw SPI address and data signals for a more advanced setup.

Refer to the *NI FlexRIO Help* for more information about NI FlexRIO CLIP items, how to configure the NI 5782 with a socketed CLIP, and for a list of available socketed CLIP signals.

## Connecting Cables

- Use any 50 Ω SMA cable to connect signals to the connectors on the front panel of your NI 5782.
- Use the SHH19-H19-AUX cable (NI part number: 152629-01 or 152629-02) to connect to the DIO and PFI signals on the AUX I/O connector.

For more information about connecting I/O signals on your device, refer to the *Appendix A: Specifications* section of this document.

## Clocking

The NI 5782 clocks control the sample rate and other timing functions on the device. Table 4 contains information about the possible NI 5782 clock resources.

<table>
<thead>
<tr>
<th>Clock</th>
<th>Frequency</th>
<th>Source Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal Clock</td>
<td>500 MHz</td>
<td>The internal voltage-controlled oscillator (VCO) acts as a free-running clock.</td>
</tr>
<tr>
<td>PLL Off</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Clock</td>
<td>500 MHz</td>
<td>The internal VCO locks to PXI_CLK10 through IoModSyncClock, which is available only through the backplane of NI PXIe-796xR devices.</td>
</tr>
<tr>
<td>PLL On</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IoModSyncClock</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Internal Clock</td>
<td>500 MHz</td>
<td>The internal VCO locks to an external Reference Clock (10 MHz). Connect the external Reference Clock through the CLK IN front panel connector.</td>
</tr>
<tr>
<td>PLL On</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(CLK IN)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>External Clock</td>
<td>250 MHz to 1 GHz</td>
<td>Connect an external Sample Clock through the CLK IN front panel connector.</td>
</tr>
</tbody>
</table>
Using Your NI 5782R with a LabVIEW FPGA Example VI

Note You must install the software before running this example. Refer to the NI FlexRIO FPGA Module Installation Guide and Specifications for more information about installing your software.

The NI FlexRIO Adapter Module Support software includes example projects to help you get started creating your LabVIEW FPGA application. This section explains how to use an existing LabVIEW FPGA example project to generate and acquire samples with the NI 5782R. This example requires at least one SMA cable to connect signals to your NI 5782R.

Note The examples available for your device depend on the version of the software and driver you are using. For more information about which software versions are compatible with your device, visit ni.com/info and enter rdsoftwareversion in the text field.

Each NI 5782R example project includes the following components:

• A LabVIEW FPGA VI that can be compiled and run on the FPGA embedded in the hardware
• A VI that runs on Windows and interacts with the LabVIEW FPGA VI

Note In the LabVIEW FPGA Module software, NI FlexRIO adapter modules are referred to as IO Modules.

Complete the following steps to run an example that acquires a waveform on CH0 of the NI 5782.

1. Connect one end of an SMA cable to AI0 on the front panel of the NI 5782 and the other end of the cable to your device under test (DUT).
2. Launch LabVIEW.
3. Click Help»Find Examples to display the NI Example Finder.
4. In the NI Example Finder window, select Hardware Input and Output»FlexRIO»IO Modules»NI 5782.
5. Select NI 5782 - Getting Started.lvproj.
6. In the Project Explorer window, open NI 5782 - Getting Started (Host).vi under My Computer to open the host VI. The Open FPGA VI Reference function in this VI uses the NI 7952R as the FPGA target by default. If you are using an NI FlexRIO FPGA module other than the NI 7952R, complete the following steps to change to the FPGA VI to support your target.
   a. Select Windows»Show Block Diagram to open the VI block diagram.
   b. On the block diagram, right-click the Open FPGA VI Reference (PXI-7952R) function and select Configure Open FPGA VI Reference.
c. In the **Configure Open FPGA VI Reference** dialog box, click the **Browse** button next to the **Bitfile** button.

d. In the **Select Bitfile** dialog box that opens, select the bitfile for your desired target. The bitfile name is based on the adapter module, example type, and FPGA module.

e. Click the **Select** button.

f. Click **OK** in the **Configure Open FPGA VI Reference** dialog box.

g. Save the VI.

7. On the front panel, in the **RIO Resource** pull-down menu, select an NI 5782R resource that corresponds with the target that you configured in step 6.

8. Select **AI 0** in the **AI Channel control**.

9. Set the **Trigger Level (V)** and the **Record Size** controls to the desired values.

10. In the **Trigger Type** box, select either **Software** or **Data Edge**. If you select **Software**, the VI acquires data every time you click the **Software Trigger** button on the front panel of the VI. If you select **Data Edge**, the VI acquires data every time an edge occurs.

11. Click the **Run** button to run the VI.

12. Click the **Software Trigger** button if you selected **Software** in the **Trigger Type** control. The VI acquires data and displays the captured waveform on the **Acquired Waveform** graph as shown in Figure 5.

13. Click the **STOP** button to stop the VI.

14. Close the VI.
Creating a LabVIEW Project and Running a VI on an FPGA Target

This section explains how to set up your target and create an FPGA VI and a host VI for data communication. This section focuses on proper project configuration, proper CLIP configuration, and how to access 5782 AI IO nodes. For more detailed information about acquiring data on your NI 5782R, refer to the device-specific examples available in NI Example Finder.

Creating a Project

1. Launch LabVIEW. If LabVIEW is already running, select File » Create Project.
2. In the Create Project dialog box, select LabVIEW FPGA Project and click Finish.
3. In the Create New LabVIEW FPGA Project dialog box, select FlexRIO on My Computer and click Next.
4. If your FlexRIO device is connected to your system, select Discover Existing System. If your device is not connected to your system, select Create New System and click Next.
5. Select your device and click Next.
6. LabVIEW generates a preview of your project. Verify that the project is correct and select Finish. The new project opens in the Project Explorer window.

Creating an FPGA Target VI
1. Right-click FPGA Target (RIOx, PXI-79xxR) and select New»FPGA Base Clock.
2. In the Resource pull-down menu, select 200 MHz Clock and click OK.
3. Right-click IO Module (5782) in the Project Explorer window and select Properties.
4. In the Clock Selections category, select 200 MHz Clock from the pull-down menu for Clk200. Leave Clk40 configured as the Top-Level Clock.
5. Select NI 5782 CLIP in the Name list of the Component Level IP pane.
6. In the Clock Selections category, select 200 MHz Clock from the pull-down menu for Clk200. Leave Clk40 configured as the Top-Level Clock.
7. Click OK.

**Note** Configuring these clocks is required for proper CLIP operation. Refer to the NI 5782 CLIP topics in the NI FlexRIO Help for more information about configuring your clocks.

8. In the Project Explorer window, right-click the FPGA target and select New»VI to open a blank VI.
9. Select Window»Show Block Diagram to open the VI block diagram.
10. In the Project Explorer window, expand the IO Module (NI 5782 : NI 5782) tree view.
11. Drag AI 0 Data N-1 to the block diagram.
12. Click and drag the bottom edge of the control node to expose the other signals, AI 0 N-1…AI 1 N.
13. Add a Timed Loop structure around the node.
14. Wire indicators to each output terminal of the IO Module\AI 0 N-1…AI 1 N.
15. Right-click the input node of the Timed Loop to wire an FPGA Clock Constant to the node. Set this constant to IO Module\Data Clock.

Your block diagram should resemble the block diagram in Figure 6.

---

**Figure 6. 5782SampleAcq (FPGA).vi Block Diagram**
Tip  Click the Clean Up Diagram button on the toolbar to cleanly organize the VI block diagrams.

16. Save the VI as 5782SampleAcq (FPGA).vi.
17. Click the Run button. LabVIEW creates a default build specification and begins compiling the VI. The Generating Intermediate Files window opens and displays the code generation progress. Next, the Compilation Status window opens and displays the progress of the compilation. The compilation takes several minutes.

18. Click Close in the Compilation Status window.
19. Save and close the VI.
20. Save the project.

Creating a Host VI

1. In the Project Explorer window, right-click My Computer and select New»VI to open a blank VI.
2. Select Window»Show Block Diagram to open the VI block diagram.
3. Add the Open FPGA VI Reference function, located on the FPGA Interface palette, to the block diagram.
4. Drag and drop your 5782SampleAcq(FPGA).vi into the Open FPGA VI Reference. The target name appears under the Open FPGA VI Reference function in the block diagram.
5. In the block diagram, add a While Loop to the right of the Open FPGA VI Reference function.
6. Right-click the conditional terminal inside the While Loop and select Create Control to create a STOP button on the VI front panel window.
7. Add the Read/Write Control function, located on the FPGA Interface palette, inside the While Loop.
8. Wire the FPGA VI Reference Out output terminal of the Open FPGA VI Reference function to the FPGA VI Reference In input terminal of the Read/Write Control function.
9. Wire the error out terminal of the Open FPGA VI Reference function to the error in control of the Read/Write Control function.
10. Configure the Read/Write Control function by clicking the terminal section labeled Unselected, and selecting IO Module/AI 0 N-1.
11. Click and drag the bottom edge of the control edge to expose the other signals, AI 0 N-1...AI 1 N, to the Read/Write Control function.
12. Wire indicators to each output terminal of the IO Module\AI 0 N-1...AI 1 N.
13. Add the Close FPGA VI Reference function, located on the FPGA Interface palette, to the right of the While Loop on the block diagram.
14. Wire the FPGA VI Reference Out terminal of the Read/Write Control function to the FPGA VI Reference In terminal of the Close FPGA VI Reference function.
15. Wire the error out terminal of the Read/Write Control function to the error in terminal of the Close FPGA VI Reference function.
Your block diagram should resemble the block diagram in Figure 7.

**Figure 7. 5782SampleAcq(Host).vi Block Diagram**

16. Save the VI as 5782SampleAcq(Host).vi.

### Running the Host VI

1. Connect one end of an SMA cable to AI 0 on the front panel of the NI 5782 and the other end of the cable to your DUT.
2. Open the front panel of 5782SampleAcq(Host).vi.
3. Click the **Run** button to run the VI.
4. The VI acquires data from the DUT on AI 0, AI 0 N-1, AI 1 N, and AI 1 N-1.
5. Click the **STOP** button on the front panel and close the VI.

### Appendix A: Specifications

This section lists the specifications of the NI FlexRIO adapter module (NI 5782). Pair these specifications with the specifications listed in the *NI FlexRIO FPGA Module Installation Guide and Specifications*. For more information about safety and electromagnetic compatibility refer to the *Read Me First: Safety and Electromagnetic Compatibility* document included in your hardware kit or available at [ni.com/manuals](http://ni.com/manuals).

**Caution**  To avoid permanent damage to the NI 5782, disconnect all signals connected to the NI 5782 before powering down the module, and only connect signals after the module has been powered on by the NI FlexRIO FPGA module.

**Note**  All numeric specifications are typical unless otherwise noted. All graphs illustrate the performance of a representative module.

Specifications are subject to change without notice. For the most recent device specifications, visit [ni.com/manuals](http://ni.com/manuals).
Analog Input (AI 0 and AI 1)

General Characteristics
Number of channels.......................................... Two, single-ended, simultaneously sampled
Connector.......................................................... SMA
Input impedance ............................................... 50 Ω, per connector
Sample rate
Internal Sample Clock ...................................... 250 MHz
External Sample Clock ...................................... 175 MHz to 250 MHz
ADC part number ............................................. ADS62P49; 14-bit resolution, dual ADC

AC-Coupled Specifications
Input range (normal operating conditions) ...... +10.2 dBm (2.05 Vpk-pk)
Absolute maximum input ................................. 50 Ω, ±10 V DC, +18 dBm (5 Vpk-pk) AC
Bandwidth (-1 dB) ............................................ 1 MHz to 250 MHz
Bandwidth (-3 dB) ............................................ 0.1 MHz to 500 MHz

Table 5 lists the AC-coupled spectral performance measurements. All values are measured with a 500 MHz internal Sample Clock.

Table 5. Analog Input AC-Coupled Spectral Performance

<table>
<thead>
<tr>
<th>Measurement</th>
<th>20.1 MHz</th>
<th>70.1 MHz</th>
<th>124.1 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Signal-to-noise ratio (SNR)</td>
<td>70.5 dB</td>
<td>70.0 dB</td>
<td>68.8 dB</td>
</tr>
<tr>
<td>Signal-to-noise and distortion ratio (SINAD)</td>
<td>70.5 dB</td>
<td>69.8 dB</td>
<td>68.6 dB</td>
</tr>
<tr>
<td>Spurious-free dynamic range (SFDR)</td>
<td>90.0 dB</td>
<td>83.0 dB</td>
<td>80.0 dB</td>
</tr>
</tbody>
</table>

Channel-to-channel isolation
1 MHz........................................................... >90 dB
100.1 MHz.................................................. 90 dB
501 MHz................................................... 70 dB

1 For additional information on the ADS62P49, refer to the Texas Instruments device data sheet at www.ti.com.
**Figure 8.** Bandwidth (Passband)

![Bandwidth Graph](image)

**Figure 9.** Terminated Input

![Terminated Input Graph](image)
**Figure 10.** Analog Input One-Tone Spectral Measurement (70 MHz, -1 dBFS)

![Figure 10](image)

**Figure 11.** Two-Tone Spectral Measurement (19.5 and 20.5 MHz, -10 dBFS)

![Figure 11](image)
DC-Coupled Specifications

Input range (normal operating conditions) ……. +4.0 dBm, 1.0 V_{pk-pk}

Absolute maximum input…………………………..50 Ω, ±4.5 V DC, +15 dBm (3.6 V_{pk-pk}) AC

Bandwidth (-1 dB) ……………………………..DC to 170 MHz

Bandwidth (-3 dB) ……………………………..DC to 330 MHz

Table 6 lists the DC-coupled spectral performance measurements. All values are measured with a 1 GHz internal Sample Clock.

<table>
<thead>
<tr>
<th>Measurement</th>
<th>20.1 MHz</th>
<th>70.1 MHz</th>
<th>124.1 MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>SNR</td>
<td>67.3 dB</td>
<td>66.2 dB</td>
<td>65.5 dB</td>
</tr>
<tr>
<td>SINAD</td>
<td>67.0 dB</td>
<td>65.4 dB</td>
<td>64.0 dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>80.0 dB</td>
<td>78.0 dB</td>
<td>66.0 dB</td>
</tr>
</tbody>
</table>

Channel-to-channel isolation

1 MHz ………………………………………………. 85 dB
100.1 MHz ………………………………………… 85 dB
501 MHz ………………………………………… 60 dB

Figure 12. Analog Input Bandwidth (Passband)
Figure 13. Analog Input Terminated Input

Figure 14. Analog Input One-Tone Spectral Measurement (70 MHz, -1 dBFS)
Figure 15. Two-Tone Spectral Measurement (19.5 and 20.5 MHz, -10 dBFS)

Analog Output (AO 0 and AO 1)

General Characteristics

Number of channels ..........................................Two, single-ended, simultaneously sampled
Connector ..........................................................SMA
Output impedance .............................................50 Ω, per connector
Sample rate
   DLL Off ....................................................<250 MHz
   DLL On.....................................................250 MHz to 1 GHz
DAC part number..............................................DAC5682Z\(^1\); 16-bit resolution, dual DAC

\(^1\) For additional information on the DAC5682Z, refer to the Texas Instruments device data sheet at www.ti.com.
AC-Coupled Specifications

Output range (normal operating conditions) .... -0.5 dBm (0.6 V_{pk-pk})

Bandwidth (-3 dB) ............................................ 1 MHz to 225 MHz\(^1\)

SNR .............................................................. 70 dBc

Table 7. SFDR (70 MHz Out, 1 GS/s, no PLL)

<table>
<thead>
<tr>
<th></th>
<th>Second Harmonic</th>
<th>Third Harmonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-Harmonic</td>
<td>61 dBc</td>
<td>72 dBc</td>
</tr>
<tr>
<td>77 dBc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Channel-to-channel isolation

1 MHz ...................................................... 100 dB
100.1 MHz ................................................ 90 dB
251 MHz ................................................... 90 dB

Figure 16. Bandwidth (Passband)

---

\(^1\) Includes DAC sinc response.
Figure 17. Analog Output One-Tone Spectral Measurement (70 MHz, 0.25 dBm, 100 Hz Resolution Bandwidth, 100 kHz Bandwidth)

Figure 18. Analog Output One-Tone Spectral Measurement (70 MHz, 0.25 dBm, 1 kHz Resolution Bandwidth, 1 MHz Bandwidth)
**Figure 19.** Analog Output One-Tone Spectral Measurement (70 MHz, 0.25 dBm, 1 kHz Resolution Bandwidth, 100 MHz Bandwidth)

![Graph showing an analog output one-tone spectral measurement with a 70 MHz frequency range, 0.25 dBm amplitude, 1 kHz resolution bandwidth, and 100 MHz bandwidth.]

**Figure 20.** Analog Output One-Tone Spectral Measurement (70 MHz, 0.25 dBm, 1 kHz Resolution Bandwidth, 500 MHz Bandwidth)

![Graph showing an analog output one-tone spectral measurement with a 70 MHz frequency range, 0.25 dBm amplitude, 1 kHz resolution bandwidth, and 500 MHz bandwidth.]
DC-Coupled Specifications

Output range (normal operating conditions)..................+4 dBm (1.0 V_{pk-pk})
Bandwidth (-3 dB)..............................................DC to 180 MHz\(^1\)
SNR.................................................................66 dBc

<table>
<thead>
<tr>
<th>Table 8. SFDR (70 MHz Out, 1 GS/s, no PLL)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-Harmonic</td>
</tr>
<tr>
<td>---------------</td>
</tr>
<tr>
<td>77 dBc</td>
</tr>
</tbody>
</table>

Channel-to-channel isolation

1.0 MHz..................................................100 dB
100.1 MHz................................................100 dB
251.0 MHz..............................................87 dB

Figure 21. Analog Output Bandwidth (Passband)

\(^1\) Includes DAC sinc response.
Figure 22. Analog Output One-Tone Spectral Measurement (70 MHz, 0.25 dBm, 100 Hz Resolution Bandwidth, 100 kHz Bandwidth)

Figure 23. Analog Output One-Tone Spectral Measurement (70 MHz, 0.25 dBm, 1 kHz Resolution Bandwidth, 1 MHz Bandwidth)
Internal Sample Clock

General Characteristics

Oscillator type.............................................. Fixed frequency synthesizer
Frequency (default)........................................ 1 GHz
Reference spurs.............................................. <60 dBc
Phase noise

<table>
<thead>
<tr>
<th>Offset</th>
<th>Phase Noise (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 kHz</td>
<td>-95 dBc/Hz</td>
</tr>
<tr>
<td>100 kHz</td>
<td>-115 dBc/Hz</td>
</tr>
</tbody>
</table>

Clock distribution part number ................................ AD9512

Reference Clock sources ........................................... Internal, External through the CLK IN connector, or IoModSyncClock

Internal reference type ........................................... TCXO

Internal reference stability ...................................... ±1 ppm

Internal reference frequency (default) ......................... 10 MHz

Internal reference phase noise

<table>
<thead>
<tr>
<th>Offset</th>
<th>Phase Noise (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 kHz</td>
<td>-137 dBc/Hz</td>
</tr>
<tr>
<td>10 kHz</td>
<td>-150 dBc/Hz</td>
</tr>
<tr>
<td>100 kHz</td>
<td>-155 dBc/Hz</td>
</tr>
</tbody>
</table>

CLK IN

General Characteristics

Number of channels .................................................. 1, single-ended

Connector ..................................................................... SMA

Input impedance ....................................................... 50 Ω

Input coupling ......................................................... AC

External Sample Clock

Input voltage range .................................................. 0.63 Vpk-pk to 2.5 Vpk-pk

Input frequency range ............................................... 250 MHz to 1 GHz

Absolute maximum input .......................................... ±10 V DC, 3.1 Vpk-pk AC

Input power (50 Ω) .................................................... 0 dBm to 12 dBm

External Reference Clock

Input voltage range .................................................. 1.4 Vpk-pk to 4.4 Vpk-pk

Input frequency range ............................................... 10 MHz

Absolute maximum input .......................................... ±10 V DC, 5 Vpk-pk AC

Input power (50 Ω) .................................................... 7.0 dBm to 16.8 dBm

---

1 For additional information about the AD9512, refer to the Analog Devices device data sheet at www.analog.com.

2 IoModSyncClock is available only on NI PXIe-796xR FPGA modules.
TRIG

General Characteristics
Number of channels .......................................... 1, single-ended
Connector .......................................................... SMA
Input impedance ................................................ 10k Ω
Input coupling ................................................... DC

Table 9. Input Levels

<table>
<thead>
<tr>
<th>Voltage Level</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>0.0 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>$V_{IH}$</td>
<td>2.0 V</td>
<td>3.6 V</td>
</tr>
</tbody>
</table>

Absolute maximum input ...................................... ±10 V

AUX I/O (Port 0 DIO <0..3>, Port 1 DIO <0..3>, and PFI <0..3>)

General Characteristics
Number of channels .......................................... 12 bidirectional (8 DIO and 4 PFI)
Connector type .................................................. HDMI
Interface standard .............................................. 3.3 V LVCMOS

Interface logic

| Maximum $V_{IL}$ | -0.3 V |
| Minimum $V_{IL}$ | 0.8 V  |
| Minimum $V_{IH}$ | 2.0 V  |
| Maximum $V_{IH}$ | 3.6 V  |
| Maximum $V_{OL}$ | 0.4 V  |
| Minimum $V_{OL}$ | 0 V    |
| Minimum $V_{OH}$ | 2.7 V  |
| Maximum $V_{OH}$ | 3.6 V  |

$Z_{out}$ .......................................................... 50 Ω ± 20%
$I_{out}$ (DC) .................................................. ±2 mA

Pull-down resistor ................................................ 150 k Ω
Recommended operating voltage ................................. -0.3 V to 3.6 V
Overvoltage protection ........................................... ±10 V
Maximum toggle frequency ...................................... 6.6 MHz
+5 V maximum power........................................ 10 mA
+5 V voltage tolerance...................................... 4 V to 5.0 V

**EEPROM**

<table>
<thead>
<tr>
<th>Byte Address</th>
<th>Size (Bytes)</th>
<th>Field Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>2</td>
<td>Vendor ID</td>
</tr>
<tr>
<td>0x2</td>
<td>2</td>
<td>Product ID</td>
</tr>
<tr>
<td>0x4</td>
<td>4</td>
<td>Serial Number</td>
</tr>
<tr>
<td>0x8</td>
<td>116</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x7C</td>
<td>132</td>
<td>User Space</td>
</tr>
</tbody>
</table>

**Caution** Only write to *User Space*. Writing to any other offset may cause the NI 5782 to stop functioning.

**Power**

Power draw (W)

- AC-coupled build ..................................... 4.59
- DC-coupled build ..................................... 5.26

**DC Power Requirements**

- VCCOA, VCCOB ........................................... 2.37 V to 2.60 V
- VEEPROM .................................................. 2.50 V to 5.50 V
- P33V ...................................................... 3.09 V to 3.47 V
- P12V ...................................................... 11.12 V to 12.60 V

**Physical**

Dimensions ................................................................ 11.4 × 10.2 × 2.00 cm
(4.5 × 4.0 × 0.8 in.)

Weight.............................................................. 317.5 g (11.2 oz)
Environmental

Operating environment\textsuperscript{1} \ldots 0 °C to 55 °C, tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range \ldots 10% to 90%, noncondensing, tested in accordance with IEC-60068-2-56.

Maximum altitude \ldots 2,000 m at 25 °C ambient temperature.

Pollution Degree \ldots 2

Indoor use only.

Storage environment

Ambient temperature range \ldots -20 °C to 70 °C, tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.

Relative humidity range \ldots 5% to 95%, noncondensing, tested in accordance with IEC-60068-2-56.

\textbf{Note} Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Shock and Vibration

Operational shock \ldots 30 g peak, half-sine, 11 ms pulse, tested in accordance with IEC-60068-2-27. Test profile developed in accordance with MIL-PRF-28800F.

Random vibration

Operating \ldots 5 Hz to 500 Hz, 0.3 g\text{rms},

Nonoperating \ldots 5 Hz to 500 Hz, 2.4 g\text{rms}, tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.

Safety

This product meets the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

\begin{itemize}
  \item IEC 61010-1, EN 61010-1
  \item UL 61010-1, CSA 61010-1
\end{itemize}

\textsuperscript{1} For PXI/PXI Express chassis configurations that group NI FlexRIO adapter modules in three or more contiguous slots, National Instruments recommends limiting the ambient operating temperature to less than 50 °C.
Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia, and New Zealand (per CISPR 11), Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note For EMC declarations and certifications, refer to the Online Product Certification section of this document.

CE Compliance

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

To obtain product certifications and the Declaration of Conformity for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the Minimize Our Environmental Impact web page at ni.com/environment. This page contains the environmental regulations and directives.
with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

**EU Customers**  At the end of the product life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

Appendix B: Installing EMI Controls

To ensure specified EMC performance, an HDMI cable ferrite and PXI EMC filler panels must be properly installed in your NI FlexRIO system. Your kit includes the HDMI cable ferrite, but the PXI EMC filler panels (National Instruments part number 778700-01) must be purchased separately. For more installation information, refer to the *NI FlexRIO FPGA Module Installation Guide and Specifications*.

Installing PXI EMC Filler Panels

Complete the following instructions to install PXI EMC filler panels (National Instruments part number 778700-01) in your PXI chassis:

1. Remove the captive screw covers.
2. Install the PXI EMC filler panels by securing the captive mounting screws to the chassis, as shown in the figure below. Make sure that the EMC gasket is on the right side of the PXI EMC filler panel.
Figure 26. PXI EMC Filler Panels and Chassis

Note You must populate all slots with a module or a PXI EMC filler panel to ensure proper module cooling. Do not over tighten screws (2.5 lb-inch maximum). For additional information about the use of PXI EMC filler panels in your PXI system, visit ni.com/info and enter emcpa...
Where to Go for Support

The National Instruments website is your complete resource for technical support. At ni.com/support you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

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