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While this hardware is compliant with the applicable regulatory EMC requirements, there is no guarantee that interference will not occur in a particular installation. To minimize the potential for the hardware to cause interference to radio and television reception or to experience unacceptable performance degradation, install and use this hardware in strict accordance with the instructions in the hardware documentation and the DoC.

If this hardware does cause interference with licensed radio communications services or other nearby electronics, which can be determined by turning the hardware off and on, you are encouraged to try to correct the interference by one or more of the following measures:

- Reorient the antenna of the receiver (the device suffering interference).
- Relocate the transmitter (the device generating interference) with respect to the receiver.
- Plug the transmitter into a different outlet so that the transmitter and the receiver are on different branch circuits.

Some hardware may require the use of a metal, shielded enclosure (windowless version) to meet the EMC requirements for special EMC environments such as, for marine use or in heavy industrial areas. Refer to the hardware’s user documentation and the DoC for product installation requirements.

When the hardware is connected to a test object or to test leads, the system may become more sensitive to disturbances or may cause interference in the local electromagnetic environment.

Operation of this hardware in a residential area is likely to cause harmful interference. Users are required to correct the interference at their own expense or cease operation of the hardware.

Changes or modifications not expressly approved by National Instruments could void the user’s right to operate the hardware under the local regulatory rules.

1 The Declaration of Conformity (DoC) contains important EMC compliance information and instructions for the user or installer. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.
# Contents

## About This Manual
Related Documentation................................................................. ix

## Chapter 1
### Getting Started
Unpacking ............................................................................................... 1-1
What You Need to Get Started ......................................................... 1-1
Key Features ......................................................................................... 1-2
Chassis Description............................................................................. 1-3
Optional Equipment ............................................................................ 1-5
  - EMC Filler Panels ......................................................................... 1-5
  - Rack Mount Kit ............................................................................ 1-5
  - Slot Blockers ................................................................................ 1-6
  - Handle/Feet Kit ........................................................................... 1-6
NI PXIe-1071 Chassis Backplane Overview ............................................. 1-6
  - Interoperability with CompactPCI ............................................... 1-6
  - System Controller Slot ................................................................ 1-7
  - Hybrid Peripheral Slots ............................................................. 1-8
  - PXI Local Bus ............................................................................ 1-8
  - PXI Trigger Bus .......................................................................... 1-9
  - System Reference Clock ............................................................. 1-9

## Chapter 2
### Installation and Configuration
Safety Information ............................................................................... 2-1
Chassis Cooling Considerations ........................................................ 2-2
  - Providing Adequate Clearance .................................................. 2-2
  - Chassis Ambient Temperature Definition .................................... 2-6
Setting Fan Speed .............................................................................. 2-6
Installing Filler Panels ......................................................................... 2-6
Installing Slot Blockers ....................................................................... 2-6
Rack Mounting ................................................................................... 2-6
Connecting Safety Ground .................................................................. 2-7
Connecting to Power Source ............................................................. 2-7
Installing a PXI Express System Controller ........................................ 2-7
Installing Peripheral Modules ............................................................. 2-10
Power Inhibit Switch LED Indicator .................................................. 2-11
Inhibit Mode Switch ........................................................................... 2-12
Contents

PXI Express System Configuration with MAX ............................................................ 2-13
PXI-1 System Configuration ........................................................................... 2-14
Using System Configuration and Initialization Files .................................................... 2-15

Chapter 3
Maintenance
Service Interval .............................................................................................................. 3-1
Preparation .................................................................................................................... 3-1
Cleaning ........................................................................................................................ 3-2
Interior Cleaning ........................................................................................................ 3-2
Exterior Cleaning ......................................................................................................... 3-2

Appendix A
Specifications

Appendix B
Pinouts

Appendix C
Technical Support and Professional Services

Glossary

Index
About This Manual

The *NI PXIe-1071 User Manual* describes the features of the NI PXIe-1071 chassis and contains information about configuring the chassis, installing the modules, and operating the chassis.

Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *PICMG EXP.0 R1.0 CompactPCI Express Specification*, PCI Industrial Computers Manufacturers Group
- *PCI Express Base Specification*, Revision 2.0, PCI Special Interest Group
- *PXI-5 PXI Express Hardware Specification*, Revision 1.0, PXI Systems Alliance
Getting Started

This chapter describes the key features of the NI PXIe-1071 chassis and lists the kit contents and optional equipment you can order from National Instruments.

Unpacking

Carefully inspect the shipping container and the chassis for damage. Check for visible damage to the metal work. Check to make sure all handles, hardware, and switches are undamaged. Inspect the inner chassis for any possible damage, debris, or detached components. If damage appears to have been caused during shipment, file a claim with the carrier. Retain the packing material for possible inspection and/or reshipment.

What You Need to Get Started

The NI PXIe-1071 chassis kit contains the following items:

- NI PXIe-1071 chassis
- Filler panels
- AC power cable—refer to Table 1-1 for AC power cables
- NI PXIe-1071 User Manual
- Software media with PXI Platform Services 2.0 or higher
- Read Me First: Safety and Electromagnetic Compatibility
- Chassis number labels
Chapter 1  Getting Started

Table 1-1.  AC Power Cables

<table>
<thead>
<tr>
<th>Power Cable</th>
<th>Reference Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard 120 V (USA)</td>
<td>ANSI C73.11/NEMA 5-15-P/IEC83</td>
</tr>
<tr>
<td>Switzerland 220 V</td>
<td>SEV</td>
</tr>
<tr>
<td>Australia 240 V</td>
<td>AS C112</td>
</tr>
<tr>
<td>Universal Euro 230 V</td>
<td>CEE (7), II, IV, VII IEC83</td>
</tr>
<tr>
<td>North America 120 V</td>
<td>ANSI C73.20/NEMA 5-15-P/IEC83</td>
</tr>
<tr>
<td>United Kingdom 230 V</td>
<td>BS 1363/IEC83</td>
</tr>
</tbody>
</table>

If you are missing any of the items listed in Table 1-1, or if you have the incorrect AC power cable, contact National Instruments.

Key Features

The NI PXIe-1071 combines a 4-slot PXI Express backplane with a structural design optimized for maximum usability in a wide range of applications.

The key features of the NI PXIe-1071 chassis include the following:

- Accepts 3U PXI Express, Compact PCI Express, and hybrid slot-compatible PXI-1/CompactPCI modules
  - x4 PCI Express link directly connected to the system slot from each hybrid slot
  - 32-bit, 33 MHz PCI connected to each hybrid slot
- Accepts 4-slot wide PXI Express embedded controller
- Rugged, compact chassis with universal AC input
- Auto/high temperature-controlled fan speed based on air intake temperature to minimize audible noise
- Rack mountable
- Optional carrying handle for portability
Figures 1-1 and 1-2 show the key features of the NI PXIe-1071 chassis front and back panels. Figure 1-1 shows the front view of the NI PXIe-1071. Figure 1-2 shows the rear view of the NI PXIe-1071.
1 Rear Intake Vents
2 AC Input
3 Power Supply Fan Exhaust
4 Removable Feet
5 Chassis Ground Screw
6 AUTO/HIGH Fan Speed Selector Switch
7 Kensington Slot

Figure 1-2. Rear View of the NI PXIe-1071 Chassis
Optional Equipment

Contact National Instruments to order the following options for the NI PXIe-1071 chassis.

**EMC Filler Panels**

Optional EMC filler panel kits are available from National Instruments.

**Rack Mount Kit**

A rack mount kit option is available for mounting the NI PXIe-1071 chassis into a 19 in. instrument cabinet. Refer to Figure A-3, *NI Chassis Rack Mount Kit Components*, for more information.
Chapter 1   Getting Started

Slot Blockers
Optional slot blocker kits are available from National Instruments for improved thermal performance when all slots are not used.

Handle/Feet Kit
An optional side handle and rubber feet kit is available from National Instruments to provide a handle for portability.

NI PXIe-1071 Chassis Backplane Overview
This section provides an overview of the backplane features for the NI PXIe-1071 chassis.

Interoperability with CompactPCI
The design of the NI PXIe-1071 provides you the flexibility to use the following devices in a single PXI Express chassis:
• PXI Express compatible products
• CompactPCI Express compatible 4-Link system controller products
• CompactPCI Express compatible Type-2 peripheral products
• PXI peripheral products
• Standard CompactPCI peripheral products
Refer to Figure 1-4 for an overview of the NI PXIe-1071 architecture.

**System Controller Slot**

The system controller slot is Slot 1 of the chassis and is a 4-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. It has three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane routes three of the system slot’s x4 PCI Express (PCIe) links to peripheral slots. The fourth link is routed as a x1 to a PCI Express-to-PCI bridge, providing a 32-bit/33 MHz PCI bus to the hybrid slots. Refer to Figure 1-4 for PCI Express and PCI connectivity.
By default, the system controller will control the power supply with the PS_ON# signals. A logic low on this line will turn the power supply on.

**Note** The Inhibit Mode switch on the backplane must be in the **Default** position for the system controller to have control of the power supply. Refer to the *Inhibit Mode Switch* section of Chapter 2, *Installation and Configuration*, for details about the Inhibit Mode switch.

### Hybrid Peripheral Slots

The chassis provides three hybrid peripheral slots as defined by the *PXI-5 PXI Express Hardware Specification*: slots 2-4. A hybrid peripheral slot can accept the following peripheral modules:

- A PXI Express Peripheral with x4 or x1 PCI Express link to the system slot
- A CompactPCI Express Type-2 Peripheral with x4 or x1 PCI Express link to the system slot
- A hybrid-compatible PXI Peripheral module that has been modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2. Refer to the *PXI Express Specification* for details. The PXI Peripheral communicates through the backplane’s 32-bit PCI bus.
- A CompactPCI 32-bit peripheral on the backplane’s 32-bit PCI bus

The hybrid peripheral slots provide PXI Express functionality (excluding DSTAR and PXI Star) and 32-bit PXI functionality except for PXI Local Bus. The hybrid peripheral slot only connects to PXI Local Bus 6 left and right.

### PXI Local Bus

The PXI backplane local bus is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right.

The backplane routes PXI Local Bus 6 between adjacent PXI slots. The left Local Bus 6 from slot 1 is not routed anywhere. The right Local Bus 6 from slot 4 also is not routed anywhere.

Local bus signals may range from high-speed TTL signals to analog signals as high as 42 V.

Initialization software uses the configuration information specific to each adjacent peripheral module to evaluate local bus compatibility.
PXI Trigger Bus

All slots share eight trigger lines. You can use these trigger lines in a variety of ways. For example, you can use triggers to synchronize the operation of several different PXI peripheral modules. In other applications, one module can control carefully timed sequences of operations performed on other modules in the system. Modules can pass triggers to one another, allowing precisely timed responses to asynchronous external events the system is monitoring or controlling.

System Reference Clock

The NI PXIe-1071 chassis supplies PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 to every peripheral slot with an independent driver for each signal.

An independent buffer (having a source impedance matched to the backplane and a skew of less than 500 ps between slots) drives PXI_CLK10 to each peripheral slot. You can use this common reference clock signal to synchronize multiple modules in a measurement or control system.
An independent buffer drives PXIe_CLK100 to each peripheral slot. These clocks are matched in skew to less than 100 ps. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_CLK100 so that when there is no peripheral or a peripheral that does not connect to PXIe_CLK100, there is no clock being driven on the pair to that slot.

An independent buffer drives PXIe_SYNC100 to each peripheral slot. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_SYNC100 so that when there is no peripheral or a peripheral that does not connect to PXIe_SYNC100, there is no clock being driven on the pair to that slot.

PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 have the default timing relationship described in Figure 1-6.

![Figure 1-6. System Reference Clock Default Behavior](image-url)
This chapter describes how to prepare and operate the NI PXIe-1071 chassis.

Before connecting the chassis to a power source, read this chapter and the Read Me First: Safety and Electromagnetic Compatibility document included with your kit.

Safety Information

Caution  Before undertaking any troubleshooting, maintenance, or exploratory procedure, carefully read the following caution notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

- **Chassis Grounding**—The chassis requires a connection from the premise wire safety ground to the chassis ground. The earth safety ground must be connected during use of this equipment to minimize shock hazards. Refer to the Connecting Safety Ground section for instructions on connecting safety ground.

- **Live Circuits**—Operating personnel and service personnel must not remove protective covers when operating or servicing the chassis. Adjustments and service to internal components must be undertaken by qualified service technicians. During service of this product, the mains connector to the premise wiring must be disconnected. Dangerous voltages may be present under certain conditions; use extreme caution.

- **Explosive Atmosphere**—Do not operate the chassis in conditions where flammable gases are present. Under such conditions, this equipment is unsafe and may ignite the gases or gas fumes.
Chapter 2  Installation and Configuration

- **Part Replacement**—Only service this equipment with parts that are exact replacements, both electrically and mechanically. Contact National Instruments for replacement part information. Installation of parts with those that are not direct replacements may cause harm to personnel operating the chassis. Furthermore, damage or fire may occur if replacement parts are unsuitable.

- **Modification**—Do not modify any part of the chassis from its original condition. Unsuitable modifications may result in safety hazards.

## Chassis Cooling Considerations

The NI PXIe-1071 chassis is designed to operate on a bench or in an instrument rack. Regardless of the configuration, you must provide the cooling clearances as outlined in the following sections.

### Providing Adequate Clearance

- **Caution**  
  Failure to provide adequate clearances may result in thermal related failures in the chassis or modules.

  Apertures in the top, bottom, front, rear, and along the sides of the chassis facilitate power supply and module cooling, as shown in Figure 2-2. Air for module cooling enters through a fan intake in the bottom of the chassis. It then exits through the upper sections at the right side and top, as shown in Figure 2-1. Air for cooling the power supply enters the front and left side of the chassis and exits through the rear of the chassis, as shown in Figure 2-2.

  Place the chassis on a bench top or in an instrument rack so that the fans (air intakes) and the air outlet apertures along the right side, the top, and the back of the chassis have adequate ventilation. Provide at least 44.5 mm (1.75 in.) clearance above, behind, and on the sides of the unit for adequate venting, as shown in Figure 2-3. High-power applications may require additional clearance.
Figure 2-1. NI PXIe-1071 Module Cooling Airflow Side View
Figure 2-2. NI PXIe-1071 Vents

1. Power Supply Cooling Intake Vent
2. Module Cooling Exhaust Vent
3. Module Cooling Intake Vent
4. Backplane Cooling Intake Vent
5. Power Supply Cooling Exhaust Vent
Figure 2-3. NI PXIe-1071 Cooling Clearances
Chapter 2 Installation and Configuration

Chassis Ambient Temperature Definition
The chassis fan control system uses intake air temperature as the input for
controlling fan speeds when in Auto Fan Speed mode. Because of this, the
chassis ambient temperature is defined as the temperature that exists just
outside of the fan intake vent on the bottom of the chassis. Note that this
temperature may be higher than ambient room temperature depending on
the surrounding equipment and/or blockages present. You must ensure that
this ambient temperature does not exceed the rated ambient temperature as
stated in Appendix A, Specifications.

Setting Fan Speed
The AUTO/HIGH fan-speed selector switch is on the rear panel of the
NI PXIe-1071. Refer to Figure 1-2, Rear View of the NI PXIe-1071
Chassis, to locate the fan-speed selector switch. Select HIGH for maximum
cooling performance (recommended) or AUTO for quieter operation.
When set to AUTO, the chassis intake air temperature determines the fan
speed.

Installing Filler Panels
To maintain proper module cooling performance, install filler panels
(provided with the chassis) in unused or empty slots. Secure with the
captive mounting screws provided.

Installing Slot Blockers
You can improve the chassis cooling performance by installing optional
slot blockers. Refer to ni.com for more details.

Rack Mounting
Rack mount applications require the optional rack mount kits available
from National Instruments. Refer to the instructions supplied with the rack
mount kits to install your NI PXIe-1071 chassis in an instrument rack.
Refer to Figure A-3, NI Chassis Rack Mount Kit Components.

Note You may want to remove the feet from the NI PXIe-1071 chassis when rack
mounting. To do so, remove the screws holding the feet in place.
Connecting Safety Ground

**Caution** The NI PXIe-1071 chassis is designed with a three-position inlet that connects the cord set ground line to the chassis ground. To minimize shock hazard, make sure the electrical power outlet you use to power the chassis has an appropriate earth safety ground.

Connecting to Power Source

**Cautions** Do *not* install modules prior to performing the following power-on test.

To completely remove power, you *must* disconnect the AC power cable.

Attach input power through the rear AC inlet using the appropriate AC power cable supplied. Refer to Figure 1-2, *Rear View of the NI PXIe-1071 Chassis*, to locate the AC inlet.

Installing a PXI Express System Controller

This section contains general installation instructions for installing a PXI Express system controller in a NI PXIe-1071 chassis. Refer to your PXI Express system controller user manual for specific instructions and warnings. To install a system controller, complete the following steps:

1. Inspect the slot 1 pins on the chassis backplane for any bending or damage prior to installation.

2. Connect the AC power source to the PXI Express chassis before installing the system controller. The AC power cord grounds the chassis and protects it from electrical damage while you install the system controller.

3. Install the system controller into the system controller slot (slot 1, indicated by the red card guides) by first placing the system controller PCB into the front of the card guides (top and bottom). Slide the system controller to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-4.
4. When you begin to feel resistance, push up on the injector/ejector handle to seat the system controller fully into the chassis frame. Secure the system controller front panel to the chassis using the system controller front-panel mounting screws.

5. Connect the keyboard, mouse, and monitor to the appropriate connectors. Connect devices to ports as required by your system configuration.

6. Power on the chassis. Verify that the system controller boots. If the system controller does not boot, refer to your system controller user manual.
Figure 2-5 shows a PXI Express system controller installed in the system controller slot of a NI PXIe-1071 chassis. You can place CompactPCI, CompactPCI Express, PXI, or PXI Express modules in other slots depending on the slot type.

Figure 2-5. NI PXI Express System Controller Installed in an NI PXIe-1071 Chassis
Installing Peripheral Modules

Caution  The NI PXIe-1071 chassis accepts a variety of peripheral module types in different slots. To prevent damage to the chassis, ensure that the peripheral module is being installed into a slot designed to accept it. Refer to Chapter 1, *Getting Started*, for a description of the various slot types.

This section contains general installation instructions for installing a peripheral module in a NI PXIe-1071 chassis. Refer to your peripheral module user manual for specific instructions and warnings. To install a module, complete the following steps:

1. Inspect the slot pins on the chassis backplane for any bending or damage prior to installation.
2. Connect the AC power source to the PXI Express chassis before installing the module. The AC power cord grounds the chassis and protects it from electrical damage while you install the module.
3. Ensure that the chassis is powered off.
4. Install a module into a chassis slot by first placing the module card PCB into the front of the card guides (top and bottom), as shown in Figure 2-6. Slide the module to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-6.
5. When you begin to feel resistance, push up on the injector/ejector handle to fully seat the module into the chassis frame. Secure the module front panel to the chassis using the module front-panel mounting screws.
Power Inhibit Switch LED Indicator

The chassis power inhibit switch has an integrated LED. This LED indicates one of two conditions:

- If the inhibit switch LED is steady green (not flashing), the chassis is powered on and operating normally.
- If the inhibit switch LED is red, the system fan has failed, and the chassis has shut down to protect modules from damage due to insufficient cooling.

Figure 2-6. Installing PXI, PXI Express, or CompactPCI Peripheral Modules
Inhibit Mode Switch

On the NI PXIe-1071 backplane is a four-position DIP switch (SW1). Switch 1 of SW1 controls the chassis inhibit mode. (Refer to Figure 2-7.) In its default position (OFF), the PXI Express controller controls the power supply on/off state based on the power switch on the chassis front panel.

![Switch 1 Diagram](image)

**Figure 2-7. Switch 1 of SW1**

When switch 1 of SW1 is on, the backplane controls the power supply on/off state. This allows you to circumvent the controller and turn the chassis on or off manually. When switch 1 of SW1 is on, the power supply turns on when you press the front panel power switch. When the power supply is on, holding down the front panel power switch for about one second turns the power supply off.

⚠️ **Cautions** Be careful to avoid damaging the backplane when accessing this switch.

Suddenly removing power from an operating controller may result in loss of data and incorrect behavior on subsequent boots.
The PXI Platform Services software included with your chassis automatically identifies your PXI Express system components to generate a **pxiesys.ini** file. You can configure your entire PXI system and identify PXI-1 chassis through Measurement & Automation Explorer (MAX), included with your system controller. MAX creates the **pxiesys.ini** and **pxisys.ini** file, which define your PXI system parameters. MAX also provides an interface to route and reserve triggers so dynamic routing, through drivers such as DAQmx, avoids double-driving and potentially damaging trigger lines. For more information about routing and reserving PXI triggers, refer to KnowledgeBase 3TJDOND8 at ni.com/support.

The configuration steps for single or multiple-chassis systems are the same.
PXI-1 System Configuration

1. Launch MAX.

2. In the Configuration tree, click the Devices and Interfaces branch to expand it.

3. If the PXI system controller has not yet been configured, it is labeled PXI System (Unidentified). Right-click this entry to display the pop-up menu, then select the appropriate system controller model from the Identify As submenu.

4. Click the PXI system controller. The chassis (or multiple chassis in a multichassis configuration) is listed below it. Identify each chassis by right-clicking its entry, then selecting the appropriate chassis model through the Identify As submenu. Further expanding the PXI System branch shows all devices in the system that can be recognized by NI-VISA. When your system controller and all your chassis are identified, the required pxisys.ini file is complete.

The PXI specification allows for many combinations of PXI chassis and system modules. To assist system integrators, the manufacturers of PXI chassis and system modules must document the capabilities of their products. PXI Express devices must provide a driver and .ini file for identification. These files are provided as part of the PXI Platform Services software included with your system controller. The minimum documentation requirements for PXI-1 are contained in .ini files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these .ini files.

The capability documentation for a PXI-1 chassis is contained in a chassis.ini file provided by the chassis manufacturer. The information in this file is combined with information about the system controller to create a single PXI-1 system initialization file called pxisys.ini (PXI System Initialization). The NI system controller uses MAX to generate the pxisys.ini file from the chassis.ini file.

Device drivers and other utility software read the pxiesys.ini and pxisys.ini file to obtain system information. For detailed information about initialization files, refer to the PXI specification at www.pxisa.org.
Using System Configuration and Initialization Files

The PXI Express specification allows many combinations of PXI Express chassis and system modules. To assist system integrators, the manufacturers of PXI Express chassis and system modules must document the capabilities of their products. The minimum documentation requirements are contained in .ini files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these .ini files.

The capability documentation for the NI PXIe-1071 chassis is contained in the chassis.ini file on the software media that comes with the chassis. The information in this file is combined with information about the system controller to create a single system initialization file called pxisys.ini (PXI System Initialization). The system controller manufacturer either provides a pxisys.ini file for the particular chassis model that contains the system controller or provides a utility that can read an arbitrary chassis.ini file and generate the corresponding pxisys.ini file. System controllers from NI provide the pxisys.ini file for the NI PXIe-1071 chassis, so you should not need to use the chassis.ini file. Refer to the documentation provided with the system controller or to ni.com/support for more information on pxisys.ini and chassis.ini files.

Device drivers and other utility software read the pxisys.ini file to obtain system information. The device drivers should have no need to directly read the chassis.ini file. For detailed information regarding initialization files, refer to the PXI Express specification at www.pxisa.org.
This chapter describes basic maintenance procedures you can perform on the NI PXIe-1071 chassis.

⚠️ **Caution** Disconnect the power cable prior to servicing a NI PXIe-1071 chassis.

### Service Interval

Clean the chassis fan filter at a maximum interval of six months. Depending on the amount of use and ambient dust levels in the operating environment, the filter may require more frequent cleaning.

Clean dust from the chassis exterior (and interior) as needed, based on the operating environment. Periodic cleaning increases reliability and cooling performance.

### Preparation

The information in this section is designed for use by qualified service personnel. Read the *Read Me First: Safety and Electromagnetic Compatibility* document included with your kit before attempting any procedures in this chapter.

⚠️ **Caution** Many components within the chassis are susceptible to static discharge damage. Service the chassis only in a static-free environment. Observe standard handling precautions for static-sensitive devices while servicing the chassis. Always wear a grounded wrist strap or equivalent while servicing the chassis.
Cleaning procedures consist of exterior and interior cleaning of the chassis and cleaning the fan filter. Refer to your module user documentation for information about cleaning the individual CompactPCI or PXI Express modules.

**Caution** Always disconnect the AC power cable before cleaning or servicing the chassis.

### Interior Cleaning

Use a dry, low-velocity stream of air to clean the interior of the chassis. Use a soft-bristle brush for cleaning around components.

### Exterior Cleaning

Clean the exterior surfaces of the chassis with a dry lint-free cloth or a soft-bristle brush. If any dirt remains, wipe with a cloth moistened in a mild soap solution. Remove any soap residue by wiping with a cloth moistened with clear water. Do not use abrasive compounds on any part of the chassis.

**Cautions** Avoid getting moisture inside the chassis during exterior cleaning, especially through the top vents. Use just enough moisture to dampen the cloth.

Do not wash the front- or rear-panel connectors or switches. Cover these components while cleaning the chassis.

Do not use harsh chemical cleaning agents; they may damage the chassis. Avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.
Specifications

This appendix contains specifications for the NI PXIe-1071 chassis.

⚠️ Caution Specifications are subject to change without notice.

Electrical

**AC Input**

- Input voltage range: 100 to 240 VAC
- Operating voltage range: 90 to 264 VAC
- Input frequency: 50/60 Hz
- Operating frequency range: 47 to 63 Hz
- Input current rating: 4-2 A

**Line regulation**

- 3.3 V: <±0.2%
- 5 V: <±0.1%
- ±12 V: <±0.1%

**Efficiency**: 70% typical

**Power disconnect**: The AC power cable provides main power disconnect.

---

1 The operating range is guaranteed by design.
Appendix A Specifications

DC Output

DC current capacity (I_{MP})

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Maximum Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3.3 V</td>
<td>18 A</td>
</tr>
<tr>
<td>+5 V</td>
<td>17 A</td>
</tr>
<tr>
<td>+12 V</td>
<td>17 A</td>
</tr>
<tr>
<td>-12 V</td>
<td>1 A</td>
</tr>
<tr>
<td>5 V_{AUX}</td>
<td>0.75 A</td>
</tr>
</tbody>
</table>

Notes
- Maximum total usable power is 230 W.
- The maximum combined power available on +3.3 V and +5 V is 125 W.
- The maximum combined power available on +3.3 V and +5 V derates linearly to 100 W from 45 °C to 50 °C operating ambient temperature range.
- The -12 V regulation is ± 5% for loads of 8 A or less on the +12 V rail.

Backplane slot current capacity

<table>
<thead>
<tr>
<th>Slot</th>
<th>+5 V</th>
<th>V (I/O)</th>
<th>+3.3 V</th>
<th>+12 V</th>
<th>-12 V</th>
<th>5 V_{AUX}</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Controller Slot</td>
<td>15 A</td>
<td>—</td>
<td>15 A</td>
<td>30 A</td>
<td>—</td>
<td>1 A</td>
</tr>
<tr>
<td>Hybrid Peripheral Slot with PXI-1 Peripheral</td>
<td>6 A</td>
<td>5 A</td>
<td>6 A</td>
<td>1 A</td>
<td>1 A</td>
<td>—</td>
</tr>
<tr>
<td>Hybrid Peripheral Slot with PXI-5 Peripheral</td>
<td>—</td>
<td>—</td>
<td>6 A</td>
<td>4 A</td>
<td>—</td>
<td>1 A</td>
</tr>
</tbody>
</table>

Notes
- Total system slot current should not exceed 45 A.
- PCI V(I/O) pins in PXI-1 peripheral slots and hybrid peripheral slots are connected to +5 V.
- The maximum power dissipated in the system slot should not exceed 140 W.
- The maximum power dissipated in a peripheral slot should not exceed 38.25 W.
Chassis Cooling

Per slot cooling capacity ....................... 38.25 W
Module cooling system ......................... Forced air circulation
(positive pressurization)
through a 150 CFM fan with
High/Auto speed selector
Slot airflow direction ......................... Bottom of module to top of module
Module cooling intake ......................... Bottom of chassis
Module cooling exhaust ....................... Right side, rear, and top of chassis
Power supply cooling system ............... Forced air circulation through
integrated fan
Power supply cooling intake ............... Front and left side of chassis
Power supply cooling exhaust ............ Rear of chassis

Environmental

Maximum altitude ......................... 2,000 m (800 mbar)
(at 25 °C ambient)
Measurement Category .................. II
Pollution Degree ......................... 2
For indoor use only.

Operating Environment

Ambient temperature range ............... 0 to 50 °C
(Tested in accordance with
IEC-60068-2-1 and
IEC-60068-2-2. Meets
MIL-PRF-28800F Class 3
low temperature limit and
MIL-PRF-28800F Class 2
high temperature limit.)
Relative humidity range .................. 20 to 80%, noncondensing
(Tested in accordance with
IEC-60068-2-56.)
Appendix A Specifications

Storage Environment

Ambient temperature range .................-40 to 71 °C
(Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)

Relative humidity range.......................5 to 95%, noncondensing
(Tested in accordance with IEC-60068-2-56.)

Shock and Vibration

Operational shock ................................30 g peak, half-sine, 11 ms pulse
(Tested in accordance with IEC-60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

Random Vibration

Operating .....................................5 to 500 Hz, 0.3 g_{rms}
Nonoperating .................................5 to 500 Hz, 2.4 g_{rms}
(Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Acoustic Emissions

Sound Pressure Level (at Operator Position)

Tested in accordance with ISO 7779. Meets MIL-PRF-28800F requirements.

Auto fan (up to ~30 °C ambient).............48.4 dBA
High fan ......................................61.9 dBA

Sound Power

Auto fan (up to ~30 °C ambient).............59.9 dBA
High fan ......................................68.7 dBA

Note Specifications are subject to change without notice.
Appendix A Specifications

Safety

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note: For UL and other safety certifications, refer to the product label or the Online Product Certification section.

Electromagnetic Compatibility

This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note: For the standards applied to assess the EMC of this product, refer to the Online Product Certification section.

Note: For EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.
Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the Minimize Our Environmental Impact web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。 (For information about China RoHS compliance, go to ni.com/environment/rohs_china)

Backplane

Size .........................................................3U-sized; one system slot (with three system expansion slots) and three peripheral slots. Compliant with IEEE 1101.10 mechanical packaging. PXI Express Specification compliant. Accepts both PXI Express and CompactPCI (PICMG 2.0 R 3.0) 3U modules.

Backplane bare-board material ...............UL 94 V-0 Recognized

Backplane connectors .........................Conforms to IEC 917 and IEC 1076-4-101, and are UL 94 V-0 rated
System Synchronization Clocks
(PXI_CLK10, PXIe_CLK100, PXIe_SYNC100)

10 MHz System Reference Clock: PXI_CLK10

Maximum slot-to-slot skew ................. 500 ps

Accuracy ............................................... ±25 ppm max (guaranteed over the operating temperature range)

Maximum jitter ............................... 5 ps RMS phase-jitter (10 Hz-1 MHz range)

Duty-factor ...................................... 45%-55%

Unloaded signal swing ....................... 3.3 V ±0.3 V

Note For other specifications refer to the PXI-1 Hardware Specification.

100 MHz System Reference Clock: PXIe_CLK100 and PXIe-SYNC100

Maximum slot-to-slot skew ................. 100 ps

Accuracy ............................................... ±25 ppm max (guaranteed over the operating temperature range)

Maximum jitter ............................... 3 ps RMS phase-jitter (10 Hz-12 kHz range) 2 ps RMS phase-jitter (12 kHz-20 MHz range)

Duty-factor for PXIe_CLK100 .............. 45%-55%

Absolute differential voltage
(When terminated with a 50 Ω load to 1.30 V or Thévenin equivalent) ........ 400-1000 mV

Note For other specifications refer to the PXI-5 PXI Express Hardware Specification.

DMA Support

For more information about this chassis’ support of hardware modules with 64-bit DMA and/or 32-bit DMA with PAE mode, please visit ni.com/info and enter the Info Code PXI64HANG.
Appendix A Specifications

Mechanical

Overall dimensions

Standard chassis

Height ....................................... 6.97 in. (177 mm)
Width ....................................... 10.12 in. (257 mm)
Depth ....................................... 8.43 in. (214.2 mm)

Note 0.5 in. (12.7 mm) is added to height when feet are installed.

Weight .................................................... 13.1 lb (5.94 kg)

Chassis materials .................................... Stainless Steel, Extruded Aluminum, Cold Rolled Steel, and PC-ABS

Finish ...................................................... Conductive Clear Iridite on Aluminum, Clear Chromate Zinc Plating on Cold Rolled Steel, Polyurethane Enamel, and Polyester Urethane Powder Paint

Figures A-1 and A-2 show the NI PXIe-1071 chassis dimensions. The holes shown are for the installation of the optional rack mount kits. Notice that the front and rear chassis mounting holes (size M4) are symmetrical.
Figure A-1. NI PXIe-1071 Chassis Dimensions (Front and Side)
Figure A-2. NI PXIe-1071 Chassis Dimensions (Bottom)
Figure A-3 shows the chassis rack mount kit components.

1 Front Rack Mount Kit  
2 NI Chassis

**Figure A-3.** NI Chassis Rack Mount Kit Components
This appendix describes the connector pinouts for the NI PXIe-1071 chassis backplane.

Table B-1 shows the XP1 connector pinout for the System Controller slot.
Table B-2 shows the XP2 Connector Pinout for the System Controller slot.
Table B-3 shows the XP3 Connector Pinout for the System Controller slot.
Table B-4 shows the XP4 Connector Pinout for the System Controller slot.
Table B-5 shows the P1 connector pinout for the Hybrid peripheral slots.
Table B-6 shows the XP3 Connector Pinout for the Hybrid peripheral slots.
Table B-7 shows the XP4 Connector Pinout for the Hybrid peripheral slots.

For more detailed information, refer to the PXI-5 PXI Express Hardware Specification, Revision 2.0. Contact the PXI Systems Alliance for a copy of the specification.
## System Controller Slot Pinouts

### Table B-1. XP1 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pins</th>
<th>Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>GND</td>
</tr>
<tr>
<td>B</td>
<td>3.3V</td>
</tr>
<tr>
<td>C</td>
<td>5V</td>
</tr>
<tr>
<td>D</td>
<td>GND</td>
</tr>
<tr>
<td>E</td>
<td>12V</td>
</tr>
<tr>
<td>F</td>
<td>12V</td>
</tr>
<tr>
<td>G</td>
<td>GND</td>
</tr>
</tbody>
</table>

### Table B-2. XP2 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>cd</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3PETp1</td>
<td>3PETn1</td>
<td>GND</td>
<td>3PERp1</td>
<td>3PERn1</td>
<td>GND</td>
<td>3PETp2</td>
<td>3PETn2</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>3PETp3</td>
<td>3PETn3</td>
<td>GND</td>
<td>3PERp3</td>
<td>3PERn3</td>
<td>GND</td>
<td>3PETp2</td>
<td>3PERn2</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>4PETp0</td>
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<td>4PERp0</td>
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<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>4PETp2</td>
<td>4PETn2</td>
<td>GND</td>
<td>4PERp2</td>
<td>4PERn2</td>
<td>GND</td>
<td>4PETp1</td>
<td>4PERn1</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>4PETp3</td>
<td>4PETn3</td>
<td>GND</td>
<td>4PERp3</td>
<td>4PERn3</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
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<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
</tbody>
</table>
## Table B-3. XP3 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
</tr>
<tr>
<td>2</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>PWR_OK</td>
<td>PS_ON#</td>
<td>GND</td>
<td>LINKCAP</td>
<td>PWRBTN#</td>
</tr>
<tr>
<td>3</td>
<td>SMBDAT</td>
<td>SMBCLK</td>
<td>GND</td>
<td>4RefClk+</td>
<td>4RefClk-</td>
<td>GND</td>
<td>2RefClk+</td>
<td>2RefClk-</td>
</tr>
<tr>
<td>4</td>
<td>RSV</td>
<td>PERST#</td>
<td>GND</td>
<td>3RefClk+</td>
<td>3RefClk-</td>
<td>GND</td>
<td>1RefClk+</td>
<td>1RefClk-</td>
</tr>
<tr>
<td>5</td>
<td>1PETp0</td>
<td>1PETn0</td>
<td>GND</td>
<td>1PERp0</td>
<td>1PERn0</td>
<td>GND</td>
<td>1PETp1</td>
<td>1PETn1</td>
</tr>
<tr>
<td>6</td>
<td>1PETp2</td>
<td>1PETn2</td>
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<td>9</td>
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<td>2PETn2</td>
<td>GND</td>
<td>2PERp2</td>
<td>2PERn2</td>
<td>GND</td>
<td>2PETp3</td>
<td>2PETn3</td>
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<tr>
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<td>3PERn0</td>
<td>GND</td>
<td>2PERp3</td>
<td>2PERn3</td>
</tr>
</tbody>
</table>

## Table B-4. XP4 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>GA4</td>
<td>GA3</td>
<td>GA2</td>
<td>GA1</td>
<td>GA0</td>
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<tr>
<td>2</td>
<td>GND</td>
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<td>GND</td>
<td>SYSEN#</td>
<td>WAKE#</td>
<td>ALERT#</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
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<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>PXI_TRIG3</td>
<td>PXI_TRIG4</td>
<td>PXI_TRIG5</td>
<td>GND</td>
<td>PXI_TRIG6</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>PXI_TRIG2</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_STAR</td>
<td>PXI_CLK10</td>
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</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>PXI_TRIG1</td>
<td>PXI_TRIG0</td>
<td>RSV</td>
<td>GND</td>
<td>PXI_TRIG7</td>
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</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>PXI_LBR6</td>
<td>GND</td>
</tr>
</tbody>
</table>
### Hybrid Slot Pinouts

#### Table B-5. P1 Connector Pinout for the Hybrid Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>GND</td>
<td>5V</td>
<td>REQ64#</td>
<td>ENUM#</td>
<td>3.3V</td>
<td>5V</td>
<td>GND</td>
</tr>
<tr>
<td>24</td>
<td>GND</td>
<td>AD[1]</td>
<td>5V</td>
<td>V(I/O)</td>
<td>AD[0]</td>
<td>ACK64#</td>
<td>GND</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>SERR#</td>
<td>GND</td>
<td>3.3V</td>
<td>PAR</td>
<td>C/BE[1]#</td>
<td>GND</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>3.3V</td>
<td>IPMB_SCL</td>
<td>IPMB_SDA</td>
<td>GND</td>
<td>PERR#</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>DEVSEL#</td>
<td>GND</td>
<td>V(I/O)</td>
<td>STOP#</td>
<td>LOCK#</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>3.3V</td>
<td>FRAME#</td>
<td>IRDY#</td>
<td>BD_SEL#</td>
<td>TRDY#</td>
<td>GND</td>
</tr>
<tr>
<td>14-12</td>
<td></td>
<td>Key Area</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>C/BE[3]#</td>
<td>IDSEL</td>
<td>AD[23]</td>
<td>GND</td>
<td>AD[22]</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>REQ#</td>
<td>GND</td>
<td>3.3V</td>
<td>CLK</td>
<td>AD[31]</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>BRSVPA5</td>
<td>BRSVPB5</td>
<td>RST#</td>
<td>GND</td>
<td>GNT#</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>IPMB_PWR</td>
<td>HEALTHY#</td>
<td>V(I/O)</td>
<td>INTP</td>
<td>INTS</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>INTA#</td>
<td>INTB#</td>
<td>INTC#</td>
<td>5V</td>
<td>INTD#</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>TCK</td>
<td>5V</td>
<td>TMS</td>
<td>TDO</td>
<td>TDI</td>
<td>GND</td>
</tr>
<tr>
<td>1</td>
<td>GND</td>
<td>5V</td>
<td>-12V</td>
<td>TRST#</td>
<td>+12V</td>
<td>5V</td>
<td>GND</td>
</tr>
</tbody>
</table>
### Table B-6. XP3 Connector Pinout for the Hybrid Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>cd</th>
<th>E</th>
<th>F</th>
<th>of</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PXIe_CLK100+</td>
<td>PXIe_CLK100-</td>
<td></td>
<td>GND</td>
<td>PXIe_SYNC100+</td>
<td></td>
<td>PXIe_SYNC100-</td>
<td>PXIe_DSTARC+</td>
<td>PXIe_DSTARC-</td>
</tr>
<tr>
<td>2</td>
<td>PRSNT#</td>
<td>PWREN#</td>
<td></td>
<td>PXIe_DSTARB+</td>
<td>PXIe_DSTARB-</td>
<td></td>
<td>PXIe_DSTARA+</td>
<td>PXIe_DSTARA-</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>SMBDAT</td>
<td>SMBCLK</td>
<td></td>
<td>RSV</td>
<td>RSV</td>
<td></td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>MPWRGD*</td>
<td>PERST#</td>
<td></td>
<td>RSV</td>
<td>RSV</td>
<td></td>
<td>PXIe_DSTARB+</td>
<td>PXIe_DSTARB-</td>
<td>PXIe_DSTARA-</td>
</tr>
<tr>
<td>5</td>
<td>IPE[Tp0]</td>
<td>IPE[Tn0]</td>
<td></td>
<td>PXIe_DSTARA+</td>
<td>PXIe_DSTARA-</td>
<td></td>
<td>PXIe_DSTARC+</td>
<td>PXIe_DSTARC-</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>IPE[Tp2]</td>
<td>IPE[Tn2]</td>
<td></td>
<td>PXIe_DSTARA+</td>
<td>PXIe_DSTARA-</td>
<td></td>
<td>PXIe_DSTARC+</td>
<td>PXIe_DSTARC-</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>IPE[Tp1]</td>
<td>IPE[Tx3]</td>
<td></td>
<td>PXIe_DSTARA+</td>
<td>PXIe_DSTARA-</td>
<td></td>
<td>PXIe_DSTARC+</td>
<td>PXIe_DSTARC-</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>IPE[Tp1]</td>
<td>IPE[Tx5]</td>
<td></td>
<td>PXIe_DSTARA+</td>
<td>PXIe_DSTARA-</td>
<td></td>
<td>PXIe_DSTARC+</td>
<td>PXIe_DSTARC-</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>RSV</td>
<td>RSV</td>
<td></td>
<td>RSV</td>
<td>RSV</td>
<td></td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
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### Table B-7. XP4 Connector Pinout for the Hybrid Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>GA4</td>
<td>GA3</td>
<td>GA2</td>
<td>GA1</td>
<td>GA0</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>5Vaux</td>
<td>GND</td>
<td>SYSSEN#</td>
<td>WAKE#</td>
<td>ALERT#</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>12V</td>
<td>12V</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>GND</td>
<td>3.3V</td>
<td>3.3V</td>
<td>3.3V</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>PXI_TRIG3</td>
<td>PXI_TRIG4</td>
<td>PXI_TRIG5</td>
<td>PXI_TRIG6</td>
<td>PXI_TRIG7</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>PXI_TRIG2</td>
<td>GND</td>
<td>ATNLED</td>
<td>PXI_STAR</td>
<td>PXI_CLK10</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>PXI_TRIG1</td>
<td>PXI_TRIG0</td>
<td>ATNSW#</td>
<td>GND</td>
<td>PXI_CLK7</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_LBL6</td>
<td>PXI_LBR6</td>
<td>GND</td>
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Glossary

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Prefix</th>
<th>Value</th>
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<tr>
<td>p</td>
<td>pico</td>
<td>$10^{-12}$</td>
</tr>
<tr>
<td>n</td>
<td>nano</td>
<td>$10^{-9}$</td>
</tr>
<tr>
<td>µ</td>
<td>micro</td>
<td>$10^{-6}$</td>
</tr>
<tr>
<td>m</td>
<td>milli</td>
<td>$10^{-3}$</td>
</tr>
<tr>
<td>k</td>
<td>kilo</td>
<td>$10^3$</td>
</tr>
<tr>
<td>M</td>
<td>mega</td>
<td>$10^6$</td>
</tr>
<tr>
<td>G</td>
<td>giga</td>
<td>$10^9$</td>
</tr>
<tr>
<td>T</td>
<td>tera</td>
<td>$10^{12}$</td>
</tr>
</tbody>
</table>

Symbols

° Degrees.
≥ Equal or greater than.
≤ Equal or less than.
% Percent.

A

A Amperes.
AC Alternating current.
ANSI American National Standards Institute.
Auto Automatic fan speed control.
AWG American Wire Gauge.
### Glossary

#### B
- **backplane**: An assembly, typically a printed circuit board, with connectors and signal paths that bus the connector pins.
- **BNC**: Bayonet Neill Concelman connector; a commonly used coaxial connector.

#### C
- **C**: Celsius.
- **CFM**: Cubic feet per minute.
- **cm**: Centimeters.
- **CompactPCI**: An adaptation of the Peripheral Component Interconnect (PCI) Specification 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. It uses industry standard mechanical components and high-performance connector technologies to provide an optimized system intended for rugged applications. It is electrically compatible with the PCI Specification, which enables low-cost PCI components to be utilized in a mechanical form factor suited for rugged environments.
- **CSA**: Canadian Standards Association.

#### D
- **daisy-chain**: A method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus.
- **DB-9**: A 9-pin D-SUB connector.
- **DC**: Direct current.
- **DoC**: Declaration of Conformity.
- **D-SUB**: Subminiature D connector.
<table>
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<td><strong>E</strong></td>
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<td>efficiency</td>
</tr>
<tr>
<td>EIA</td>
</tr>
<tr>
<td>EMC</td>
</tr>
<tr>
<td>EMI</td>
</tr>
<tr>
<td><strong>F</strong></td>
</tr>
<tr>
<td>FCC</td>
</tr>
<tr>
<td>filler panel</td>
</tr>
<tr>
<td><strong>G</strong></td>
</tr>
<tr>
<td>g</td>
</tr>
<tr>
<td>GPIB</td>
</tr>
<tr>
<td>$g_{RMS}$</td>
</tr>
<tr>
<td><strong>H</strong></td>
</tr>
<tr>
<td>hr</td>
</tr>
<tr>
<td>Hz</td>
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<tr>
<td>IEC</td>
</tr>
<tr>
<td>IEEE</td>
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<tr>
<td>$I_{MP}$</td>
</tr>
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</table>
Glossary

in. Inches.
inhibit To turn off.

J
jitter A measure of the small, rapid variations in clock transition times from their nominal regular intervals. Units: seconds RMS.

K
kg Kilograms.
km Kilometers.

L
lb Pounds.
LED Light emitting diode.
line regulation The maximum steady-state percentage that a DC voltage output will change as a result of a specified change in input AC voltage (step change from 90 to 132 VAC or 180 to 264 VAC).
load regulation The maximum steady-state percentage that a DC voltage output will change as a result of a step change from no-load to full-load output current.

M
m Meters.
MHz Megahertz. One million Hertz; one Hertz equals one cycle per second.
mi Miles.
ms Milliseconds.
MTBF Mean time between failure.
MTTR Mean time to repair.
Glossary

N
NEMA National Electrical Manufacturers Association.
NI National Instruments.

P
power supply shuttle A removable module that contains the chassis power supply.
PXI PCI eXtensions for Instrumentation.
PXI_CLK10 10 MHz PXI system reference clock.

R
RH Relative humidity.
RMS Root mean square.

S
s Seconds.
skew Deviation in signal transmission times.
slot blocker An assembly installed into an empty slot to improve the airflow in adjacent slots.
standby The backplane is unpowered (off), but the chassis is still connected to AC power mains.
System controller A module configured for installation in Slot 1 of a PXI chassis. This device is unique in the PXI system in that it performs the system controller functions, including clock sourcing and arbitration for data transfers across the backplane. Installing such a device into any other slot can damage the device, the PXI backplane, or both.
### Glossary

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>system reference clock</td>
<td>A 10 MHz clock, also called PXI_CLK10, that is distributed to all peripheral slots in the chassis, as well as a BNC connector on the rear of chassis labeled 10 MHz REF OUT. The system reference clock can be used for synchronization of multiple modules in a measurement or control system. The 10 MHz REF IN and OUT BNC connectors on the rear of the chassis can be used to synchronize multiple chassis to one reference clock. The PXI backplane specification defines implementation guidelines for PXI_CLK10.</td>
</tr>
<tr>
<td>System Timing slot</td>
<td>This slot is located at slot 4 and has dedicated trigger lines to other slots.</td>
</tr>
<tr>
<td><strong>T</strong></td>
<td></td>
</tr>
<tr>
<td>TTL</td>
<td>Transistor-transistor logic.</td>
</tr>
<tr>
<td><strong>U</strong></td>
<td></td>
</tr>
<tr>
<td>UL</td>
<td>Underwriter’s Laboratories.</td>
</tr>
<tr>
<td><strong>V</strong></td>
<td></td>
</tr>
<tr>
<td>V</td>
<td>Volts.</td>
</tr>
<tr>
<td>VAC</td>
<td>Volts alternating current.</td>
</tr>
<tr>
<td>V&lt;sub&gt;pp&lt;/sub&gt;</td>
<td>Peak-to-peak voltage.</td>
</tr>
<tr>
<td><strong>W</strong></td>
<td></td>
</tr>
<tr>
<td>W</td>
<td>Watts.</td>
</tr>
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</table>
Index

A
AC power cables (table), 1-2

B
backplane
  hybrid peripheral slots, 1-8
  interoperability with CompactPCI, 1-6
  overview, 1-6
  PXI local bus, routing, 1-8
  specifications, A-6
  system controller slot, 1-7
  system reference clock, 1-9
    default behavior (figure), 1-10
  trigger bus, 1-9

C
cables, power (table), 1-2
  calibration certificate (NI resources), C-2
  CE compliance, specifications, A-5
  chassis ambient temperature definitions, 2-6
  chassis cooling considerations
    ambient temperature definitions, 2-6
    clearances, 2-2
    figure, 2-5
    vents (figure), 2-4
  chassis initialization file, 2-15
  chassis ventilation (figure), 2-4
  cleaning fan filter, 3-1
  clearances for chassis cooling, 2-2
    figure, 2-5
CompactPCI
  interoperability with NI PXIe-1071
    backplane, 1-6
  configuration in MAX (figure), 2-13

cooling
  air cooling of NI PXIe-1071, 2-2
  air intake (figure), 2-3
  filler panel installation, 2-6
  setting fan speed, 2-6
  slot blocker installation, 2-6

D
  Declaration of Conformity (NI resources), C-2
  diagnostic tools (NI resources), C-1
  dimensions (figure), A-9, A-10
  DMA support, A-7
  documentation
    NI resources, C-1
    related documentation, ix
  drivers (NI resources), C-1

E
electromagnetic compatibility, A-5
  EMC filler panel kit, 1-5
  environmental management, specifications
    WEEE information, A-6
  examples (NI resources), C-1

F
  fan, setting speed, 2-6
  filler panel installation, 2-6

G
  ground, connecting, 2-7
Index

H
handle/feet kit, 1-6
help, technical support, C-1
hybrid peripheral slots, description, 1-8
hybrid slot pinouts
  P1 connector (table), B-4
  XP3 connector (table), B-5
  XP4 connector (table), B-5

I
IEC 320 inlet, 1-4, 2-7
inhibit mode switch, 2-12
installation, configuration, and operation
  chassis initialization file, 2-15
  configuration in MAX (figure), 2-13
  connecting safety ground, 2-7
  filler panel installation, 2-6
  installing a PXI Express system
    controller, 2-7
      figure, 2-8
  module installation
    CompactPCI or PXI modules
      (figure), 2-11
  peripheral module installation, 2-10
      figure, 2-11
  PXI Express configuration in MAX, 2-13
  PXI Express system controller installed in
    a NI PXIe-1071 chassis (figure), 2-9
  PXI-1 configuration in MAX, 2-14
  rack mounting, 2-6
  setting fan speed, 2-6
  site considerations, 2-2
  slot blocker installation, 2-6
  testing power up, 2-7
  unpacking the NI PXIe-1071, 1-1
  installing a PXI Express system controller
      (figure), 2-8
  instrument drivers (NI resources), C-1
  interoperability with CompactPCI, 1-6

K
key features, 1-2
kit contents, 1-1
KnowledgeBase, C-1

M
maintenance of NI PXIe-1071 chassis, 3-1
  cleaning
    exterior cleaning, 3-2
    interior cleaning, 3-2
  preparation, 3-1
  service interval, 3-1
  static discharge damage (caution), 3-1

N
National Instruments support and
services, C-1
NI PXIe-1071
  fan speed, setting, 2-6
  front view (figure), 1-3
  installation. See installation,
    configuration, and operation
  key features, 1-2
  maintenance. See maintenance of
    NI PXIe-1071 chassis
  module cooling air intake (figure), 2-3
  optional equipment, 1-5
  rack mounting, 2-6
  rear view of NI PXIe-1071 chassis, 1-4
  safety ground, connecting, 2-7
  unpacking, 1-1
NI PXIe-1071 backplane
  hybrid peripheral slots, 1-8
  interoperability with CompactPCI, 1-6
  overview, 1-6
  PXI local bus, routing, 1-8
  specifications, A-6
  system controller slot, 1-7
Index

system reference clock, 1-9
  default behavior (figure), 1-10
  trigger bus, 1-9

O
  optional equipment, 1-5

P
  peripheral module installation, figure, 2-11
  pinouts, B-1
  power cables (table), 1-2
  power inhibit switch LED indicator, 2-11
  power supply, connecting to, 2-7
  power up, testing, 2-7
  programming examples (NI resources), C-1
  PXI Express configuration in MAX, 2-13
  PXI Express system controller, 2-7
    figure, 2-8
    installing in a NI PXIe-1071 chassis (figure), 2-9
  PXI local bus, routing, 1-8
  PXI trigger bus, routing (figure), 1-9
  PXI-1 configuration in MAX, 2-14

R
  rack mount kit dimensions (figure), A-11
  rack mounting, 2-6
    kit, 1-5
  recycling hardware, A-6
  related documentation, ix

S
  safety and caution notices, 2-1
  safety ground, connecting, 2-7
  safety specifications, A-5
  service interval, 3-1
  setting fan speed, 2-6
  slot blocker
    installation, 2-6
    kit, 1-6
  software (NI resources), C-1
  specifications
    acoustic emissions
      sound power, A-4
      sound pressure level (at operator position), A-4
    backplane
      10 MHz system reference clock (PXI_CLK10), A-7
      100 MHz system reference clock (PXIe_CLK100 and PXIe_SYNC100), A-7
    CE compliance, A-5
    chassis cooling, A-3
    dimensions (figure), A-9, A-10
    electrical
      AC input, A-1
      DC output, A-2
    electromagnetic compatibility, A-5
    environmental
      operating environment, A-3
      storage environment, A-4
    WEEE information, A-6
    mechanical, A-8
    online product certification, A-5
    rack mount kit dimensions (figure), A-11
    safety, A-5
    shock and vibration, A-4
    system reference clocks, A-7
    static discharge damage (caution), 3-1
    support, technical, C-1
    system controller slot
      description, 1-7
      pinouts
        XP1 connector (table), B-2
        XP2 connector (table), B-2
        XP3 connector (table), B-3
        XP4 connector (table), B-3
Index

system reference clock, 1-9
  default behavior (figure), 1-10
  specifications, A-7

T
  technical support, C-1
  testing power up, 2-7
  training and certification (NI resources), C-1
  trigger bus, 1-9
  troubleshooting (NI resources), C-1

U
  unpacking the NI PXIe-1071 chassis, 1-1

W
  Web resources, C-1
  WEEE information, A-6