Worldwide Technical Support and Product Information

ni.com

Worldwide Offices
Visit ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

National Instruments Corporate Headquarters
11500 North Mopac Expressway  Austin, Texas 78759-3504  USA  Tel: 512 683 0100

For further support information, refer to the Technical Support and Professional Services appendix. To comment on National Instruments documentation, refer to the National Instruments Web site at ni.com/info and enter the Info Code feedback.

© 2006–2012 National Instruments. All rights reserved.
Important Information

Warranty
The NI PXIe-1062Q is warranted against defects in materials and workmanship for a period of one year from the date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace equipment that proves to be defective during the warranty period. This warranty includes parts and labor.

The media on which you receive National Instruments software are warranted not to fail to execute programming instructions, due to defects in materials and workmanship, for a period of 90 days from date of shipment, as evidenced by receipts or other documentation. National Instruments will, at its option, repair or replace software media that do not execute programming instructions if National Instruments receives notice of such defects during the warranty period. National Instruments does not warrant that the operation of the software shall be uninterrupted or error free.

A Return Material Authorization (RMA) number must be obtained from the factory and clearly marked on the outside of the package before any equipment will be accepted for warranty work. National Instruments will pay the shipping costs of returning to the owner parts which are covered by warranty.

National Instruments believes that the information in this document is accurate. The document has been carefully reviewed for technical accuracy. In the event that technical or typographical errors exist, National Instruments reserves the right to make changes to subsequent editions of this document without prior notice to holders of this edition. The reader should consult National Instruments if errors are suspected. In no event shall National Instruments be liable for any damages arising out of or related to this document or the information contained in it.

EXCEPT AS SPECIFIED HEREIN, NATIONAL INSTRUMENTS MAKES NO WARRANTIES, EXPRESS OR IMPLIED, AND SPECIFICALLY DISCLAIMS ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. CUSTOMER’S RIGHT TO RECOVER DAMAGES CAUSED BY FAULT OR NEGLIGENCE ON THE PART OF NATIONAL INSTRUMENTS SHALL BE LIMITED TO THE AMOUNT THEREFORE PAID BY THE CUSTOMER. NATIONAL INSTRUMENTS WILL NOT BE LIABLE FOR DAMAGES RESULTING FROM LOSS OF DATA, PROFITS, USE OF PRODUCTS, OR INCIDENTAL OR CONSEQUENTIAL DAMAGES, EVEN IF ADVISED OF THE POSSIBILITY THEREOF. This limitation of the liability of National Instruments will apply regardless of the form of action, whether in contract or tort, including negligence. Any action against National Instruments must be brought within one year after the cause of action accrues. National Instruments shall not be liable for any delay in performance due to causes beyond its reasonable control. The warranty provided herein does not cover damages, defects, malfunctions, or service due to causes beyond its reasonable control.

Copyright
Under the copyright laws, this publication may not be reproduced or transmitted in any form, electronic or mechanical, including photocopying, recording, storing in an information retrieval system, or translating, in whole or in part, without the prior written consent of National Instruments Corporation.

National Instruments respects the intellectual property of others, and we ask our users to do the same. NI software is protected by copyright and other intellectual property laws. Where NI software may be used to reproduce software or other materials belonging to others, you may use NI software only to reproduce materials that you may reproduce in accordance with the terms of any applicable license or other legal restriction.

End-User License Agreements and Third-Party Legal Notices
You can find end-user license agreements (EULAs) and third-party legal notices in the following locations:

- Notices are located in the `<National Instruments>\_Legal Information` and `<National Instruments>\_Shared\MDF\EULAs` directories.
- EULAs are located in the `<National Instruments>\_Legal Information\_Legal Information.txt` for more information on including legal information in installers built with NI products.

Trademarks
LabVIEW, National Instruments, NI, ni.com, the National Instruments corporate logo, and the Eagle logo are trademarks of National Instruments Corporation. Refer to the `Trademark Information at ni.com/trademarks` for other National Instruments trademarks.

Other product and company names mentioned herein are trademarks or trade names of their respective companies.

Members of the National Instruments Alliance Partner Program are business entities independent from National Instruments and have no agency, partnership, or joint-venture relationship with National Instruments.

Patents
For patents covering National Instruments products/technology, refer to the appropriate location: Help\Patents in your software, the patents.txt file on your media, or the National Instruments Patent Notice at ni.com/patents.

Export Compliance Information
Refer to the Export Compliance Information at `ni.com/legal/export-compliance` for the National Instruments global trade compliance policy and how to obtain relevant HTS codes, ECCNs, and other import/export data.

WARNING REGARDING USE OF NATIONAL INSTRUMENTS PRODUCTS

(1) NATIONAL INSTRUMENTS PRODUCTS ARE NOT DESIGNED WITH COMPONENTS AND TESTING FOR A LEVEL OF RELIABILITY SUITABLE FOR USE IN OR IN CONNECTION WITH SURGICAL IMPLANTS OR AS CRITICAL COMPONENTS IN ANY LIFE SUPPORT SYSTEMS WHOSE FAILURE TO PERFORM CAN REASONABLY BE EXPECTED TO CAUSE SIGNIFICANT HARM TO A HUMAN.

(2) IN ANY APPLICATION, INCLUDING THE ABOVE, RELIABILITY OF OPERATION OF THE SOFTWARE PRODUCTS CAN BE IMPAIRED BY ADVERSE FACTORS, INCLUDING BUT NOT LIMITED TO FLUCTUATIONS IN ELECTRICAL POWER SUPPLY, COMPUTER HARDWARE MALFUNCTIONS, COMPUTER OPERATING SYSTEM SOFTWARE, FITNESS, AND DEVELOPMENT SOFTWARE USED TO DEVELOP AN APPLICATION, INSTALLATION ERRORS, SOFTWARE AND HARDWARE COMPATIBILITY PROBLEMS, MALFUNCTIONS OR FAILURES OF ELECTRONIC MONITORING OR CONTROL DEVICES, TRANSMISSION ERRORS OF ELECTRONIC SYSTEMS (HARDWARE AND/OR SOFTWARE), UNANTICIPATED USES OR MISUSES, OR ERRORS ON THE PART OF THE USER OR APPLICATIONS DESIGNER (ADVERSE FACTORS SUCH AS THESE ARE HEREINAFTER COLLECTIVELY TERMED “SYSTEM FAILURES”). ANY APPLICATION WHERE A SYSTEM FAILURE WOULD CREATE A RISK OF HARM TO PROPERTY OR PERSONS (INCLUDING THE RISK OF BODILY INJURY AND DEATH) SHOULD NOT BE RELIANT SOLELY...
UPON ONE FORM OF ELECTRONIC SYSTEM DUE TO THE RISK OF SYSTEM FAILURE. TO AVOID DAMAGE, INJURY, OR DEATH,
THE USER OR APPLICATION DESIGNER MUST TAKE REASONABLY PRUDENT STEPS TO PROTECT AGAINST SYSTEM FAILURES,
INCLUDING BUT NOT LIMITED TO BACK-UP OR SHUT DOWN MECHANISMS. BECAUSE EACH END-USER SYSTEM IS
CUSTOMIZED AND DIFFERS FROM NATIONAL INSTRUMENTS TESTING PLATFORMS AND BECAUSE A USER OR APPLICATION
DESIGNER MAY USE NATIONAL INSTRUMENTS PRODUCTS IN COMBINATION WITH OTHER PRODUCTS IN A MANNER NOT
EVALUATED OR CONTEMPLATED BY NATIONAL INSTRUMENTS, THE USER OR APPLICATION DESIGNER IS ULTIMATELY
RESPONSIBLE FOR VERIFYING AND VALIDATING THE SUITABILITY OF NATIONAL INSTRUMENTS PRODUCTS WHENEVER
NATIONAL INSTRUMENTS PRODUCTS ARE INCORPORATED IN A SYSTEM OR APPLICATION, INCLUDING, WITHOUT
LIMITATION, THE APPROPRIATE DESIGN, PROCESS AND SAFETY LEVEL OF SUCH SYSTEM OR APPLICATION.
Contents

About This Manual
Conventions .......................................................... vii
Related Documentation ........................................ viii

Chapter 1
Getting Started
Unpacking ............................................................. 1-1
What You Need to Get Started .................................. 1-1
Key Features ........................................................ 1-2
Chassis Description ............................................... 1-4
Optional Equipment ............................................ 1-6
  EMC Filler Panels .............................................. 1-6
  Rack Mount Kit ................................................ 1-6
  Slot Blockers ................................................... 1-6
NI PXIe-1062Q Chassis Backplane Overview .... 1-6
  Interoperability with CompactPCI ..................... 1-6
  System Controller Slot .................................. 1-7
  Hybrid Peripheral Slots ................................ 1-7
  PXI Peripheral Slots .................................... 1-8
  System Timing Slot ...................................... 1-8
  PXI Local Bus ............................................... 1-9
  PXI Trigger Bus ............................................ 1-10
  System Reference Clock ................................. 1-10
  PXIe_SYNC_CTRL ........................................... 1-13

Chapter 2
Installation and Configuration
Safety Information ............................................ 2-1
Chassis Cooling Considerations ............................. 2-2
  Providing Adequate Clearance .......................... 2-2
  Chassis Ambient Temperature Definition ............ 2-5
  Setting Fan Speed ........................................ 2-5
  Installing Filler Panels .................................. 2-5
  Installing Slot Blockers ................................ 2-5
Rack Mounting .................................................. 2-5
Connecting Safety Ground .................................. 2-6
Connecting to Power Source .............................. 2-6
Installing a PXI Express System Controller .......... 2-7
About This Manual

The *NI PXIe-1062Q User Manual* describes the features of the NI PXIe-1062Q chassis and contains information about configuring the chassis, installing the modules, and operating the chassis.

Conventions

The following conventions are used in this manual:

»

The » symbol leads you through nested menu items and dialog box options to a final action. The sequence Options»Settings»General directs you to pull down the Options menu, select the Settings item, and select General from the last dialog box.

This icon denotes a note, which alerts you to important information.

This icon denotes a caution, which advises you of precautions to take to avoid injury, data loss, or a system crash. When this symbol is marked on the product, refer to the *Read Me First: Safety and Electromagnetic Compatibility* document, shipped with the product, for precautions to take.

**bold**

Bold text denotes items that you must select or click in the software, such as menu items and dialog box options. Bold text also denotes parameter names.

**italic**

Italic text denotes variables, emphasis, a cross-reference, or an introduction to a key concept. Italic text also denotes text that is a placeholder for a word or value that you must supply.

**monospace**

Text in this font denotes text or characters that you should enter from the keyboard, sections of code, programming examples, and syntax examples. This font is also used for the proper names of disk drives, paths, directories, programs, subprograms, subroutines, device names, functions, operations, variables, filenames, and extensions.
Related Documentation

The following documents contain information that you might find helpful as you read this manual:

- *PICMG EXP.0 R1.0 CompactPCI Express Specification*, PCI Industrial Computers Manufacturers Group
- *PCI Express Base Specification*, Revision 1.1, PCI Special Interest Group
- *PXI-5 PXI Express Hardware Specification*, Revision 2.0, PXI Systems Alliance
Getting Started

This chapter describes the key features of the NI PXIe-1062Q chassis and lists the kit contents and optional equipment you can order from National Instruments.

Unpacking

Carefully inspect the shipping container and the chassis for damage. Check for visible damage to the metal work. Check to make sure all handles, hardware, and switches are undamaged. Inspect the inner chassis for any possible damage, debris, or detached components. If damage appears to have been caused during shipment, file a claim with the carrier. Retain the packing material for possible inspection and/or reshipment.

What You Need to Get Started

The NI PXIe-1062Q chassis kit contains the following items:

- NI PXIe-1062Q chassis
- Filler panels
- AC power cable—refer to Table 1-1 for AC power cables
- NI PXIe-1062Q User Manual
- Software media with PXI Platform Services 2.0 or higher
- Read Me First: Safety and Electromagnetic Compatibility
- Chassis number labels
Chapter 1  Getting Started

Table 1-1. AC Power Cables

<table>
<thead>
<tr>
<th>Power Cable</th>
<th>Reference Standards</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard 120 V (USA)</td>
<td>ANSI C73.11/NEMA 5-15-P/IEC83</td>
</tr>
<tr>
<td>Switzerland 220 V</td>
<td>SEV</td>
</tr>
<tr>
<td>Australia 240 V</td>
<td>AS C112</td>
</tr>
<tr>
<td>Universal Euro 230 V</td>
<td>CEE (7), II, IV, VII IEC83</td>
</tr>
<tr>
<td>North America 120 V</td>
<td>ANSI C73.20/NEMA 5-15-P/IEC83</td>
</tr>
<tr>
<td>United Kingdom 230 V</td>
<td>BS 1363/IEC83</td>
</tr>
</tbody>
</table>

If you are missing any of the items listed in Table 1-1, or if you have the incorrect AC power cable, contact National Instruments.

Key Features

The NI PXIe-1062Q chassis combines a high-performance 8-slot PXI Express backplane with a high-output power supply and a structural design that has been optimized for maximum usability in a wide range of applications. The chassis’ modular design ensures a high level of maintainability, resulting in a very low mean time to repair (MTTR). The NI PXIe-1062Q chassis fully complies with the PXI-5 PXI Express Hardware Specification, offering advanced timing and synchronization features.

The key features of the NI PXIe-1062Q chassis include the following:

High Performance for Instrumentation Requirements

- Up to 1 GB/s (single direction) per PXI Express slot dedicated bandwidth (x4 PCIe)
- 353.9 W available power for 0 to 55 °C
- 30 W per slot cooling meets increased PXI Express cooling requirements
- Low-jitter internal 10 MHz reference clock for PXI slots with ± 25 ppm stability
- Low-jitter internal 100 MHz reference clock for PXI Express slots with ± 25 ppm stability
- Quiet operation for 0 to 30 °C at 43.6 dBA
• Variable speed fan controller optimizes cooling and acoustic emissions
• Remote power-inhibit control
• Complies with PXI and CompactPCI Specifications

High Reliability
• 0 to 55 °C extended temperature range
• Power supply, temperature, and fan monitoring
• HALT tested for increased reliability
• Field replaceable power supply shuttle

Multi-Chassis Support
• PXI Express System Timing Slot for tight synchronization across chassis
• Rear CLK10 I/O connectors
• Switchless CLK10 routing

Optional Features
• Front and rear rack-mount kits
• Replacement power supply shuttle
• EMC filler panels
• Slot blockers for improved cooling performance
• Factory installation services
Chassis Description

Figures 1-1 and 1-2 show the key features of the NI PXIe-1062Q chassis front and back panels. Figure 1-1 shows the front view of the NI PXIe-1062Q. Figure 1-2 shows the rear view of the NI PXIe-1062Q.

**Figure 1-1.** Front View of the NI PXIe-1062Q Chassis

1. Power Inhibit Switch
2. Power Inhibit Switch LED
3. Removable Feet
4. Chassis Carry Handle
5. Chassis Model Name
6. Backplane Connectors
7. System Controller Expansion Slots
8. PXI Express System Controller Slot
9. PXI Express Hybrid Peripheral Slots
10. PXI Express System Timing Slot
11. PXI Peripheral Slot
12. PXI Filler Panels
Figure 1-2. Rear View of the NI PXIe-1062Q Chassis

1 Power Supply Shuttle
2 Push-Reset Circuit Breaker
3 Universal AC Input
4 Chassis Ground Screw
5 10 MHz REF OUT BNC
6 10 MHz REF IN BNC
7 Remote Inhibit and Voltage Monitoring Connector
8 Air Filter Retainer
9 Air Filter Retainer Screw
10 Power Supply Shuttle ID Label
11 Fan Speed Selector Switch
12 Inhibit Mode Selector Switch
13 Power Supply Shuttle Handle (2x)
14 Power Supply Shuttle Mounting Screws (8x)
Optional Equipment

Contact National Instruments to order the following options for the NI PXIe-1062Q chassis.

EMC Filler Panels

Optional EMC filler panel kits are available from National Instruments.

Rack Mount Kit

There are two optional kits for mounting the NI PXIe-1062Q chassis into a rack. The first option is a pair of mounting brackets for use on the front of the chassis. The second option is a rear rack mount kit. The rear rack mount kit differs from the front kit to allow for easier installation into the rack. For more information, refer to Figure A-3, *NI Chassis Rack Mount Kit Components*.

Slot Blockers

Optional slot blocker kits are available from National Instruments for improved thermal performance when all slots are not used.

NI PXIe-1062Q Chassis Backplane Overview

This section provides an overview of the backplane features for the NI PXIe-1062Q chassis.

Interoperability with CompactPCI

The design of the NI PXIe-1062Q provides you the flexibility to use the following devices in a single PXI Express chassis:

- PXI Express compatible products
- CompactPCI Express compatible 4-Link system controller products
- CompactPCI Express compatible Type-2 peripheral products
- PXI peripheral products
- Standard CompactPCI peripheral products
System Controller Slot

The system controller slot is Slot 1 of the chassis and is a 4-Link configuration system slot as defined by the CompactPCI Express and PXI Express specifications. It has three system controller expansion slots for system controller modules that are wider than one slot. These slots allow the system controller to expand to the left to prevent the system controller from using peripheral slots.

The backplane routes a x4 PCI Express link from the system controller slot to slots 3, 4, and 5, and a x1 PCI Express link to a PCI Express to PCI Translation Bridge on the backplane. The PCI Express to PCI Translation Bridge on the backplane provides a 32-bit/33MHz PCI bus to slots 2, 3, 5, 6, 7, and 8.

The system controller slot also has connectivity to some PXI features such as: PXI_CLK10, PXI Star, PXI Trigger Bus and PXI Local Bus 6.

By default, the system controller will control the power supply with the PS_ON# signals. A logic low on this line will turn the power supply on.

Note The Inhibit Mode switch on the rear of the chassis must be in the Default position for the system controller to have control of the power supply. Refer to the Inhibit Mode Switch section of Chapter 2, Installation and Configuration, for details about the Inhibit Mode switch.

Hybrid Peripheral Slots

The chassis provides two hybrid peripheral slots as defined by the PXI-5 PXI Express Hardware Specification: slot 3 and slot 5. A hybrid peripheral slot can accept the following peripheral modules:

- A PXI Express Peripheral with x4 or x1 PCI Express link to the system slot
- A CompactPCI Express Type-2 Peripheral with x4 or x1 PCI Express link to the system slot
- A hybrid-compatible PXI Peripheral module that has been modified by replacing the J2 connector with an XJ4 connector installed in the upper eight rows of J2. Refer to the PXI Express Specification for details. The PXI Peripheral communicates through the backplane’s 32-bit PCI bus.
- A CompactPCI 32-bit peripheral on the backplane’s 32-bit PCI bus

The hybrid peripheral slots provide full PXI Express functionality and 32-bit PXI functionality except for PXI Local Bus. The hybrid peripheral slot only connects to PXI Local Bus 6 left and right.
PXI Peripheral Slots

There are four PXI peripheral slots which will accept PXI or CompactPCI peripherals: slot 2, slot 6, slot 7, and slot 8. These slots are on the backplane’s 32-bit PCI bus. These slots offer full PXI functionality, but have no PXI Express features. The 64-bit PCI signals on the P2 connectors are not connected.

System Timing Slot

The System Timing Slot is slot 4. The system timing slot will accept the following peripheral modules:

- A PXI Express System Timing Module with x4 or x1 PCI Express link to the system slot.
- A PXI Express Peripheral with x4 or x1 PCI Express link to the system slot.
- A CompactPCI Express Type-2 Peripheral with x4 or x1 PCI Express link to the system slot.

The system timing slot has 3 dedicated differential pairs (PXIe_DSTAR) connected from the TP2 connector to the XP3 connector for each hybrid peripheral slot, as well as routed back to the XP3 connector of the system timing slot as shown in Figure 1-3. The PXIe_DSTAR pairs can be used for high-speed triggering, synchronization and clocking. Refer to the PXI Express Specification for details.

The system timing slot also has a single-ended (PXI Star) trigger connected to every slot. Refer to Figure 1-3 for details.

The system timing slot has a pin (PXI_CLK10_IN) through which a system timing module may source a 10MHz clock to which the backplane will phase-lock. Refer to the System Reference Clock section for details.

The system timing slot has a pin (PXIe_SYNC_CTRL) through which a system timing module can control the PXIe_SYNC100 timing. Refer to the PXI Express Specification and the PXIe_SYNC_CTRL section of this chapter for details.
Figure 1-3. PXle_DSTAR and PXI Star Connectivity Diagram

**PXI Local Bus**

The PXI backplane local bus is a daisy-chained bus that connects each peripheral slot with adjacent peripheral slots to the left and right, as shown in Figure 1-4.

The backplane routes the full 13-line PXI Local Bus between adjacent PXI slots (slots 6, 7, and 8) and PXI Local Bus 6 between all other slots. Refer to Figure 1-4 for details. The left local bus 6 from slot 1 is not routed anywhere and the right local bus signals from slot 8 are not routed anywhere.

Local bus signals may range from high-speed TTL signals to analog signals as high as 42 V.
Initialization software uses the configuration information specific to each adjacent peripheral module to evaluate local bus compatibility.

**Figure 1-4. PXI Trigger Bus and Local Bus Connectivity Diagram**

**PXI Trigger Bus**

All slots share eight trigger lines. You can use these trigger lines in a variety of ways. For example, you can use triggers to synchronize the operation of several different PXI peripheral modules. In other applications, one module can control carefully timed sequences of operations performed on other modules in the system. Modules can pass triggers to one another, allowing precisely timed responses to asynchronous external events the system is monitoring or controlling.

**System Reference Clock**

The NI PXIe-1062Q chassis supplies the PXI 10 MHz system clock signal (PXI_CLK10) independently driven to each peripheral slot and PXIe_CLK100 and PXIe_SYNC100 to the hybrid slots and system timing slot.

An independent buffer (having a source impedance matched to the backplane and a skew of less than 250 ps between slots) drives PXI_CLK10 to each peripheral slot. Refer to Figure 1-5 for the routing configuration of PXI_CLK10. You can use this common reference clock signal to synchronize multiple modules in a measurement or control system.

An independent buffer drives PXIe_CLK100 to the hybrid peripheral slots and system timing slot. Refer to Figure 1-5 for the routing configuration of PXIe_CLK100. These clocks are matched in skew to less than 100 ps. The
differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_CLK100 so that when there is no peripheral or a peripheral that does not connect to PXIe_CLK100, there is no clock being driven on the pair to that slot.

An independent buffer drives PXIe_SYNC100 to the hybrid peripheral slot and system timing slot. Refer to Figure 1-5 for the routing configuration of PXIe_SYNC100. These clocks are matched in skew to less than 100 ps. The differential pair must be terminated on the peripheral with LVPECL termination for the buffer to drive PXIe_SYNC100 so that when there is no peripheral or a peripheral that does not connect to PXIe_SYNC100, there is no clock being driven on the pair to that slot.

Figure 1-5. Distribution of PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100
PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 have the default timing relationship described in Figure 1-6.

![Figure 1-6. System Reference Clock Default Behavior](image)

To synchronize the system to an external clock, you can drive PXI_CLK10 from an external source through the PXI_CLK10_IN pin on the System Timing Slot. Refer to Table B-7, *XP4 Connector Pinout for the System Timing Slot*, for the pinout. When a 10 MHz clock is detected on this pin, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots (refer to Figure 1-5 for the distribution of PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100). Refer to Appendix A, *Specifications*, for the specification information for an external clock provided on the PXI_CLK10_IN pin of the system timing slot.

You also can drive a 10 MHz clock on the 10 MHz REF IN connector on the rear of the chassis. When a 10 MHz clock is detected on this connector, the backplane automatically phase-locks the PXI_CLK10, PXIe_CLK100, and PXIe_SYNC100 signals to this external clock and distributes these signals to the slots (refer to Figure 1-5 for the distribution of PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100). Refer to Appendix A, *Specifications*, for the specification information for an external clock provided on the 10 MHz REF IN connector on the rear panel of the chassis.
If the 10 MHz clock is present on both the PXI_CLK10_IN pin of the System Timing Slot and the 10 MHz REF IN connector on the rear of the chassis, the signal on the System Timing Slot is selected. Refer to Table 1-2 which explains how the 10 MHz clocks are selected by the backplane.

Table 1-2. Backplane External Clock Input Truth Table

<table>
<thead>
<tr>
<th>System Timing Slot PXI_CLK10_IN</th>
<th>Rear Chassis Panel 10 MHz REF IN</th>
<th>Backplane PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100</th>
</tr>
</thead>
<tbody>
<tr>
<td>No clock present</td>
<td>No clock present</td>
<td>Backplane generates its own clocks</td>
</tr>
<tr>
<td>No clock present</td>
<td>10 MHz clock present</td>
<td>PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to Rear Chassis Panel—10 MHz REF IN</td>
</tr>
<tr>
<td>10 MHz clock present</td>
<td>No clock present</td>
<td>PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to System Timing Slot—PXI_CLK10_IN</td>
</tr>
<tr>
<td>10 MHz clock present</td>
<td>10 MHz clock present</td>
<td>PXI_CLK10, PXIe_CLK100 and PXIe_SYNC100 all phase-locked to System Timing Slot—PXI_CLK10_IN</td>
</tr>
</tbody>
</table>

A copy of the backplane’s PXI_CLK10 is exported to the 10 MHz REF OUT connector on the rear of the chassis. This clock is driven by an independent buffer. Refer to Appendix A, Specifications, for the specification information for the 10 MHz REF OUT signal on the rear panel of the chassis.

**PXIe_SYNC_CTRL**

PXIe_SYNC100 is by default a 10 ns pulse synchronous to PXI_CLK10. The frequency of PXIe_SYNC100 is 10/n MHz, where n is a positive integer. The default for n is 1, giving PXIe_SYNC100 a 100 ns period. However, the backplane allows n to be programmed to other integers. For instance, setting n = 3 gives a PXIe_SYNC100 with a 300 ns period while still maintaining its phase relationship to PXI_CLK10. The value for n may be set to any positive integer from 1 to 255.

The system timing slot has a control pin for PXIe_SYNC100 called PXIe_SYNC_CTRL for use when n > 1. Refer to Table B-6, XP3 Connector Pinout for the System Timing Slot, for system timing slot pinout. Refer to Appendix A, Specifications, for the PXIe_SYNC_CTRL input specifications.
By default, a high-level detected by the backplane on the PXIe_SYNC_CTRL pin causes a synchronous restart for the PXIe_SYNC100 signal. On the next PXI_CLK10 edge the PXIe_SYNC100 signal will restart. This will allow several chassis to have their PXIe_SYNC100 in phase with each other. Refer to Figure 1-7 for timing details with this method.

Figure 1-7. PXIe_SYNC100 at 3.33 MHz Using PXIe_SYNC_CTRL as Restart
Installation and Configuration

This chapter describes how to prepare and operate the NI PXIe-1062Q chassis.

Before connecting the chassis to a power source, read this chapter and the Read Me First: Safety and Electromagnetic Compatibility document included with your kit.

Safety Information

⚠️ **Caution**  Before undertaking any troubleshooting, maintenance, or exploratory procedure, carefully read the following caution notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

- **Chassis Grounding**—The chassis requires a connection from the premise wire safety ground to the chassis ground. The earth safety ground must be connected during use of this equipment to minimize shock hazards. Refer to the Connecting Safety Ground section for instructions on connecting safety ground.

- **Live Circuits**—Operating personnel and service personnel must not remove protective covers when operating or servicing the chassis. Adjustments and service to internal components must be undertaken by qualified service technicians. During service of this product, the mains connector to the premise wiring must be disconnected. Dangerous voltages may be present under certain conditions; use extreme caution.

- **Explosive Atmosphere**—Do not operate the chassis in conditions where flammable gases are present. Under such conditions, this equipment is unsafe and may ignite the gases or gas fumes.
Chapter 2  Installation and Configuration

- **Part Replacement**—Only service this equipment with parts that are exact replacements, both electrically and mechanically. Contact National Instruments for replacement part information. Installation of parts with those that are not direct replacements may cause harm to personnel operating the chassis. Furthermore, damage or fire may occur if replacement parts are unsuitable.

- **Modification**—Do not modify any part of the chassis from its original condition. Unsuitable modifications may result in safety hazards.

## Chassis Cooling Considerations

The NI PXIe-1062Q chassis is designed to operate on a bench or in an instrument rack. Regardless of the configuration you must provide the cooling clearances as outlined in the following sections.

### Providing Adequate Clearance

The primary cooling exhaust vent for the NI PXIe-1062Q is on the top of the chassis. The primary intake vent is on the rear of the chassis where the air is filtered as it enters the power supply shuttle. The secondary intake and exhaust vents are located along the sides of the chassis. Adequate clearance between the chassis and surrounding equipment or blockages must be maintained to ensure proper cooling of the chassis power supply as well as the modules plugged into the chassis. These clearances are outlined in Figure 2-1. The vent locations for the NI PXIe-1062Q chassis are shown in Figure 2-2. Failure to provide these clearances may result in thermal-related failures in the chassis or modules.
Figure 2-1. NI PXIe-1062Q Cooling Clearances
Figure 2-2. NI PXIe-1062Q Vents
Chapter 2  Installation and Configuration

Chassis Ambient Temperature Definition

The chassis fan control system uses intake air temperature as the input for controlling fan speeds when in Auto Fan Speed mode. Because of this, the chassis ambient temperature is defined as the temperature that exists just outside of the fan intake vents on the rear of the chassis. Note that this temperature may be higher than ambient room temperature depending on the surrounding equipment and/or blockages present. It is the user’s responsibility to ensure that this ambient temperature does not exceed the rated ambient temperature as stated in Appendix A, Specifications. If the temperature exceeds the stated spec the power switch LED will blink green, as discussed in the Power Inhibit Switch LED Indicator section of this chapter.

Setting Fan Speed

The fan-speed selector switch is on the rear panel of the NI PXIe-1062Q chassis. Refer to Figure 1-2, Rear View of the NI PXIe-1062Q Chassis, to locate the fan-speed selector switch. Select High for maximum cooling performance or Auto for improved acoustic performance. When set to Auto, the fan speed is determined by chassis intake air temperature.

Installing Filler Panels

To maintain proper module cooling performance, install filler panels (provided with the chassis) in unused or empty slots. Secure with the captive mounting screws provided.

Installing Slot Blockers

The cooling performance of the chassis can be improved by installing optional slot blockers. Refer to ni.com for more details.

Rack Mounting

Rack mount applications require the optional rack mount kits available from National Instruments. Refer to the instructions supplied with the rack mount kits to install your NI PXIe-1062Q chassis in an instrument rack. Refer to Figure A-3, NI Chassis Rack Mount Kit Components.

Note  You may want to remove the feet from the NI PXIe-1062Q chassis when rack mounting. To do so, remove the screws holding the feet in place.
Connecting Safety Ground

**Caution** The NI PXIe-1062Q chassis are designed with a three-position NEMA 5-15 style plug for the U.S. that connects the ground line to the chassis ground. To minimize shock hazard, make sure the electrical power outlet you use to power the chassis has an appropriate earth safety ground.

If your power outlet does not have an appropriate ground connection, you must connect the premise safety ground to the chassis grounding screw located on the rear panel. Refer to Figure 1-2, *Rear View of the NI PXIe-1062Q Chassis*, to locate the chassis grounding screw. To connect the safety ground, complete the following steps:

1. Connect a 16 AWG (1.3 mm) wire to the chassis grounding screw using a grounding lug. The wire must have green insulation with a yellow stripe or must be noninsulated (bare).
2. Attach the opposite end of the wire to permanent earth ground using toothed washers or a toothed lug.

Connecting to Power Source

**Cautions** Do *not* install modules prior to performing the following power-on test.

To completely remove power, you *must* disconnect the AC power cable.

Attach input power through the rear AC inlet using the appropriate AC power cable supplied. Refer to Figure 1-2, *Rear View of the NI PXIe-1062Q Chassis*, to locate the AC inlet.

The Inhibit Mode switch allows you to power on the chassis or place it in standby mode. Set the Inhibit Mode switch on the back of the chassis to the Manual position. Observe that all fans become operational and the power switch LED is a steady green. Switching the Inhibit Mode switch to the Default position allows the system controller to control the power supply.
Installing a PXI Express System Controller

This section contains general installation instructions for installing a PXI Express system controller in a NI PXIe-1062Q chassis. Refer to your PXI Express system controller user manual for specific instructions and warnings. To install a system controller, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the system controller. The AC power cord grounds the chassis and protects it from electrical damage while you install the system controller.

2. Install the system controller into the system controller slot (slot 1, indicated by the red card guides) by first placing the system controller PCB into the front of the card guides (top and bottom). Slide the system controller to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-3.
3. When you begin to feel resistance, push up on the injector/ejector handle to seat the system controller fully into the chassis frame. Secure the system controller front panel to the chassis using the system controller front-panel mounting screws.

4. Connect the keyboard, mouse, and monitor to the appropriate connectors. Connect devices to ports as required by your system configuration.

5. Power on the chassis. Verify that the system controller boots. If the system controller does not boot, refer to your system controller user manual.

Figure 2-4 shows a PXI Express system controller installed in the system controller slot of a NI PXIe-1062Q chassis. You can place CompactPCI, CompactPCI Express, PXI, or PXI Express modules in other slots depending on the slot type.
Installing Peripheral Modules

⚠️ **Caution**  The NI PXIe-1062Q chassis has been designed to accept a variety of peripheral module types in different slots. To prevent damage to the chassis, ensure that the peripheral module is being installed into a slot designed to accept it. Refer to Chapter 1, *Getting Started*, for a description of the various slot types.

This section contains general installation instructions for installing a peripheral module in a NI PXIe-1062Q chassis. Refer to your peripheral module user manual for specific instructions and warnings. To install a module, complete the following steps:

1. Connect the AC power source to the PXI Express chassis before installing the module. The AC power cord grounds the chassis and protects it from electrical damage while you install the module.

2. Ensure that the chassis is powered off.

3. Install a module into a chassis slot by first placing the module card PCB into the front of the card guides (top and bottom), as shown in Figure 2-5. Slide the module to the rear of the chassis, making sure that the injector/ejector handle is pushed down as shown in Figure 2-5.

4. When you begin to feel resistance, push up on the injector/ejector handle to fully seat the module into the chassis frame. Secure the module front panel to the chassis using the module front-panel mounting screws.
Power Inhibit Switch LED Indicator

The chassis power inhibit switch has an integrated LED. This LED indicates one of four different conditions:

- If the inhibit switch LED is steady green (not flashing), the chassis is powered on and operating normally.
- If the inhibit switch LED is flashing green, the air-intake temperature has exceeded the chassis operating range.
• If the inhibit switch LED is flashing red, the power supply outputs are not within voltage regulation requirements.
• If the inhibit switch LED is steady red, the system fans or power supply fan has failed. The remaining fans will automatically be driven high.

**Note** If both system fans or the power supply fan fails the chassis will shut down automatically, preventing the chassis and modules from damage due to overheating.

### Remote Voltage Monitoring and Control

The NI PXIe-1062Q chassis supports remote voltage monitoring and inhibiting through a female 9-pin D-SUB (DB-9) connector located on the rear panel. Table 2-1 shows the pinout of the 9-pin D-SUB (DB-9) connector.

<table>
<thead>
<tr>
<th>DB-9 Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Logic Ground</td>
</tr>
<tr>
<td>2</td>
<td>+5 VDC</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
</tr>
<tr>
<td>4</td>
<td>+3.3 VDC</td>
</tr>
<tr>
<td>5</td>
<td>Inhibit (Active Low)</td>
</tr>
<tr>
<td>6</td>
<td>+12 VDC</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
</tr>
<tr>
<td>8</td>
<td>–12 VDC</td>
</tr>
<tr>
<td>9</td>
<td>Logic Ground</td>
</tr>
</tbody>
</table>
Caution When connecting digital voltmeter probes to the rear 9-pin D-SUB (DB-9) connector, be careful not to short the probe leads together. Doing so could damage the power supply.

You can use a digital voltmeter to ensure all voltage levels in the NI PXIe-1062Q chassis are within the allowable limits. Referring to Table 2-2, connect one lead of the voltmeter to a supply pin on the remote voltage monitoring connector (9-pin D-SUB) on the rear panel. Refer to Table 2-1 for a pinout diagram of the remote voltage monitoring connector. Connect the reference lead of the voltmeter to one of the ground pins. Compare each voltage reading to the values listed in Table 2-2.

Note Use the rear-panel 9-pin D-SUB connector to check voltages only. Do not use the connector to supply power to external devices.

Table 2-2. Power Supply Voltages at Voltage Monitoring Connector (DB-9)

<table>
<thead>
<tr>
<th>Pin</th>
<th>Supply</th>
<th>Acceptable Voltage Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>+5 V</td>
<td>4.75 to 5.25 V</td>
</tr>
<tr>
<td>4</td>
<td>+3.3 V</td>
<td>3.135 to 3.465 V</td>
</tr>
<tr>
<td>6</td>
<td>+12 V</td>
<td>11.4 to 12.6 V</td>
</tr>
<tr>
<td>8</td>
<td>–12 V</td>
<td>–12.6 to –11.4 V</td>
</tr>
<tr>
<td>1, 9</td>
<td>Logic Ground</td>
<td>0 V</td>
</tr>
</tbody>
</table>

If the voltages fall within the specified ranges, the chassis complies with the CompactPCI voltage-limit specifications.
Inhibit Mode Switch

On the rear panel of the chassis there is an Inhibit Mode switch. Refer to Figure 1-2, Rear View of the NI PXIe-1062Q Chassis, for the location. The Inhibit Mode switch is recessed to prevent it from accidentally being switched.

The Inhibit Mode switch should be in the Default position when normal power inhibit switch functionality is desired. If the user needs to power on a chassis without a system controller installed the switch should be in the Manual position.

When the Inhibit Mode switch is set to the Manual position, the power supplies are enabled, and you can use the Inhibit signal (active low) on pin 5 of the Remote Inhibit and Voltage Monitoring connector to power off the chassis. To remotely power off the chassis, connect the Inhibit pin (pin 5) to a Logic Ground pin (pin 1 or 9). As long as this connection exists, the chassis will remain off (standby); when you remove this connection, the chassis turns on.

Note For the Remote Inhibit signal to control the On/Off (standby) state of the chassis, the Inhibit Mode switch must be in the Manual position.

PXI_CLK10 Rear Connectors

There are two BNC connectors on the rear of the NI PXIe-1062Q chassis for PXI_CLK10. The connectors are labeled IN and OUT. You can use them for supplying the backplane with PXI_CLK10 or routing the backplane’s PXI_CLK10 to another chassis. Refer to the System Reference Clock section of Chapter 1, Getting Started, for details about these signals.
PXI Express System Configuration with MAX

The PXI Platform Services software included with your chassis automatically identifies your PXI Express system components to generate a `pxiesys.ini` file. You can configure your entire PXI system and identify PXI-1 chassis through Measurement & Automation Explorer (MAX), included with your system controller. MAX creates the `pxiesys.ini` and `pxisys.ini` file, which define your PXI system parameters. MAX also provides an interface to route and reserve triggers so dynamic routing, through drivers such as DAQmx, avoids double-driving and potentially damaging trigger lines. For more information about routing and reserving PXI triggers, refer to KnowledgeBase 3TJDOND8 at ni.com/support.

The configuration steps for single or multiple-chassis systems are the same.

Figure 2-6. Multichassis Configuration in MAX
PXI-1 System Configuration

1. Launch MAX.

2. In the Configuration tree, click the Devices and Interfaces branch to expand it.

3. If the PXI system controller has not yet been configured, it is labeled PXI System (Unidentified). Right-click this entry to display the pop-up menu, then select the appropriate system controller model from the Identify As submenu.

4. Click the PXI system controller. The chassis (or multiple chassis, in a multichassis configuration) is listed below it. Identify each chassis by right-clicking its entry, then selecting the appropriate chassis model through the Identify As submenu. Further expanding the PXI System branch shows all devices in the system that can be recognized by NI-VISA. When your system controller and all your chassis are identified, the required pxisys.ini file is complete.

The PXI specification allows for many combinations of PXI chassis and system modules. To assist system integrators, the manufacturers of PXI chassis and system modules must document the capabilities of their products. PXI Express devices must provide a driver and .ini file for identification. These files are provided as part of the PXI Platform Services software included with your system controller. The minimum documentation requirements for PXI-1 are contained in .ini files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these .ini files.

The capability documentation for a PXI-1 chassis is contained in a chassis.ini file provided by the chassis manufacturer. The information in this file is combined with information about the system controller to create a single PXI-1 system initialization file called pxisys.ini (PXI System Initialization). The NI system controller uses MAX to generate the pxisys.ini file from the chassis.ini file.

Device drivers and other utility software read the pxisys.ini and pxisys.ini file to obtain system information. For detailed information about initialization files, refer to the PXI specification at www.pxisa.org.
Using System Configuration and Initialization Files

The PXI Express specification allows many combinations of PXI Express chassis and system modules. To assist system integrators, the manufacturers of PXI Express chassis and system modules must document the capabilities of their products. The minimum documentation requirements are contained in .ini files, which consist of ASCII text. System integrators, configuration utilities, and device drivers can use these .ini files.

The capability documentation for the NI PXIe-1062Q chassis is contained in the chassis.ini file on the software media that comes with the chassis. The information in this file is combined with information about the system controller to create a single system initialization file called pxisys.ini (PXI System Initialization). The system controller manufacturer either provides a pxisys.ini file for the particular chassis model that contains the system controller or provides a utility that can read an arbitrary chassis.ini file and generate the corresponding pxisys.ini file. System controllers from NI provide the pxisys.ini file for the NI PXIe-1062Q chassis, so you should not need to use the chassis.ini file. Refer to the documentation provided with the system controller or to ni.com/support for more information on pxisys.ini and chassis.ini files.

Device drivers and other utility software read the pxisys.ini file to obtain system information. The device drivers should have no need to directly read the chassis.ini file. For detailed information regarding initialization files, refer to the PXI Express specification at www.pxisa.org.
3

Maintenance

This chapter describes basic maintenance procedures you can perform on the NI PXIe-1062Q chassis.

⚠️ Caution Disconnect the power cable prior to servicing a NI PXIe-1062Q chassis.

Service Interval

Clean the chassis fan filters at a maximum interval of six months. Depending on the amount of use and ambient dust levels in the operating environment, the filters may require more frequent cleaning.

Clean dust from the chassis exterior (and interior) as needed, based on the operating environment. Periodic cleaning increases reliability.

Preparation

The information in this section is designed for use by qualified service personnel. Read the Read Me First: Safety and Electromagnetic Compatibility document included with your kit before attempting any procedures in this chapter.

⚠️ Caution Many components within the chassis are susceptible to static discharge damage. Service the chassis only in a static-free environment. Observe standard handling precautions for static-sensitive devices while servicing the chassis. Always wear a grounded wrist strap or equivalent while servicing the chassis.

Cleaning

Cleaning procedures consist of exterior and interior cleaning of the chassis and cleaning the fan filters. Refer to your module user documentation for information on cleaning the individual CompactPCI or PXI Express modules.

⚠️ Caution Always disconnect the AC power cable before cleaning or servicing the chassis.
Chapter 3  Maintenance

Interior Cleaning
Use a dry, low-velocity stream of air to clean the interior of the chassis. Use a soft-bristle brush for cleaning around components.

Exterior Cleaning
Clean the exterior surfaces of the chassis with a dry lint-free cloth or a soft-bristle brush. If any dirt remains, wipe with a cloth moistened in a mild soap solution. Remove any soap residue by wiping with a cloth moistened with clear water. Do not use abrasive compounds on any part of the chassis.

Caution  Avoid getting moisture inside the chassis during exterior cleaning, especially through the top vents. Use just enough moisture to dampen the cloth.

Do not wash the front- or rear-panel connectors or switches. Cover these components while cleaning the chassis.

Do not use harsh chemical cleaning agents; they may damage the chassis. Avoid chemicals that contain benzene, toluene, xylene, acetone, or similar solvents.

Cleaning the Fan Filters
Dirty fan filters can dramatically affect the cooling performance of a NI PXIe-1062Q chassis. Clean the filters whenever they become visibly dirty. You can easily remove the chassis air filters from the rear of the chassis by removing the filter retainer. To remove the filter retainer, loosen the retainer screw. The filter cover and retainer are shown in Figure 1-2, Rear View of the NI PXIe-1062Q Chassis.

Clean the fan filters by washing them in a mild soap solution and then vacuuming or blowing air through them. Rinse the filters with water and allow them to dry before reinstalling them on the chassis.

Resetting the AC Mains Circuit Breaker
If the NI PXIe-1062Q chassis is connected to an AC source and encounters an over-current condition, the circuit breaker on the rear panel will trip to prevent damage to the chassis. Complete the following steps to reset the circuit breaker.
1. Turn off the chassis.
2. Disconnect the AC power cable.
3. Depress the circuit breaker to reset it.
4. Reconnect the AC power cable.
5. Turn on the chassis.

If the circuit breaker trips again, complete the following steps:
1. Turn off the chassis.
2. Disconnect the AC power cable.
3. Remove all modules from the chassis.
4. Complete the procedure described in the Connecting to Power Source section of Chapter 2, Installation and Configuration. If the power switch LED is not a steady green, contact National Instruments.
5. Verify that the NI PXIe-1062Q chassis can meet the power requirements of your CompactPCI or PXI Express modules. Overloading the chassis can cause the breaker to trip. Refer to Appendix A, Specifications.
6. The over-current condition that caused the circuit breaker to trip may be due to a faulty CompactPCI or PXI Express module. Refer to the documentation supplied with the modules for troubleshooting information.

**Replacing the Modular Power Supply**

This section describes how to remove, configure, and install the AC power supply shuttle in the NI PXIe-1062Q chassis.

⚠️ **Cautions** Disconnect the power cable prior to replacing the power supply.

Do not attempt to use a power supply shuttle from another chassis such as the NI PXI-1042. Doing so may damage your chassis and the power supply shuttle.

Before connecting the power supply shuttle to a power source, read this section and the Read Me First: Safety and Electromagnetic Compatibility document included with the kit.

**Removal**

The NI PXIe-1062Q AC power supply is a replacement part for the NI PXIe-1062Q AC chassis. Before attempting to replace the power supply shuttle, verify that there is adequate clearance behind the chassis. Disconnect the power cable from the power supply shuttle on the back of the chassis. Identify the eight mounting screws for the NI PXIe-1062Q that
attach the power supply shuttle to the chassis. Refer to Figure 1-2, Rear View of the NI PXIe-1062Q Chassis, for the screw locations. Using a Phillips screwdriver, remove the screws. Pull on the two rear handles of the power supply shuttle to remove it from the back of the chassis.

Installation

Ensure that there is no visible damage to the new power supply shuttle. Verify that the housing and connector on the new power supply shuttle have no foreign material inside. Remove the protective cap on the PXI_CLK10 connector. Install the new power supply shuttle into the opening on the rear of the chassis. Replace and tighten the eight screws with a Phillips screwdriver.

Configuration

The fan-speed selector switch is on the rear panel of the power supply shuttle. Refer to Figure 1-2, Rear View of the NI PXIe-1062Q Chassis, to locate the fan-speed selector. Select High for maximum cooling performance (recommended) or Auto for quieter operation. Set the Inhibit Mode switch to the Default position.

Connecting Safety Ground

Refer to the Connecting Safety Ground section of Chapter 2, Installation and Configuration.

Connecting to Power Source

Refer to the Connecting to Power Source section of Chapter 2, Installation and Configuration.
Specifications

This appendix contains specifications for the NI PXIe-1062Q chassis.

⚠️ Caution
Specifications are subject to change without notice.

Electrical

### AC Input

Input voltage range................. 100 to 240 VAC
Operating voltage range\(^1\)........ 90 to 264 VAC
Input frequency ....................... 50/60 Hz
Operating frequency range\(^1\) ..... 47 to 63 Hz
Input current rating.................. 8 A
Over-current protection.............. 10 A circuit breaker

Line regulation
- 3.3 V........................................... <±0.2%
- 5 V............................................. <±0.1%
- ±12 V ....................................... <±0.1%

Efficiency................................. 70% typical

\(^1\) The operating range is guaranteed by design.
Power disconnect....................................The AC power cable provides main power disconnect. The front-panel power switch causes the internal chassis power supply to provide DC power to the CompactPCI/PXI Express backplane. You also can use the rear-panel D-SUB 9-pin connector and power mode switch to control the internal chassis power supply.

## DC Output

DC current capacity (I\textsubscript{MP})

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Maximum Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3.3 V</td>
<td>32 A</td>
</tr>
<tr>
<td>+5 V</td>
<td>30 A</td>
</tr>
<tr>
<td>+12 V</td>
<td>25 A</td>
</tr>
<tr>
<td>–12 V</td>
<td>1.5 A</td>
</tr>
<tr>
<td>5 V\textsubscript{AUX}</td>
<td>2 A</td>
</tr>
</tbody>
</table>

**Note** Maximum total usable power is 353.6 W.

Backplane slot current capacity

<table>
<thead>
<tr>
<th>Slot</th>
<th>+5 V</th>
<th>V (I/O)</th>
<th>+3.3 V</th>
<th>+12 V</th>
<th>–12 V</th>
<th>5 V\textsubscript{AUX}</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Controller Slot</td>
<td>15 A</td>
<td>—</td>
<td>15 A</td>
<td>30 A</td>
<td>—</td>
<td>1 A</td>
</tr>
<tr>
<td>System Timing Slot</td>
<td>—</td>
<td>—</td>
<td>6 A</td>
<td>4 A</td>
<td>—</td>
<td>1 A</td>
</tr>
<tr>
<td>Hybrid Peripheral Slot with PXI-1 Peripheral</td>
<td>6 A</td>
<td>5 A</td>
<td>6 A</td>
<td>1 A</td>
<td>1 A</td>
<td>—</td>
</tr>
<tr>
<td>Hybrid Peripheral Slot with PXI-5 Peripheral</td>
<td>—</td>
<td>—</td>
<td>6 A</td>
<td>4 A</td>
<td>—</td>
<td>1 A</td>
</tr>
<tr>
<td>PXI-1 Peripheral Slot</td>
<td>6 A</td>
<td>11 A</td>
<td>6 A</td>
<td>1 A</td>
<td>1 A</td>
<td>—</td>
</tr>
</tbody>
</table>
Notes  Total system slot current should not exceed 45 A.

PCI V(I/O) pins in PXI-1 peripheral slots and hybrid peripheral slots are connected to +5 V.

The maximum power dissipated in the system slot should not exceed 140 W.

The maximum power dissipated in a peripheral slot should not exceed 38.25 W.

Load regulation

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Load Regulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3.3 V</td>
<td>&lt;5%</td>
</tr>
<tr>
<td>+12 V</td>
<td>&lt;5%</td>
</tr>
<tr>
<td>+5 V</td>
<td>&lt;5%</td>
</tr>
<tr>
<td>−12 V</td>
<td>&lt;5%</td>
</tr>
</tbody>
</table>

Maximum ripple and noise (20 MHz bandwidth)

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Maximum Ripple and Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>+3.3 V</td>
<td>50 mV_{pp}</td>
</tr>
<tr>
<td>+12 V</td>
<td>50 mV_{pp}</td>
</tr>
<tr>
<td>+5 V</td>
<td>50 mV_{pp}</td>
</tr>
<tr>
<td>−12 V</td>
<td>50 mV_{pp}</td>
</tr>
</tbody>
</table>

Over-current protection.......................... All outputs protected from short
circuit and overload with
automatic recovery

Over-voltage protection

3.3 V and 5 V ................................. Clamped at 20 to 30% above
nominal output voltage

Power supply shuttle MTTR................. Replacement in under 5 minutes
Appendix A Specifications

Chassis Cooling

Module cooling system
NI PXIe-1062Q ...............................Forced air circulation (positive pressurization) through two 110 cfm fans with High/Auto speed selector
Slot airflow direction .........................Bottom of module to top of module
Module cooling intake ........................Bottom rear of chassis
Module cooling exhaust ......................Along both sides and top of chassis

Power supply cooling system ...............Forced air circulation through integrated fan
Power supply cooling intake ................Right side of chassis
Power supply cooling exhaust ..............Left side of chassis

Environmental

Maximum altitude ..........................2,000 m (800 mbar)
(at 25 °C ambient)
Pollution Degree ...........................2
For indoor use only.

Operating Environment

Ambient temperature range ..............0 to 55 °C
(Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range ..................10 to 90%, noncondensing
(Tested in accordance with IEC-60068-2-56.)
Appendix A Specifications

Storage Environment

Ambient temperature range: –40 to 71 °C
(Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)

Relative humidity range: 5 to 95%, noncondensing
(Tested in accordance with IEC-60068-2-56.)

Shock and Vibration

Operational shock: 30 g peak, half-sine, 11 ms pulse
(Tested in accordance with IEC-60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)

Random Vibration
Operating: 5 to 500 Hz, 0.3 g_{rms}
Nonoperating: 5 to 500 Hz, 2.4 g_{rms}
(Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Acoustic Emissions

Sound Pressure Level (at Operator Position)
(Tested in accordance with ISO 7779. Meets MIL-PRF-28800F requirements.)

Auto fan (up to ~30 °C ambient): 43.6 dBA

High fan: 62 dBA

Sound Power

Auto fan (up to ~30 °C ambient): 52.8 dBA

High fan: 72 dBA
Appendix A Specifications

Safety

This product is designed to meet the requirements of the following standards of safety for information technology equipment:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label or the Online Product Certification section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326 (IEC 61326): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note For the standards applied to assess the EMC of this product, refer to the Online Product Certification section.

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance

This product meets the essential requirements of applicable European Directives as follows:

- 2006/95/EC; Low-Voltage Directive (safety)
- 2004/108/EC; Electromagnetic Compatibility Directive (EMC)

Online Product Certification

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.
Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers

At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

Backplane

Size........................................................................... 3U-sized; one system slot (with three system expansion slots) and seven peripheral slots. Compliant with IEEE 1101.10 mechanical packaging. PXI Express Specification compliant. Accepts both PXI Express and CompactPCI (PICMG 2.0 R 3.0) 3U modules.

Backplane bare-board material ............ UL 94 V-0 Recognized

Backplane connectors ......................... Conforms to IEC 917 and IEC 1076-4-101, and are UL 94 V-0 rated

(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)
System Synchronization Clocks  
(PXI_CLK10, PXIe_CLK100, PXIe_SYNC100)

**10 MHz System Reference Clock: PXI_CLK10**

- Maximum slot-to-slot skew: 250 ps
- Accuracy: ±25 ppm max. (guaranteed over the operating temperature range)
- Maximum jitter: 5 ps RMS phase-jitter (10 Hz–1 MHz range)
- Duty-factor: 45%–55%
- Unloaded signal swing: 3.3 V ±0.3 V

**Note**  For other specifications refer to the *PXI-1 Hardware Specification*.

**100 MHz System Reference Clock: PXIe_CLK100 and PXIe_SYNC100**

- Maximum slot-to-slot skew: 100 ps
- Accuracy: ±25 ppm max. (guaranteed over the operating temperature range)
- Maximum jitter: 3 ps RMS phase-jitter (10 Hz–12 kHz range) 2 ps RMS phase-jitter (12 kHz–20 MHz range)
- Duty-factor for PXIe_CLK100: 45%–55%
- Absolute differential voltage  
  (When terminated with a 50 Ω load to 1.30 V or Thévenin equivalent): 400–1000 mV
- Single-ended $V_{OH}$: 2.0–2.5 V

**Note**  For other specifications, refer to the *PXI-5 PXI Express Hardware Specification*. 
External 10 MHz Reference Out  
(BNC on rear panel of chassis)  

Accuracy ................................................ ±25 ppm max. (guaranteed over the operating temperature range)  

Maximum jitter ...................................... 5 ps RMS phase-jitter  
(10 Hz–1 MHz range)  

Output amplitude .................................... 1 V_{pp} ±20% square-wave  
into 50 Ω  
2 V_{pp} unloaded  

Output impedance ................................. 50 Ω ±5 Ω  

External Clock Source  
Frequency ............................................... 10 MHz ±100 PPM  

Input amplitude  
Rear panel BNC .............................. 200 mV_{pp} to 5 V_{pp} square-wave  
or sine-wave  

System timing slot  
PXI_CLK10_IN.............................. 5 V or 3.3 V TTL signal  

Rear panel BNC input impedance .............................. 50 Ω ±5 Ω  

Maximum jitter introduced by backplane ............................................. 1 ps RMS phase-jitter  
(10 Hz–1 MHz range)  

PXIe_SYNC_CTRL  
V_{HI}.......................................................... 3.0–5.5 V  
V_{IL}.......................................................... 0–0.8 V  

PXI Star Trigger  
Maximum slot-to-slot skew .................... 250 ps  

Backplane characteristic impedance ...... 65 Ω ±10%
**Appendix A Specifications**

**Notes** For PXI slot to PXI Star mapping refer to the *System Timing Slot* section of Chapter 1, *Getting Started*.

For other specifications refer to the *PXI-1 Hardware Specification*.

**PXI Differential Star Triggers (PXle-DSTARA, PXle-DSTARB, PXle-DSTARC)**

- Maximum slot-to-slot skew ................. 150 ps
- Maximum differential skew .................. 25 ps
- Backplane differential impedance .......... 100 Ω ±10%

**Notes** For PXIe slot to PXI DSTAR mapping refer to the *System Timing Slot* section of Chapter 1, *Getting Started*.

For other specifications, the NI PXIe-1062Q complies with the *PXI-5 PXI Express Hardware Specification*.

**DMA Support**

For more information about this chassis’ support of hardware modules with 64-bit DMA and/or 32-bit DMA with PAE mode, please visit ni.com/info and enter the Info Code PXI64HANG.

**Mechanical**

Overall dimensions

Standard chassis

- Height ........................................ 6.97 in. (177.1 mm)
- Width ........................................ 10.68 in. (271.4 mm)
- Depth ........................................ 15.61 in. (396.5 mm)

**Note** 0.57 in. (14.5 mm) is added to height when feet are installed. When tilted with front feet extended on table top, height is increased approximately 2.08 in. (52.8 mm) in front and 0.583 in. (14.8 mm) in rear.

- Weight ........................................ 8.8 kg (19.4 lb)
- Chassis materials ............................. Sheet Aluminum (5052-H32, 3003-H14, and 6061-T6), Extruded Aluminum (6060-T6), and Cold Rolled Steel, PC-ABS, Santoprene, Nylon
Appendix A Specifications

Finish...................................................... Conductive Clear Iridite
on Aluminum
Clear Chromate Zinc Plating
on Cold Rolled Steel
Polyurethane Enamel

Figures A-1 and A-2 show the NI PXIe-1062Q chassis dimensions. The holes shown are for the installation of the optional rack mount kits. You can install those kits on the front or rear of the chassis, depending on which end of the chassis you want to face toward the front of the instrument cabinet. Notice that the front and rear chassis mounting holes (size M4) are symmetrical.
Figure A-1. NI PXIe-1062Q Chassis Dimensions (Front and Side)
Figure A-2. NI PXIe-1062Q Chassis Dimensions (Bottom)
Figure A-3 shows the chassis rack mount kit components.

![Figure A-3. NI Chassis Rack Mount Kit Components](image)

**Note**  The chassis shown in Figure A-3 is representative of the NI PXI-1042/NI PXIe-1062Q product line.
Pinouts

This appendix describes the connector pinouts for the NI PXIe-1062Q chassis backplane.

Table B-1 shows the XP1 Connector Pinout for the System Controller slot.
Table B-2 shows the XP2 Connector Pinout for the System Controller slot.
Table B-3 shows the XP3 Connector Pinout for the System Controller slot.
Table B-4 shows the XP4 Connector Pinout for the System Controller slot.
Table B-5 shows the TP2 Connector Pinout for the System Timing slot.
Table B-6 shows the XP3 Connector Pinout for the System Timing slot.
Table B-7 shows the XP4 Connector Pinout for the System Timing slot.
Table B-8 shows the P1 Connector Pinout for the Peripheral slots.
Table B-9 shows the P2 Connector Pinout for the Peripheral slots.
Table B-10 shows the P1 Connector Pinout for the Hybrid Peripheral slots.
Table B-11 shows the XP3 Connector Pinout for the Hybrid Peripheral slots.
Table B-12 shows the XP4 Connector Pinout for the Hybrid Peripheral slots.

For more detailed information, refer to the *PXI-5 PXI Express Hardware Specification*, Revision 2.0. Contact the PXI Systems Alliance for a copy of the specification.
## System Controller Slot Pinouts

### Table B-1. XP1 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pins</th>
<th>Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>GND</td>
</tr>
<tr>
<td>B</td>
<td>12V</td>
</tr>
<tr>
<td>C</td>
<td>12V</td>
</tr>
<tr>
<td>D</td>
<td>GND</td>
</tr>
<tr>
<td>E</td>
<td>5V</td>
</tr>
<tr>
<td>F</td>
<td>3.3V</td>
</tr>
<tr>
<td>G</td>
<td>GND</td>
</tr>
</tbody>
</table>

### Table B-2. XP2 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>cd</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3PETp1</td>
<td>3PETn1</td>
<td>GND</td>
<td>3PERp1</td>
<td>3PERn1</td>
<td>GND</td>
<td>3PETp2</td>
<td>3PETn2</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>3PETp3</td>
<td>3PETn3</td>
<td>GND</td>
<td>3PERp3</td>
<td>3PERn3</td>
<td>GND</td>
<td>3PERp2</td>
<td>3PERn2</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>4PETp0</td>
<td>4PETn0</td>
<td>GND</td>
<td>4PERp0</td>
<td>4PERn0</td>
<td>GND</td>
<td>4PETp1</td>
<td>4PETn1</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>4PETp2</td>
<td>4PETn2</td>
<td>GND</td>
<td>4PERp2</td>
<td>4PERn2</td>
<td>GND</td>
<td>4PERp1</td>
<td>4PERn1</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>4PETp3</td>
<td>4PETn3</td>
<td>GND</td>
<td>4PERp3</td>
<td>4PERn3</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
</tbody>
</table>
### Table B-3. XP3 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>cd</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>PWR_OK</td>
<td>PS_ON#</td>
<td>GND</td>
<td>LINKCAP</td>
<td>PWRBTN#</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>SMBDAT</td>
<td>SMBCLK</td>
<td>GND</td>
<td>4RefClk+</td>
<td>4RefClk-</td>
<td>GND</td>
<td>2RefClk+</td>
<td>2RefClk-</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>RSV</td>
<td>PERST#</td>
<td>GND</td>
<td>3RefClk+</td>
<td>3RefClk-</td>
<td>GND</td>
<td>1RefClk+</td>
<td>1RefClk-</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>1PETp0</td>
<td>1PETn0</td>
<td>GND</td>
<td>1PERp0</td>
<td>1PERn0</td>
<td>GND</td>
<td>1PETp1</td>
<td>1PETn1</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>1PETp2</td>
<td>1PETn2</td>
<td>GND</td>
<td>1PERp2</td>
<td>1PERn2</td>
<td>GND</td>
<td>1PERp1</td>
<td>1PERn1</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>1PETp3</td>
<td>1PETn3</td>
<td>GND</td>
<td>1PERp3</td>
<td>1PERn3</td>
<td>GND</td>
<td>2PETp0</td>
<td>2PETn0</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>2PETp1</td>
<td>2PETn1</td>
<td>GND</td>
<td>2PERp1</td>
<td>2PERn1</td>
<td>GND</td>
<td>2PERp0</td>
<td>2PERn0</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>2PETp2</td>
<td>2PETn2</td>
<td>GND</td>
<td>2PERp2</td>
<td>2PERn2</td>
<td>GND</td>
<td>2PETp3</td>
<td>2PETn3</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>3PETp0</td>
<td>3PETn0</td>
<td>GND</td>
<td>3PERp0</td>
<td>3PERn0</td>
<td>GND</td>
<td>2PETp3</td>
<td>2PETn3</td>
<td>GND</td>
</tr>
</tbody>
</table>

### Table B-4. XP4 Connector Pinout for the System Controller Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>GA4</td>
<td>GA3</td>
<td>GA2</td>
<td>GA1</td>
<td>GA0</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>5Vaux</td>
<td>GND</td>
<td>SYSEN#</td>
<td>WAKE#</td>
<td>ALERT#</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>PXI_TRIG3</td>
<td>PXI_TRIG4</td>
<td>PXI_TRIG5</td>
<td>GND</td>
<td>PXI_TRIG6</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>PXI_TRIG2</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_STAR</td>
<td>PXI_CLK10</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>PXI_TRIG1</td>
<td>PXI_TRIG0</td>
<td>RSV</td>
<td>GND</td>
<td>PXI_TRIG7</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_LBR6</td>
<td>GND</td>
<td>GND</td>
</tr>
</tbody>
</table>
## System Timing Slot Pinouts

### Table B-5. TP2 Connector Pinout for the System Timing Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PXIe_DSTARC0+</td>
<td>PXIe_DSTARC0−</td>
<td>GND</td>
<td>PXIe_DSTARC8+</td>
<td>PXIe_DSTARC8−</td>
<td>GND</td>
<td>PXIe_DSTARB8+</td>
<td>PXIe_DSTARB8−</td>
</tr>
<tr>
<td>2</td>
<td>PXIe_DSTARA0+</td>
<td>PXIe_DSTARA0−</td>
<td>GND</td>
<td>PXIe_DSTARC9+</td>
<td>PXIe_DSTARC9−</td>
<td>GND</td>
<td>PXIe_DSTARA9+</td>
<td>PXIe_DSTARA9−</td>
</tr>
<tr>
<td>3</td>
<td>PXIe_DSTARB0+</td>
<td>PXIe_DSTARB0−</td>
<td>GND</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>PXIe_DSTARA9+</td>
<td>PXIe_DSTARA9−</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>PXI_STAR0</td>
<td>PXI_STAR1</td>
<td>GND</td>
<td>PXI_STAR2</td>
<td>PXI_STAR3</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>PXI_STAR2</td>
<td>PXI_STAR3</td>
<td>GND</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>PXI_STAR4</td>
<td>PXI_STAR5</td>
<td>GND</td>
<td>NC</td>
<td>NC</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>NC</td>
</tr>
<tr>
<td>8</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>NC</td>
</tr>
<tr>
<td>9</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>NC</td>
</tr>
<tr>
<td>10</td>
<td>NC</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>NC</td>
<td>NC</td>
<td>GND</td>
<td>NC</td>
</tr>
</tbody>
</table>

### Table B-6. XP3 Connector Pinout for the System Timing Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PXIe_CLK100+</td>
<td>PXIe_CLK100−</td>
<td>GND</td>
<td>PXIe_SYNC100+</td>
<td>PXIe_SYNC100−</td>
<td>GND</td>
<td>PXIe_DSTARC+</td>
<td>PXIe_DSTARC−</td>
</tr>
<tr>
<td>2</td>
<td>PRSNT#</td>
<td>PWREN#</td>
<td>GND</td>
<td>PXIe_DSTARB+</td>
<td>PXIe_DSTARB−</td>
<td>GND</td>
<td>PXIe_DSTARA+</td>
<td>PXIe_DSTARA−</td>
</tr>
<tr>
<td>3</td>
<td>SMBDAT</td>
<td>SMBCLK</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
</tr>
<tr>
<td>4</td>
<td>MPWRGD*</td>
<td>PERST#</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
</tr>
<tr>
<td>5</td>
<td>1PETp0</td>
<td>1PETn0</td>
<td>GND</td>
<td>1Perp0</td>
<td>1Pern0</td>
<td>GND</td>
<td>1PETp1</td>
<td>1PETn1</td>
</tr>
<tr>
<td>6</td>
<td>1PETp2</td>
<td>1PETn2</td>
<td>GND</td>
<td>1Perp2</td>
<td>1Pern2</td>
<td>GND</td>
<td>1PETp3</td>
<td>1PETn3</td>
</tr>
<tr>
<td>7</td>
<td>1PETp3</td>
<td>1PETn3</td>
<td>GND</td>
<td>1Perp3</td>
<td>1Pern3</td>
<td>GND</td>
<td>1PETp4</td>
<td>1PETn4</td>
</tr>
<tr>
<td>8</td>
<td>1PETp5</td>
<td>1PETn5</td>
<td>GND</td>
<td>1Perp5</td>
<td>1Pern5</td>
<td>GND</td>
<td>1PETp7</td>
<td>1PETn7</td>
</tr>
<tr>
<td>9</td>
<td>1PETp6</td>
<td>1PETn6</td>
<td>GND</td>
<td>1Perp6</td>
<td>1Pern6</td>
<td>GND</td>
<td>1PETp7</td>
<td>1PETn7</td>
</tr>
<tr>
<td>10</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>1PETp7</td>
<td>1PETn7</td>
</tr>
</tbody>
</table>
Table B-7. XP4 Connector Pinout for the System Timing Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>GA4</td>
<td>GA3</td>
<td>GA2</td>
<td>GA1</td>
<td>GA0</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>5Vaux</td>
<td>GND</td>
<td>SYSEN#</td>
<td>WAKE#</td>
<td>ALERT#</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>12V</td>
<td>12V</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>3.3V</td>
<td>3.3V</td>
<td>3.3V</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>PXI_TRIG3</td>
<td>PXI_TRIG4</td>
<td>PXI_TRIG5</td>
<td>GND</td>
<td>PXI_TRIG6</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>PXI_TRIG2</td>
<td>GND</td>
<td>ATNLED</td>
<td>PXI_CLK10_IN</td>
<td>PXI_CLK10</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>PXI_TRIG1</td>
<td>PXI_TRIG0</td>
<td>ATNSW#</td>
<td>GND</td>
<td>PXI_TRIG7</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>PXIe_SYNC_CTRL</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_LBL6</td>
<td>PXI_LBR6</td>
<td>GND</td>
</tr>
</tbody>
</table>
### Peripheral Slot Pinouts

#### Table B-8. P1 Connector Pinout for the Peripheral Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>GND</td>
<td>5V</td>
<td>REQ64#</td>
<td>ENUM#</td>
<td>3.3V</td>
<td>5V</td>
<td>GND</td>
</tr>
<tr>
<td>24</td>
<td>GND</td>
<td>AD[1]</td>
<td>5V</td>
<td>V(I/O)</td>
<td>AD[0]</td>
<td>ACK64#</td>
<td>GND</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>SERR#</td>
<td>GND</td>
<td>3.3V</td>
<td>PAR</td>
<td>C/BE[1]#</td>
<td>GND</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>3.3V</td>
<td>IPMB_SCL</td>
<td>IPMB_SDA</td>
<td>GND</td>
<td>PERR#</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>DEVSEL#</td>
<td>GND</td>
<td>V(I/O)</td>
<td>STOP#</td>
<td>LOCK#</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>3.3V</td>
<td>FRAME#</td>
<td>IRDY#</td>
<td>BD_SEL#</td>
<td>TRDY#</td>
<td>GND</td>
</tr>
<tr>
<td>12–14</td>
<td></td>
<td>Key Area</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>C/BE[3]#</td>
<td>IDSEL</td>
<td>AD[23]</td>
<td>GND</td>
<td>AD[22]</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>REQ#</td>
<td>GND</td>
<td>3.3V</td>
<td>CLK</td>
<td>AD[31]</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>BRSPV1A5</td>
<td>BRSPV1B5</td>
<td>RST#</td>
<td>GND</td>
<td>GNT#</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>IPMB_PWR</td>
<td>HEALTHY</td>
<td>V(I/O)</td>
<td>INTP</td>
<td>INTS</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>INTA#</td>
<td>INTB#</td>
<td>INTC#</td>
<td>5V</td>
<td>INTD#</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>TCK</td>
<td>5V</td>
<td>TMS</td>
<td>TDO</td>
<td>TDI</td>
<td>GND</td>
</tr>
<tr>
<td>1</td>
<td>GND</td>
<td>5V</td>
<td>~12V</td>
<td>TRST#</td>
<td>+12V</td>
<td>5V</td>
<td>GND</td>
</tr>
</tbody>
</table>
### Table B-9. P2 Connector Pinout for the Peripheral Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>GND</td>
<td>GA4</td>
<td>GA3</td>
<td>GA2</td>
<td>GA1</td>
<td>GA0</td>
<td>GND</td>
</tr>
<tr>
<td>21</td>
<td>GND</td>
<td>PXI_LBR0</td>
<td>GND</td>
<td>PXI_LBR1</td>
<td>PXI_LBR2</td>
<td>PXI_LBR3</td>
<td>GND</td>
</tr>
<tr>
<td>20</td>
<td>GND</td>
<td>PXI_LBR4</td>
<td>PXI_LBR5</td>
<td>PXI_LBL0</td>
<td>GND</td>
<td>PXI_LBL1</td>
<td>GND</td>
</tr>
<tr>
<td>19</td>
<td>GND</td>
<td>PXI_LBL2</td>
<td>GND</td>
<td>PXI_LBL3</td>
<td>PXI_LBL4</td>
<td>PXI_LBL5</td>
<td>GND</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>PXI_TRIG3</td>
<td>PXI_TRIG4</td>
<td>PXI_TRIG5</td>
<td>GND</td>
<td>PXI_TRIG6</td>
<td>GND</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>PXI_TRIG2</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_STAR</td>
<td>PXI_CLK10</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>PXI_TRIG1</td>
<td>PXI_TRIG0</td>
<td>RSV</td>
<td>GND</td>
<td>PXI_TRIG7</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>PXI_BRSVA15</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_LBL6</td>
<td>PXI_LBR6</td>
<td>GND</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>13</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>V(I/O)</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>V(I/O)</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>10</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>V(I/O)</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>V(I/O)</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>V(I/O)</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>V(I/O)</td>
<td>64EN#</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>PXI_LBR7</td>
<td>GND</td>
<td>PXI_LBR8</td>
<td>PXI_LBR9</td>
<td>PXI_LBR10</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>PXI_LBR11</td>
<td>PXI_LBR12</td>
<td>UNC</td>
<td>PXI_LBL7</td>
<td>PXI_LBL8</td>
<td>GND</td>
</tr>
<tr>
<td>1</td>
<td>GND</td>
<td>PXI_LBL9</td>
<td>GND</td>
<td>PXI_LBL10</td>
<td>PXI_LBL11</td>
<td>PXI_LBL12</td>
<td>GND</td>
</tr>
</tbody>
</table>
## Hybrid Slot Pinouts

### Table B-10. P1 Connector Pinout for the Hybrid Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>GND</td>
<td>5V</td>
<td>REQ64#</td>
<td>ENUM#</td>
<td>3.3V</td>
<td>5V</td>
<td>GND</td>
</tr>
<tr>
<td>24</td>
<td>GND</td>
<td>AD[1]</td>
<td>5V</td>
<td>V(I/O)</td>
<td>AD[0]</td>
<td></td>
<td>ACK64#</td>
</tr>
<tr>
<td>18</td>
<td>GND</td>
<td>SERR#</td>
<td>GND</td>
<td>3.3V</td>
<td>PAR</td>
<td>C/BE[1]#</td>
<td>GND</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>3.3V</td>
<td>IPMB_SCL</td>
<td>IPMB_SDA</td>
<td>GND</td>
<td>PERR#</td>
<td>GND</td>
</tr>
<tr>
<td>16</td>
<td>GND</td>
<td>DEVSEL#</td>
<td>GND</td>
<td>V(I/O)</td>
<td>STOP#</td>
<td>LOCK#</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>3.3V</td>
<td>FRAME#</td>
<td>IRDY#</td>
<td>BD_SEL#</td>
<td>TRDY#</td>
<td>GND</td>
</tr>
</tbody>
</table>

### Key Area

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>GND</td>
<td>C/BE[3]#</td>
<td>IDSEL</td>
<td>AD[23]</td>
<td>GND</td>
<td>AD[22]</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>REQ#</td>
<td>GND</td>
<td>3.3V</td>
<td>CLK</td>
<td>AD[31]</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>BRSVP1A5</td>
<td>BRSVP1B5</td>
<td>RST#</td>
<td>GND</td>
<td>GNT#</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>IPMB_PWR</td>
<td>HEALTHY#</td>
<td>V(I/O)</td>
<td>INTP</td>
<td>INTS</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>INTA#</td>
<td>INTB#</td>
<td>INTC#</td>
<td>5V</td>
<td>INTD#</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>TCK</td>
<td>5V</td>
<td>TMS</td>
<td>TDO</td>
<td>TDI</td>
<td>GND</td>
</tr>
<tr>
<td>1</td>
<td>GND</td>
<td>5V</td>
<td>–12V</td>
<td>TRST#</td>
<td>+12V</td>
<td>5V</td>
<td>GND</td>
</tr>
</tbody>
</table>
### Table B-11. XP3 Connector Pinout for the Hybrid Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>A</th>
<th>B</th>
<th>ab</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
<th>ef</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>PXIe_CLK100+</td>
<td>PXIe_CLK100–</td>
<td>GND</td>
<td>PXIe_SYNC100+</td>
<td>PXIe_SYNC100–</td>
<td>GND</td>
<td>PXIe_DSTARC+</td>
<td>PXIe_DSTARC–</td>
</tr>
<tr>
<td>2</td>
<td>PRSNT#</td>
<td>PWREN#</td>
<td>GND</td>
<td>PXIe_DSTARB+</td>
<td>PXIe_DSTARB–</td>
<td>GND</td>
<td>PXIe_DSTARA+</td>
<td>PXIe_DSTARA–</td>
</tr>
<tr>
<td>3</td>
<td>SMRDAT</td>
<td>SMBCLK</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
</tr>
<tr>
<td>4</td>
<td>MPWRGD*</td>
<td>PERST#</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
</tr>
<tr>
<td>5</td>
<td>1PETp0</td>
<td>1PETn0</td>
<td>GND</td>
<td>1PERp0</td>
<td>1PERn0</td>
<td>GND</td>
<td>1PETp1</td>
<td>1PETn1</td>
</tr>
<tr>
<td>6</td>
<td>1PETp2</td>
<td>1PETn2</td>
<td>GND</td>
<td>1PERp2</td>
<td>1PERn2</td>
<td>GND</td>
<td>1PERp1</td>
<td>1PERn1</td>
</tr>
<tr>
<td>7</td>
<td>1PETp3</td>
<td>1PETn3</td>
<td>GND</td>
<td>1PERp3</td>
<td>1PERn3</td>
<td>GND</td>
<td>1PETp4</td>
<td>1PETn4</td>
</tr>
<tr>
<td>8</td>
<td>1PETp5</td>
<td>1PETn5</td>
<td>GND</td>
<td>1PERp5</td>
<td>1PERn5</td>
<td>GND</td>
<td>1PERp4</td>
<td>1PERn4</td>
</tr>
<tr>
<td>9</td>
<td>1PETp6</td>
<td>1PETn6</td>
<td>GND</td>
<td>1PERp6</td>
<td>1PERn6</td>
<td>GND</td>
<td>1PETp7</td>
<td>1PETn7</td>
</tr>
<tr>
<td>10</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>RSV</td>
</tr>
</tbody>
</table>

### Table B-12. XP4 Connector Pinout for the Hybrid Slot

<table>
<thead>
<tr>
<th>Pin</th>
<th>Z</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>D</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>GA4</td>
<td>GA3</td>
<td>GA2</td>
<td>GA1</td>
<td>GA0</td>
<td>GND</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>5Vaux</td>
<td>GND</td>
<td>SYSEN#</td>
<td>WAKE#</td>
<td>ALERT#</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>12V</td>
<td>12V</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>GND</td>
<td>GND</td>
<td>3.3V</td>
<td>3.3V</td>
<td>3.3V</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>PXI_TRIG3</td>
<td>PXI_TRIG4</td>
<td>PXI_TRIG5</td>
<td>PXI_TRIG6</td>
<td>GND</td>
<td>PXI_TRIG6</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
<td>PXI_TRIG2</td>
<td>GND</td>
<td>ATNLED</td>
<td>PXI_STAR</td>
<td>PXI_CLK10</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>PXI_TRIG1</td>
<td>PXI_TRIG0</td>
<td>ATNSW#</td>
<td>GND</td>
<td>PXI_TRIG7</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
<td>RSV</td>
<td>GND</td>
<td>RSV</td>
<td>PXI_LBL6</td>
<td>PXI_LBR6</td>
<td>GND</td>
</tr>
</tbody>
</table>
Log in to your National Instruments ni.com User Profile to get personalized access to your services. Visit the following sections of ni.com for technical support and professional services:

- **Support**—Technical support at ni.com/support includes the following resources:
  - **Self-Help Technical Resources**—For answers and solutions, visit ni.com/support for software drivers and updates, a searchable KnowledgeBase, product manuals, step-by-step troubleshooting wizards, thousands of example programs, tutorials, application notes, instrument drivers, and so on. Registered users also receive access to the NI Discussion Forums at ni.com/forums. NI Applications Engineers make sure every question submitted online receives an answer.
  - **Standard Service Program Membership**—This program entitles members to direct access to NI Applications Engineers via phone and email for one-to-one technical support, as well as exclusive access to eLearning training modules at ni.com/elearning. All customers automatically receive a one-year membership in the Standard Service Program (SSP) with the purchase of most software products and bundles including NI Developer Suite. NI also offers flexible extended contract options that guarantee your SSP benefits are available without interruption for as long as you need them. Visit ni.com/ssp for more information.

  For information about other technical support options in your area, visit ni.com/services, or contact your local office at ni.com/contact.

- **Training and Certification**—Visit ni.com/training for training and certification program information. You can also register for instructor-led, hands-on courses at locations around the world.
Appendix C  Technical Support and Professional Services

- **System Integration**—If you have time constraints, limited in-house technical resources, or other project challenges, National Instruments Alliance Partner members can help. To learn more, call your local NI office or visit ni.com/alliance.

- **Declaration of Conformity (DoC)**—A DoC is our claim of compliance with the Council of the European Communities using the manufacturer’s declaration of conformity. This system affords the user protection for electromagnetic compatibility (EMC) and product safety. You can obtain the DoC for your product by visiting ni.com/certification.

- **Calibration Certificate**—If your product supports calibration, you can obtain the calibration certificate for your product at ni.com/calibration.

You also can visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.
## Glossary

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Prefix</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>p</td>
<td>pico</td>
<td>$10^{-12}$</td>
</tr>
<tr>
<td>n</td>
<td>nano</td>
<td>$10^{-9}$</td>
</tr>
<tr>
<td>μ</td>
<td>micro</td>
<td>$10^{-6}$</td>
</tr>
<tr>
<td>m</td>
<td>milli</td>
<td>$10^{-3}$</td>
</tr>
<tr>
<td>k</td>
<td>kilo</td>
<td>$10^3$</td>
</tr>
<tr>
<td>M</td>
<td>mega</td>
<td>$10^6$</td>
</tr>
<tr>
<td>G</td>
<td>giga</td>
<td>$10^9$</td>
</tr>
<tr>
<td>T</td>
<td>tera</td>
<td>$10^{12}$</td>
</tr>
</tbody>
</table>

### Symbols

- °: Degrees.
- ≥: Equal or greater than.
- ≤: Equal or less than.
- %: Percent.

### A

- A: Amperes.
- AC: Alternating current.
- Auto: Automatic fan speed control.
- AWG: American Wire Gauge.
### Glossary

**B**

backplane  
An assembly, typically a printed circuit board, with connectors and signal paths that bus the connector pins.

BNC  
Bayonet Neill Concelman connector; a commonly used coaxial connector.

**C**

C  
Celsius.

cfm  
Cubic feet per minute.

CFR  
Code of Federal Regulations.

cm  
Centimeters.

CompactPCI  
An adaptation of the Peripheral Component Interconnect (PCI) Specification 2.1 or later for industrial and/or embedded applications requiring a more robust mechanical form factor than desktop PCI. It uses industry standard mechanical components and high-performance connector technologies to provide an optimized system intended for rugged applications. It is electrically compatible with the PCI Specification, which enables low-cost PCI components to be utilized in a mechanical form factor suited for rugged environments.

CSA  
Canadian Standards Association.

**D**

daisy-chain  
A method of propagating signals along a bus, in which the devices are prioritized on the basis of their position on the bus.

DB-9  
A 9-pin D-SUB connector.

DC  
Direct current.

DoC  
Declaration of Conformity.

D-SUB  
Subminiature D connector.
### Glossary

<table>
<thead>
<tr>
<th>Letter</th>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>E</strong></td>
<td>efficiency</td>
<td>Ratio of output power to input power, expressed as a percentage.</td>
</tr>
<tr>
<td></td>
<td>EIA</td>
<td>Electronic Industries Association.</td>
</tr>
<tr>
<td></td>
<td>EMC</td>
<td>Electromagnetic Compatibility.</td>
</tr>
<tr>
<td></td>
<td>EMI</td>
<td>Electromagnetic Interference.</td>
</tr>
<tr>
<td><strong>F</strong></td>
<td>FCC</td>
<td>Federal Communications Commission.</td>
</tr>
<tr>
<td></td>
<td>filler panel</td>
<td>A blank module front panel used to fill empty slots in the chassis.</td>
</tr>
<tr>
<td><strong>G</strong></td>
<td>g</td>
<td>(1) grams; (2) a measure of acceleration equal to 9.8 m/s².</td>
</tr>
<tr>
<td></td>
<td>GPIB</td>
<td>General Purpose Interface Bus (IEEE 488).</td>
</tr>
<tr>
<td></td>
<td>gRMS</td>
<td>A measure of random vibration. The root mean square of acceleration levels in a random vibration test profile.</td>
</tr>
<tr>
<td><strong>H</strong></td>
<td>hr</td>
<td>Hours.</td>
</tr>
<tr>
<td></td>
<td>Hz</td>
<td>Hertz; cycles per second.</td>
</tr>
<tr>
<td><strong>I</strong></td>
<td>IEC</td>
<td>International Electrotechnical Commission; an organization that sets international electrical and electronics standards.</td>
</tr>
<tr>
<td></td>
<td>IEEE</td>
<td>Institute of Electrical and Electronics Engineers.</td>
</tr>
<tr>
<td></td>
<td>IMP</td>
<td>Mainframe peak current.</td>
</tr>
<tr>
<td><strong>Glossary</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>----------------</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>in.</strong></td>
<td>Inches.</td>
<td></td>
</tr>
<tr>
<td><strong>inhibit</strong></td>
<td>To turn off.</td>
<td></td>
</tr>
<tr>
<td><strong>J</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>jitter</strong></td>
<td>A measure of the small, rapid variations in clock transition times from their nominal regular intervals. Units: seconds RMS.</td>
<td></td>
</tr>
<tr>
<td><strong>K</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>kg</strong></td>
<td>Kilograms.</td>
<td></td>
</tr>
<tr>
<td><strong>km</strong></td>
<td>Kilometers.</td>
<td></td>
</tr>
<tr>
<td><strong>L</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>lb</strong></td>
<td>Pounds.</td>
<td></td>
</tr>
<tr>
<td><strong>LED</strong></td>
<td>Light emitting diode.</td>
<td></td>
</tr>
<tr>
<td><strong>line regulation</strong></td>
<td>The maximum steady-state percentage that a DC voltage output will change as a result of a specified change in input AC voltage (step change from 90 to 132 VAC or 180 to 264 VAC).</td>
<td></td>
</tr>
<tr>
<td><strong>load regulation</strong></td>
<td>The maximum steady-state percentage that a DC voltage output will change as a result of a step change from no-load to full-load output current.</td>
<td></td>
</tr>
<tr>
<td><strong>M</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>m</strong></td>
<td>Meters.</td>
<td></td>
</tr>
<tr>
<td><strong>MHz</strong></td>
<td>Megahertz. One million Hertz; one Hertz equals one cycle per second.</td>
<td></td>
</tr>
<tr>
<td><strong>mi</strong></td>
<td>Miles.</td>
<td></td>
</tr>
<tr>
<td><strong>ms</strong></td>
<td>Milliseconds.</td>
<td></td>
</tr>
<tr>
<td><strong>MTBF</strong></td>
<td>Mean time between failure.</td>
<td></td>
</tr>
<tr>
<td><strong>MTTR</strong></td>
<td>Mean time to repair.</td>
<td></td>
</tr>
<tr>
<td><strong>N</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>----------</td>
<td>------------------------------------------------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>NEMA</td>
<td>National Electrical Manufacturers Association.</td>
<td></td>
</tr>
<tr>
<td>NI</td>
<td>National Instruments.</td>
<td></td>
</tr>
<tr>
<td><strong>P</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>power supply shuttle</td>
<td>A removable module that contains the chassis power supply.</td>
<td></td>
</tr>
<tr>
<td>PXI</td>
<td>PCI eXtensions for Instrumentation.</td>
<td></td>
</tr>
<tr>
<td>PXI_CLK10</td>
<td>10 MHz PXI system reference clock.</td>
<td></td>
</tr>
<tr>
<td><strong>R</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RH</td>
<td>Relative humidity.</td>
<td></td>
</tr>
<tr>
<td>RMS</td>
<td>Root mean square.</td>
<td></td>
</tr>
<tr>
<td><strong>S</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>s</td>
<td>Seconds.</td>
<td></td>
</tr>
<tr>
<td>skew</td>
<td>Deviation in signal transmission times.</td>
<td></td>
</tr>
<tr>
<td>slot blocker</td>
<td>An assembly installed into an empty slot to improve the airflow in adjacent slots.</td>
<td></td>
</tr>
<tr>
<td>standby</td>
<td>The backplane is unpowered (off), but the chassis is still connected to AC power mains.</td>
<td></td>
</tr>
</tbody>
</table>
| System controller | A module configured for installation in Slot 1 of a PXI chassis. This device is unique in the PXI system in that it performs the system controller functions, including clock sourcing and arbitration for data transfers across the backplane. Installing such a device into any other slot can damage the device, the PXI backplane, or both.
### Glossary

**system reference clock**
A 10 MHz clock, also called PXI_CLK10, that is distributed to all peripheral slots in the chassis, as well as a BNC connector on the rear of chassis labeled 10 MHz REF OUT. The system reference clock can be used for synchronization of multiple modules in a measurement or control system. The 10 MHz REF IN and OUT BNC connectors on the rear of the chassis can be used to synchronize multiple chassis to one reference clock. The PXI backplane specification defines implementation guidelines for PXI_CLK10.

**System Timing slot**
This slot is located at slot 4 and has dedicated trigger lines to other slots.

**T**

TTL
Transistor-transistor logic.

**U**

UL
Underwriter's Laboratories.

**V**

V
Volts.

VAC
Volts alternating current.

$V_{PP}$
Peak-to-peak voltage.

**W**

W
Watts.
Index

A
AC power cables (table), 1-2

B
backplane
  hybrid peripheral slots, 1-7
  interoperability with CompactPCI, 1-6
  overview, 1-6
  PXI local bus, routing, 1-9
  PXI peripheral slots, 1-8
  PXIe_SYNC_CTRL, 1-13, 1-14
  specifications, A-7
  system controller slot, 1-7
  system reference clock, 1-10
    default behavior (figure), 1-12
    routing (figure), 1-11
  system timing slot, 1-8
  trigger bus, 1-10

C
cables, power (table), 1-2
  calibration certificate (NI resources), C-2
  CE compliance specifications, A-6
  chassis ambient temperature definitions, 2-5
  chassis cooling considerations
    ambient temperature definitions, 2-5
    clearances, 2-2
    figure, 2-3
    vents (figure), 2-4
  chassis initialization file, 2-16
  chassis ventilation (figure), 2-4
  cleaning fan filters, 3-1
  clearances for chassis cooling, 2-2
    figure, 2-3
  CLK10 rear connectors, 2-13

CompactPCI
  interoperability with NI PXIe-1062Q
    backplane, 1-6
  configuration in MAX (figure), 2-14
  configuration. See installation, configuration, and operation
  connector pinouts. See pinouts
  conventions used in the manual, vii
  cooling
    air cooling of an NI PXIe-1062Q
    chassis, 2-2
    filler panel installation, 2-5
    setting fan speed, 2-5
    slot blocker installation, 2-5

D
DB-9 connector
  pinout (table), 2-11
  power supply voltages (table), 2-12
  Declaration of Conformity (NI resources), C-2
  diagnostic tools (NI resources), C-1
  dimensions (figure), A-12, A-13
  documentation
    conventions used in manual, vii
    NI resources, C-1
    related documentation, viii
    drivers (NI resources), C-1

E
electromagnetic compatibility, A-6
  EMC filler panel kit, 1-6
  examples (NI resources), C-1
  external clock source specifications, A-9
Index

F
fan, setting speed, 2-5
filler panel installation, 2-5

G
ground, connecting, 2-6

H
help, technical support, C-1
hybrid peripheral slots, description, 1-7
hybrid slot pinouts
   P1 connector (table), B-8
   XP3 connector (table), B-9
   XP4 connector (table), B-9

I
IEC 320 inlet, 1-5, 2-6
inhibit mode switch, 2-13
installation, configuration, and operation
   chassis initialization file, 2-16
   configuration in MAX (figure), 2-14
   connecting safety ground, 2-6
   filler panel installation, 2-5
   installing a PXI Express system controller, 2-7
      figure, 2-7
   module installation
      CompactPCI or PXI modules (figure), 2-10
   peripheral module installation, 2-9
      figure, 2-10
   PXI Express configuration in MAX, 2-14
   PXI Express system controller installed in a NI PXIe-1062Q chassis (figure), 2-8
   PXI-1 configuration in MAX, 2-15
   rack mounting, 2-5
   remote voltage monitoring and inhibiting interface, 2-11
   setting fan speed, 2-5
   site considerations, 2-2
   slot blocker installation, 2-5
   testing power up, 2-6
   unpacking the NI PXIe-1062Q, 1-1
   installing a PXI Express system controller (figure), 2-7
   instrument drivers (NI resources), C-1
   interoperability with CompactPCI, 1-6

K
key features, 1-2
kit contents, 1-1
KnowledgeBase, C-1

L
local bus, routing (figure), 1-10

M
maintenance of NI PXIe-1062Q chassis, 3-1
   cleaning
      exterior cleaning, 3-2
      fan filters, 3-2
      interior cleaning, 3-2
   preparation, 3-1
   resetting the AC mains circuit breaker, 3-2
   service interval, 3-1
   static discharge damage (caution), 3-1
Index

N

National Instruments support and services, C-1
NI PXIe-1062Q
  fan speed, setting, 2-5
  front view (figure), 1-4
  installation. See installation, configuration, and operation key features, 1-2
  maintenance. See maintenance of NI PXIe-1062Q chassis
optional equipment, 1-6
rack mounting, 2-5
rear view of NI PXIe-1062Q chassis, 1-5
safety ground, connecting, 2-6
unpacking, 1-1
NI PXIe-1062Q backplane
  hybrid peripheral slots, 1-7
  interoperability with CompactPCI, 1-6
  overview, 1-6
  PXI local bus, routing, 1-9
  PXI peripheral slots, 1-8
  PXIe_SYNC_CTRL, 1-13
    using as restart (figure), 1-14
  specifications, A-7
  system controller slot, 1-7
  system reference clock, 1-10
    default behavior (figure), 1-12
    routing (figure), 1-11
  system timing slot, 1-8
  trigger bus, 1-10
NI support and services, C-1

O

optional equipment, 1-6

P

peripheral module installation, 2-9
  figure, 2-10
peripheral slot pinouts
  P1 connector (table), B-6
  P2 connector (table), B-7
pinouts, B-1
  DB-9 connector (table), 2-11
power cables (table), 1-2
power inhibit switch LED indicator, 2-10
power supply
  connecting to, 2-6
  remote voltage monitoring and inhibiting interface, 2-11
  replacing, 3-3
    configuration, 3-4
    connecting safety ground, 3-4
    connecting to power source, 3-4
    installation, 3-4
    removal, 3-3
  voltages at voltage monitoring connector (DB-9) (table), 2-11
power up, testing, 2-6
programming examples (NI resources), C-1
PXI differential star trigger specifications (PXIe-DSTARA, PXIe-DSTAR, PXIe-DSTARC), A-10
PXI Express configuration in MAX, 2-14
PXI Express system controller, 2-7
  figure, 2-7
  installing in a NI PXIe-1062Q chassis (figure), 2-8
PXI local bus, routing, 1-9
PXI peripheral slots, description, 1-8
PXI star trigger specifications, A-9
PXI star, routing, 1-9
PXI-1 configuration in MAX, 2-15
PXIe_DSTAR, routing, 1-9
PXIe_SYNC_CTRL, 1-13
  specifications, A-9
  using as restart (figure), 1-14
Index

R
rack mount kit dimensions (figure), A-14
rack mounting, 2-5
  kit, 1-6
related documentation, viii
remote voltage monitoring and inhibiting interface, 2-11
replacing the power supply, 3-3

S
safety and caution notices, 2-1
safety specifications, A-6
service interval, 3-1
setting fan speed, 2-5
slot blocker
  installation, 2-5
  kit, 1-6
software (NI resources), C-1
specifications
  acoustic emissions
    sound power, A-5
    sound pressure level (at operator position), A-5
backplane
  10 MHz system reference clock
    (PXI_CLK10), A-8
  100 MHz Reference Out BNC, A-9
  100 MHz system reference clock
    (PXIe_CLK100 and PXIe_SYNC100), A-8
CE compliance, A-6
chassis cooling, A-4
dimensions (figure), A-12, A-13
electrical
  AC input, A-1
  DC output, A-2
electromagnetic compatibility, A-6
environmental
  operating environment, A-4
  storage environment, A-5
  external clock source, A-9
  mechanical, A-10
  PXI differential star triggers
    (PXIe-DSTARA, PXIe-DSTARBB, PXIe-DSTARC), A-10
  PXI star trigger, A-9
  PXIe_SYNC_CTRL, A-9
rack mount kit dimensions (figure), A-14
  safety, A-6
  shock and vibration, A-5
  system reference clocks, A-8
static discharge damage (caution), 3-1
support, technical, C-1
system controller slot
  description, 1-7
  pinouts
    XP1 connector (table), B-2
    XP2 connector (table), B-2
    XP3 connector (table), B-3
    XP4 connector (table), B-3
system reference clock, 1-10
  default behavior (figure), 1-12
  routing (figure), 1-11
  specifications, A-8
system timing slot
  description, 1-8
  pinouts
    TP2 connector (table), B-4
    XP3 connector (table), B-4
    XP4 connector (table), B-5

T
technical support, C-1
testing power up, 2-6
training and certification (NI resources), C-1
trigger bus, 1-10
troubleshooting (NI resources), C-1
U
unpacking the NI PXIe-1062Q chassis, 1-1

V
voltage monitoring connector. See DB-9 connector
voltages at voltage monitoring connector (DB-9) (table), 2-12

W
Web resources, C-1