LabVIEW™ FPGA Module Release and Upgrade Notes

Version 8.0

These release notes contain instructions for installing the LabVIEW FPGA Module, introduce new features, and provide upgrade information. Refer to the resources listed at the end of this document for information about developing applications with the FPGA Module.

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System Requirements

The *development computer* is a PC or PXI system running Windows and on which you install the LabVIEW development system and the FPGA Module. You create and edit FPGA VIs and host VIs on the development computer. The development computer must meet the following requirements to run the FPGA Module.

- Windows 2000/XP
- 1.2 GHz Pentium processor or equivalent
- 512 MB memory for 1 million gate FPGA targets; 2 GB memory for 3 million gate FPGA targets
- 2.5 GB additional available disk space
- LabVIEW 8.0 Full or Professional Development System

You also must have an *FPGA target*. The FPGA target is the hardware on which the FPGA VI runs, such as an NI Reconfigurable I/O device. You can develop an FPGA VI without an FPGA target, but you cannot run the FPGA VI without an FPGA target.

Installing the LabVIEW FPGA Module

Complete the following steps to set up a development computer with LabVIEW, the LabVIEW Real-Time (RT) Module (optional), the FPGA Module, and the appropriate NI device drivers.

1. Log in to the development computer as an administrator or as a user with administrative privileges.
2. Install LabVIEW 8.0 from the LabVIEW 8.0 installation CD. Refer to the *LabVIEW Release Notes* for information about installing the LabVIEW development system.

Note The LabVIEW installer prompts you to insert the NI Device Drivers CD to install certain device drivers. If you plan to install the LabVIEW Real-Time Module, wait until after step 3 to install the NI Device Drivers CD.

3. (Optional) Install the LabVIEW Real-Time Module from the LabVIEW Real-Time Module 8.0 installation CD. Refer to the *LabVIEW Real-Time Module Release and Upgrade Notes* for information about installing the RT Module and the device drivers you need and for information about configuring RT targets.

4. Install the FPGA Module from the LabVIEW FPGA Module 8.0 installation CD, following the instructions that appear on the screen. Select **Complete** when you reach the **Select Installation Type** step. By default, the FPGA Module installer attempts to install NI-RIO and prompts you to insert the NI-RIO CD. Install NI-RIO if it is the appropriate driver software for the FPGA target you use.

   The FPGA Module installs program files and documentation and copies files from Xilinx ISE to the *x*:\NIFPGA80 directory, where *x* is the drive on which you installed LabVIEW 8.0. Xilinx ISE is third-party software that the FPGA Module uses to compile FPGA VIs into code that runs on the FPGA target.

5. (Optional) Install NI device drivers available on the NI Device Drivers CD.

Note The NI Device Drivers CD might not include drivers for the FPGA target you use. If the NI Device Drivers CD does not include the driver for the FPGA target you use, install FPGA target drivers from the CDs available with the targets in step 6.

6. (Optional) Install the appropriate drivers and FPGA Module support files for the FPGA target you will use. Refer to the specific hardware documentation for information about the appropriate drivers and for information about installing and configuring the FPGA target.

LabVIEW FPGA Module 8.0 Features

The FPGA Module 8.0 includes the following new features to help you better manage and implement the components of an FPGA application: FPGA targets, FPGA VIs, host VIs, and target-specific options. The *FPGA VI* is the VI you create to run on an FPGA target and define the functionality of the target. The *host VI* is the VI you create to run in Windows or on an RT target and communicate with the FPGA VI on the FPGA target. You can run only one FPGA VI on an FPGA target at a time.

Refer to the *LabVIEW Help*, available by selecting **Help»Search the LabVIEW Help**, for more information about the new features.

Managing FPGA Targets and VIs in LabVIEW Projects

LabVIEW 8.0 features the new **Project Explorer** window and the LabVIEW project to manage applications that include multiple VIs and resources, such as FPGA targets. The FPGA Module 8.0 uses the **Project Explorer** window to manage the components of an FPGA application, including FPGA VIs, host VIs, FPGA targets, and target-specific options, such as FPGA I/O, FPGA FIFOs, and FPGA clocks. The **Project Explorer**

window surpasses the functionality of the **Embedded Project Manager** window in the FPGA Module 1.1. You now can manage all the components of an FPGA application, including FPGA VIs and host VIs, in a single project.

Note You must create projects to create FPGA VIs. Click the **Empty Project** link in the **Getting Started** window to create an empty project. Use the Real-Time Project Wizard, available by selecting **Real-Time Project** from the **Targets** pull-down menu in the **Getting Started** window, if you want to create a new project that includes an RT target and VIs ready to deploy to the RT target. You then can right-click **My Computer** or the RT target in the **Project Explorer** window and select **New»Targets and Devices** from the shortcut menu to add an FPGA target to the project.

Adding I/O to the Project

You can add FPGA I/O to a project by right-clicking an FPGA target in the **Project Explorer** window and selecting **New»FPGA I/O** from the shortcut menu. You can determine the I/O resources on the FPGA target that you want to use, and you then can assign unique names to the I/O resources you use.

To use the FPGA I/O you configure in the **Project Explorer** window in an FPGA VI, first place an FPGA I/O Node on the block diagram of an FPGA VI under the same FPGA target in the **Project Explorer** window. To configure the FPGA I/O Node to perform the I/O operations you created in the **Project Explorer** window, click the I/O Name terminal in the FPGA I/O Node and select an I/O resource you configured from the shortcut menu. You also can drag an FPGA I/O item from the **Project Explorer** window onto the block diagram to drop a configured FPGA I/O Node on the block diagram. You no longer need to select from a few pre-defined FPGA Device I/O functions on the palette.

Tip Some I/O resources, such as digital input/output lines, allow you to change read or write behavior from the shortcut menu of the FPGA I/O Node. Right-click the FPGA I/O Node after you configure it for digital input or output and select **Change to Write** from the shortcut menu if you want to write to the I/O resource or **Change to Read** from the shortcut menu if you want to read the I/O resource.

You can put inputs and outputs, analog and digital, all in the same node on the block diagram. You can set target-specific properties and call methods on the FPGA I/O items with the FPGA I/O Property Node and the FPGA I/O Method Node, respectively. Some FPGA targets allow you to select I/O, PXI, and RTSI resources. Other FPGA targets allow you to select resources in the FPGA on the device that provide fixed features designed by National Instruments. Refer to the specific FPGA target hardware documentation for more information.

Using Direct Memory Access with FPGA FIFO Functions

The FPGA Module 8.0 includes direct memory access (DMA) support with the new DMA transfer type of the FPGA FIFO functions. Use the DMA FIFOs to transfer large amounts of data quickly from the FPGA target to the host computer.

Create DMA FIFOs for the FPGA VI in the **Project Explorer** window by right-clicking the FPGA target and selecting **New»FIFO** from the shortcut menu. In the **FPGA FIFO Properties** dialog box that appears, select **DMA** from the **Type** pull-down menu. You then can use the FPGA FIFO functions in the FPGA VI. Retrieve data from the DMA FIFO in the host VI with the Invoke Method function calling one of the DMA FIFO methods. You cannot write data to the DMA FIFOs from the host VI.

Note Some targets might not support the DMA FIFOs. Refer to the specific hardware documentation for information about supported features.

Using Multiple Clock Domains

The FPGA Module 8.0 allows multiple clocks within a single FPGA VI. In the FPGA Module 1.1, you can use only one global clock. You now can use multiple clocks to partition an FPGA VI into sections of code that run at different clock rates. You can use higher clock rates for applications such as pulse width measurement and pulse generation where the speed of the loop directly impacts the resolution of the measurement or generation.

All FPGA targets include an FPGA base clock in the **Project Explorer** window. You also can create derived clocks by right-clicking the base clock and selecting **New FPGA Derived Clock** from the shortcut menu. You also can specify that a single-cycle Timed Loop use a clock you created as the timing source in the **Configure Timed Loop** dialog box, available by double-clicking the Input Node of the Timed Loop. To set a top-level clock for the FPGA VI, right-click the FPGA target in the **Project Explorer** window and select **Properties** from the shortcut menu. Then select the **Top-Level Clock** category and select a clock from the **Configured Clock** list.

Note Support for multiple clock domains varies by FPGA target. Refer to the specific FPGA target hardware documentation for information about multiple clock domain support and usage.

Saving the Compiled FPGA Code in a Separate File

LabVIEW now saves the code generated during compilation of an FPGA VI, or *bitfile*, in a file separate from the FPGA VI. You can open a reference to a specific bitfile from host VIs with the Open FPGA VI Reference function for Programmatic FPGA Interface Communication. If you do not have the FPGA Module, you must open a reference to the specific bitfile.

Note National Instruments recommends you open a reference to the FPGA VI rather than a specific bitfile for most applications. You must include the host VI in the same LabVIEW project as the FPGA VI if you open a reference to an FPGA VI. If you open a reference to a bitfile, you do not need to include the host VI in a project.

Binding FPGA VI Reference Out Parameters to Type Definitions

In the FPGA Module 1.*x*, you cannot bind the **FPGA VI Reference Out** parameter of the Open FPGA VI Reference or Up Cast function to type definitions, which makes it difficult to use subVIs in the host VI. You now can bind the **FPGA VI Reference Out** parameter of the Open FPGA VI Reference or Up Cast function to type definitions so that LabVIEW automatically propagates configuration changes to subsequent subVIs in the data flow.

Note Some targets might not support the Up Cast function. Refer to the specific FPGA target hardware documentation for information about supported features.

Using Interactive Front Panel Communication and FPGA Target Emulators

The FPGA Module 8.0 supports many new National Instruments hardware targets. All NI FPGA targets include support for Programmatic FPGA Interface Communication. Some FPGA targets also include support for Interactive Front Panel Communication. A subset of the FPGA targets that support Interactive Front Panel Communication include support for FPGA target emulators. Refer to the specific target hardware documentation for information about whether the target supports Interactive Front Panel Communication or an FPGA target emulator.

If the target supports an FPGA target emulator, you can specify that VIs under the target in the **Project Explorer** window run with the FPGA target emulator in the **FPGA Target Properties** dialog box, available by right-clicking the FPGA target in the **Project Explorer** window and selecting **Properties** from the shortcut menu.

Programmatically Aborting and Resetting FPGA VIs

In the FPGA Module 1.*x*, LabVIEW aborts and resets the FPGA VI when you use the Invoke Method function with the Abort method in the host VI. In the FPGA Module 8.0, LabVIEW only aborts the FPGA VI without resetting the FPGA VI when you use the Invoke Method function with the Abort method. You must use the Invoke Method function with the new Reset method if you want to abort and reset the FPGA VI.

Upgrading to the LabVIEW FPGA Module 8.0

This section describes upgrade and compatibility issues for the FPGA Module 8.0.

Refer to `ni.com/info` and enter the info code `ex8kk4` for more information about how to perform FPGA Module 1.*x* tasks with the FPGA Module 8.0.

FPGA Device I/O Functions

The FPGA Module no longer supports the FPGA Device I/O functions. Use the FPGA I/O Node configured to target-specific I/O resources instead.

Embedded Project Manager

The FPGA Module no longer supports the Embedded Project Manager. Use the **Project Explorer** window instead.

Upgrading FPGA VIs, Host VIs, and Embedded Projects from the LabVIEW FPGA Module 1.*x* to 8.0

If you created FPGA VIs or host VIs using LabVIEW 7.*x* and the FPGA Module 1.*x*, you can update the VIs for use with LabVIEW 8.0 and the FPGA Module 8.0. Complete the following steps to update the VIs for use with LabVIEW 8.0 and the FPGA Module 8.0.

Note NI recommends you back up your files before you begin updating them for use with the FPGA Module 8.0.

1. Launch LabVIEW 8.0.
2. Select **Tools»FPGA Module»Import FPGA Files from LabVIEW FPGA Module 1.X** in the **Getting Started** window or in the **Project Explorer** window of an open project to launch the **Import FPGA Files from LabVIEW FPGA Module 1.X** utility. If you do not have a project open, LabVIEW prompts you to create a new project.

- Upgrading from the FPGA Module 1.1 only.

  3. Complete the following steps to add the LEP file you want to import to the **LabVIEW Embedded Project (*.lep) Files** list.
     a. Click the **Add** button below the **LabVIEW Embedded Project (*.lep) Files** list. The **Select an Embedded Project to Add** dialog box appears.
     b. Navigate to the location of the LEP file you want to import.
     c. Click the **Add** button. LabVIEW adds the LEP file and all the VIs associated with the LEP file to the **Import FPGA Files from LabVIEW FPGA Module 1.X** utility. You can see only the LEP file in the **LabVIEW Embedded Project (*.lep) Files** list.
     d. Proceed to step 5.

- Upgrading from the FPGA Module 1.0 only.

  4. Complete the following steps to add the FPGA VIs you want to import to the **FPGA 1.0 VIs** list.
     a. Click the **Add** button below the **FPGA 1.0 VIs** list. The **Select a VI to Add** dialog box appears.
     b. Navigate to the location of the FPGA VI you want to import.
     c. Click the **Add** button. LabVIEW adds the FPGA VI to the **Import FPGA Files from LabVIEW FPGA Module 1.X** utility.
     d. Proceed to step 5.
  5. Add host VIs from the FPGA Module 1.*x* you want to import to the **Host VIs** list.
  6. Click the **Continue** button. The **Import Status** dialog box appears. When LabVIEW finishes importing the 1.*x* files, the **Save VIs** dialog box appears.
  7. Select a location in the **Save Location** section to save the imported VIs. Select **Next to Project** if you want to save the new VIs in the same location as the new project. National Instruments recommends this option. Select **Choose a Location** if you want to specify a different location. Select **Defer Decision - Leave VIs open in memory** if you want to wait until later to save the VIs.
  8. If you select **Choose a Location** or **Next to Project** and you have not saved the project, click the **Continue** button. If you select **Choose a Location**, the **Location to Save** dialog box appears. If you select **Next to Project**, the **Name the Project** dialog box appears. Proceed to step 9.

     If you have saved the project or if you select **Defer Decision - Leave VIs open in memory**, click the **Finish** button. LabVIEW returns you to the project. If you select **Defer Decision - Leave VIs open in memory**, LabVIEW also opens the front panels of the top-level VIs.

9. If you have the **Location to Save** dialog box open, choose an existing folder or create a new folder in which to save the new project and click the **Save** button. If you have the **Name the Project** dialog box open, type a name for the new LabVIEW project file (`.lvproj`) and click the **Save** button to save the new project.

The project file now includes all the VI and I/O information, as well as the FPGA target(s) on which the FPGA VI runs.

Where to Go from Here

National Instruments provides many resources to help you succeed with your NI products. Use the following resources as you start exploring LabVIEW and the FPGA Module.

Examples

The driver software for many FPGA targets includes corresponding examples. Refer to the specific hardware documentation for information about whether the FPGA target you use comes with corresponding examples.

You can start with an existing example and use it as a framework for developing FPGA VIs and host VIs. From LabVIEW, launch the NI Example Finder by selecting **Help»Find Examples**. Browse the examples by directory or by task.

Related Documentation

Refer to the *LabVIEW Help* for information about LabVIEW and the FPGA Module, and refer to the **Context Help** window for information about using VIs and functions.

- *LabVIEW Help*—Available by selecting **Help»Search the LabVIEW Help**. Browse the **FPGA Module** book in the **Contents** tab for an overview of the FPGA Module and hardware-specific information included in the *LabVIEW Help*. Browse the **FPGA Interface** book in the **Contents** tab for an overview of the FPGA Interface information included in the *LabVIEW Help*.
- **Context Help** window—Available by selecting **Help»Show Context Help**.

Refer to the specific hardware documentation for information about using the FPGA target with LabVIEW and the FPGA Module and for information about hardware specifications.

NI Web Site

Visit ni.com/fpga for the latest NI Developer Zone articles, examples, and support information for the FPGA Module.

Known Issues

Refer to readme_FPGA.html on the LabVIEW FPGA Module CD for information about known issues with the FPGA Module. You also can find the readme_FPGA.html file installed in the LabVIEW 8.0\readme directory. Select **Start»All Programs»National Instruments» LabVIEW 8.0»Readme** to open the LabVIEW 8.0\readme directory.

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