NI 6731/6733 Specifications

This document lists the specifications for the NI 6731/6733 analog output devices. The following specifications are typical at 25 °C unless otherwise noted.

Note With NI-DAQmx, National Instruments has revised its terminal names so they are easier to understand and more consistent among NI hardware and software products. The revised terminal names used in this document are usually similar to the names they replace. For a complete list of Traditional NI-DAQ terminal names and their NI-DAQmx equivalents, refer to the Terminal Name Equivalents section of Chapter 2, I/O Connector, of the Analog Output Series User Manual.

Analog Output

Output Characteristics

Number of channels
- NI 6731 ....................................... 4 voltage outputs
- NI 6733 ....................................... 8 voltage outputs

Resolution ....................................... 16 bits, 1 in 65,536

Max update rate

<table>
<thead>
<tr>
<th>Number of Channels</th>
<th>Max Update Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Using Local FIFO (kS/s)†</td>
</tr>
<tr>
<td>1</td>
<td>1,000</td>
</tr>
<tr>
<td>2</td>
<td>1,000</td>
</tr>
<tr>
<td>3</td>
<td>1,000</td>
</tr>
<tr>
<td>4</td>
<td>1,000</td>
</tr>
<tr>
<td>5</td>
<td>1,000</td>
</tr>
<tr>
<td>6</td>
<td>952</td>
</tr>
</tbody>
</table>

* These numbers apply to continuous waveform generation, which allows for the time it takes to reset the FIFO to the beginning when cycling through it. This additional time, about 200 ns, is not incurred when using host PC memory for waveform generation. Max update rate in FIFO mode does not change regardless of the number of devices in the system.

† These results were measured using a PCI-6711/6713 device with a 90 MHz Pentium machine. These numbers may change when using more devices or when other CPU or bus activity occurs.

Max Update Rate

<table>
<thead>
<tr>
<th>Number of Channels</th>
<th>Max Update Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Using Local FIFO (kS/s)†</td>
</tr>
<tr>
<td>7</td>
<td>833</td>
</tr>
<tr>
<td>8</td>
<td>740</td>
</tr>
</tbody>
</table>

- Type of DAC: Double-buffered, multiplying
- FIFO buffer size
  - NI 6731: 8,192 samples
  - NI 6733: 16,384 samples
- DMA channels: 3
- Data transfers: DMA, interrupts, programmed I/O
- DMA modes: Scatter-gather
### Accuracy Information

<table>
<thead>
<tr>
<th>Nominal Range at Full Scale (V)</th>
<th>Absolute Accuracy</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>% of Reading</td>
</tr>
<tr>
<td></td>
<td>24 Hours</td>
</tr>
<tr>
<td>±10</td>
<td>0.0044%</td>
</tr>
</tbody>
</table>

Absolute accuracy = (% of Reading × Voltage) + Offset + (Temp Drift × Voltage)

**Note:** Temp drift applies only if ambient is greater than ±10 °C of previous external calibration.

### Transfer Characteristics

Relative accuracy (INL)
- After calibration: ±2.2 LSB max
- Before calibration: ±2.2 LSB max

DNL
- After calibration: ±1.0 LSB max
- Before calibration: ±1.0 LSB max

Monotonicity: 16 bits guaranteed after calibration

Offset error
- After calibration: ±168 μV max
- Before calibration: ±40 mV max

Gain error (relative to internal reference)
- After calibration: ±30 ppm of output max
- Before calibration: ±9,000 ppm of output max

Gain error (relative to external reference)
- ±0.1% of output max, not adjustable

### Voltage Output

Ranges: ±10 V, ±EXT REF

Output coupling: DC

Output impedance: 0.1 Ω max

Current drive: ±5 mA max

Output stability: Any passive load, up to 1,500 pF

Protection: Short-circuit to ground

Power-on state: 0 V (±200 mV)

### External Reference Input

Range: ±11 V

Overvoltage protection: ±25 V powered on, ±15 V powered off

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Figure 1. Scaling Attenuation versus External Reference Frequency

Figure 2. AO External Reference THD versus External Reference Frequency
Dynamic Characteristics

Slew rate .......................... 15 V/μs
Noise ...................................... 80 μVrms, DC to 1 MHz
Channel crosstalk ....................... –95 dB with SH68-68-EP
cable (generating a 10 V, 10 point sinusoidal at 100 kHz on the reference
channel)
Settling time .......................... 2.8 μs to ±1.0 LSB
Accuracy
Total harmonic distortion .............. –90 dB typ (generating a
10 V, 1,000 point, 750 Hz
sine wave, summing
9 harmonics)

Stability
Offset temperature coefficient ...... ±35 μV/°C
Gain temperature coefficient
Internal reference ...................... ±6.5 ppm/°C
External reference ..................... ±5.0 ppm/°C
Onboard calibration reference
Level ........................................ 5,000 V (1.0 mV) (actual
value stored in EEPROM)
Temperature coefficient .......... ±0.6 ppm/°C max
Long-term stability ................. ±15 ppm/√h

Digital I/O

Number of channels .................. 8 input/output
Compatibility ......................... TTL/CMOS

Digital logic levels

<table>
<thead>
<tr>
<th>Level</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input low voltage</td>
<td>0 V</td>
<td>0.8 V</td>
</tr>
<tr>
<td>Input high voltage</td>
<td>2.0 V</td>
<td>5.0 V</td>
</tr>
<tr>
<td>Input low current (Vin = 0 V)</td>
<td>—</td>
<td>–320 μA</td>
</tr>
<tr>
<td>Input high current (Vin = 5 V)</td>
<td>—</td>
<td>10 μA</td>
</tr>
<tr>
<td>Output low voltage (IOL = 24 mA)</td>
<td>—</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Output high voltage (IOH = –13 mA)</td>
<td>4.35 V</td>
<td>—</td>
</tr>
</tbody>
</table>

Power-on state ....................... Input (high-impedance)
Data transfers ........................... DMA, interrupts,
programmed I/O
Input buffer .......................... 2,000 bytes

Timing I/O

Number of channels .................. 2 up/down
Counter/timers ....................... 24 bits
Frequency scaler .................... 4 bits
Compatibility .......................... TTL/CMOS
Base clocks available
Counter/timers ....................... 20 MHz, 100 kHz
Frequency scaler .................... 10 MHz, 100 kHz
Base clock accuracy .................. ±0.01% over operating
temperature
Max source frequency .................. 20 MHz
Min source pulse duration .......... 10 ns, edge-detect mode
Min gate pulse duration .......... 10 ns, edge-detect mode
Data transfers .......................... DMA, interrupts,
programmed I/O
DMA modes .......................... Scatter-gather

Triggers

Digital Trigger
Purpose
Analog output .................. Start trigger, gate, clock
Counter/timers .................. Source, gate
Source .......................... PFI <0..9>
Compatibility .................. TTL
Response .......................... Rising or falling edge
Pulse width .......................... 10 ns min

RTSI Bus (PCI Only)
Trigger lines <0..6> ............... 7
RTSI clock .......................... 1

PXI Trigger Bus (PXI Only)
Trigger lines <0..5> ............... 6
Star trigger .................. 1
Clock .......................... 1
Bus Interface
NI PCI-6731/6733 .................................................. 5 V PCI master, slave
NI PXI-6733 .......................................................... PXI/CompactPCI master, slave

Power Requirement
NI 6731
+5 VDC (±5%) ........................................... 0.80 A typ, 1.25 A max
+3.3 VDC (±5%) ........................................... 125 mA typ, 250 mA max
Power available at I/O connector ......................... +4.65 to +5.25 VDC at 1 A

NI 6733
+5 VDC (±5%) ........................................... 1.25 A typ, 1.8 A max
+3.3 VDC (±5%) ........................................... 125 mA typ, 250 mA max
Power available at I/O connector ......................... +4.65 to +5.25 VDC at 1 A

Physical
Dimensions (not including connectors)
NI PCI-6731/6733 ............................................. 17.5 × 10.7 cm (6.87 × 4.2 in.)
NI PXI-6733 ................................................... 16 × 10 cm (6.3 × 3.9 in.)
I/O connector .................................................. 68-pin male SCSI-II type

Maximum Working Voltage
Maximum working voltage refers to the signal voltage plus the common-mode voltage.
Channel-to-earth ............................................ ±11 V, Installation Category I
Channel-to-channel ........................................ ±22 V, Installation Category I

Environmental
The NI 6731/6733 is intended for indoor use only.
Operating temperature ......................... 0 to 50 °C
Storage temperature .............................. -20 to 70 °C
Humidity ..................................................... 5 to 90% RH, noncondensing
Maximum altitude .................................... 2,000 meters
Pollution Degree ....................................... 2

Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Safety
This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:
- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1

Note For UL and other safety certifications, refer to the product label, or visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Electromagnetic Compatibility
This product is designed to meet the requirements of the following standards of EMC for electrical equipment for measurement, control, and laboratory use:
- EN 61326 EMC requirements; Minimum Immunity
- EN 55011 Emissions; Group 1, Class A
- CE, C-Tick, ICES, and FCC Part 15 Emissions; Class A

Note For EMC compliance, operate this device with shielded cabling.

CE Compliance
This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:
- 73/23/EEC; Low-Voltage Directive (safety)
- 89/336/EEC; Electromagnetic Compatibility Directive (EMC)

Note Refer to the Declaration of Conformity (DoC) for this product for any additional regulatory compliance information. To obtain the DoC for this product, visit ni.com/certification, search by model number or product line, and click the appropriate link in the Certification column.

Waste Electrical and Electronic Equipment (WEEE)
EU Customers At the end of their life cycle, all products must be sent to a WEEE recycling center. For more information about WEEE recycling centers and National Instruments WEEE initiatives, visit ni.com/environment/weee.htm.
Device Pinouts

Figure 3. NI 6731 68-Pin AO I/O Connector Pin Assignments
Figure 4. NI 6733 68-Pin AO I/O Connector Pin Assignments