

Detailed Specifications | Pinouts/Front Panel Connections

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16-Channel, 50 MS/s, 14-Bit Digitizer Adapter Module for NI FlexRIO

NI 5751



- 16 simultaneously sampled 50 MS/s channels
- 14-bit vertical resolution
- 2 V_{pp}, 50 Ω single-ended inputs with DC coupling
- 8 general-purpose digital input and output lines for system stimulus and control
- Well-suited for applications ranging from research to large-scale deployment
- Requires NI FlexRIO FPGA module

Overview

Experiments and measurements in areas such as experimental physics, nondestructive test, and medical imaging can span across tens or hundreds of channels, requiring not only a system with high-channel density but also a way to retrieve and transfer the data and/or measurements of interest. The NI 5751 digitizer adapter module for NI FlexRIO provides the unique combination of high-channel density, scalability with PXI and PXI Express, and a fully programmable FPGA, which you can add for tasks such as custom triggering or inline signal processing. Eight digital inputs and outputs offer further benefits as system stimulus or control signals.

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Application and Technology

Key Specifications

Specification	Analog Input
Sample Rate	50 MS/s
Resolution	14 bits
Number of Channels	16, single-ended
Bandwidth	26 MHz
Input Range	2 V _{pk-pk}
Coupling	DC
Input Impedance	50 Ω
Crosstalk	-75 dB (1 MHz); -65 dB (5 MHz)

Table 1. Key Typical Specifications of the NI 5751

Combined with an NI FlexRIO FPGA module, the NI 5751 provides a powerful solution for applications requiring a high-channel-count digitizer with low crosstalk, the small form factor and scalability of PXI, and a user-accessible FPGA for custom real-time processing.

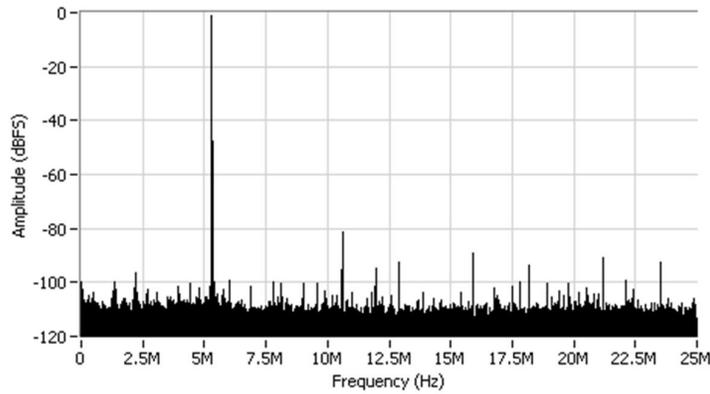


Figure 1. NI 5751 Characteristic Dynamic Performance, Spectrum – 64 k Samples, 5.3 MHz, -1 dBFS Input Signal

Application Areas

Application	Example Algorithms
High-channel-count advanced diagnostics	Data reduction, custom and event-based triggering
Complex detector systems	Combinational logic for advanced triggering on transient events
Tomography	Data reduction, FFT, cross-correlation
High-resolution time domain measurements	Custom data triggers, hysteresis, time in region, timing and voltage measurements

Table 2. Applications and Example Algorithms for the NI 5751

About NI FlexRIO

The NI FlexRIO family consists of PXI and PXI Express field-programmable gate array (FPGA) modules coupled to I/O adapter modules. Programmed with the NI LabVIEW FPGA Module, these modules together provide high-performance I/O and user-defined hardware processing on the PXI platform.

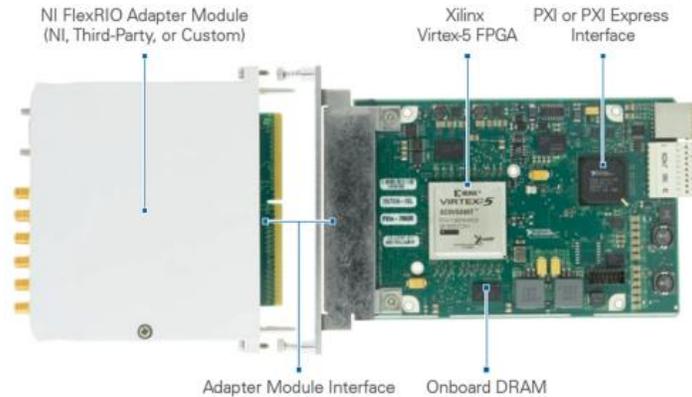


Figure 2. NI FlexRIO Architecture

NI FlexRIO FPGA modules feature the latest in FPGA technology and high-performance bus interfaces.

Model	Bus/Form Factor	FPGA	FPGA Slices	FPGA DSP Slices	FPGA Memory (Block RAM)	Onboard Memory (DRAM)
NI PXIe-7965R	PXI Express	Virtex-5 SX95T	14,720	640	8,784 kbits	512 MB
NI PXIe-7962R	PXI Express	Virtex-5 SX50T	8,160	288	4,752 kbits	512 MB
NI PXIe-7961R	PXI Express	Virtex-5 SX50T	8,160	288	4,752 kbits	0 MB
NI PXI-7954R	PXI	Virtex-5 LX110	17,280	64	4,608 kbits	128 MB
NI PXI-7953R	PXI	Virtex-5 LX85	12,960	48	3,456 kbits	128 MB
NI PXI-7952R	PXI	Virtex-5 LX50	7,200	48	1,728 kbits	128 MB
NI PXI-7951R	PXI	Virtex-5 LX30	4,800	32	1,152 kbits	0 MB

Table 3. NI FlexRIO FPGA Module Options

PXI Express NI FlexRIO FPGA modules feature Xilinx Virtex-5 SXT FPGAs with up to 512 MB of onboard DRAM, which you can access at bandwidths up to 3.2 GB/s. In addition to general-purpose reconfigurable logic, SXT FPGAs are optimized for high-speed digital signal processing (DSP), with up to 640 DSP slices for single-cycle multiplication and filtering functions. PXI Express NI FlexRIO FPGA modules also feature the NI STC-3 application-specific integrated circuit (ASIC), providing an optimized, high-bandwidth PCI Express x4 communications link to the backplane of the PXI Express chassis. This ASIC reduces the FPGA resources needed to implement host communication and enables new data transfer technology in the unique peer-to-peer (P2P) streaming feature. With NI P2P data streaming technology, you can continuously transfer data to and from PXI Express

NI FlexRIO FPGA modules at rates greater than 800 MB/s for additional processing and I/O integration. You can also stream to and from select PXI Express NI modular instruments for an even greater variety of I/O.

PXI NI FlexRIO FPGA modules feature Xilinx Virtex-5 LX FPGAs with up to 128 MB of onboard DRAM, which you can access at bandwidths up to 1.6 GB/s. They feature all the benefits of the PXI platform including synchronization, triggering, and high-speed data transfer to and from their host.

Feature	PXI NI FlexRIO FPGA Modules	PXI Express NI FlexRIO FPGA Modules
Xilinx Virtex-5 FPGAs	✓	✓
132-Line Line Adapter Module Interface	✓	✓
I/O Module Synchronization Clock	-	✓
Peer-to-Peer Data Streaming	-	✓

Table 4. PXI and PXI Express FPGA Module Comparison

National Instruments and third parties offer NI FlexRIO adapter modules, and you can build your own adapter modules using the NI FlexRIO Adapter Module Development Kit (MDK). With custom adapter modules, you can implement the exact analog and digital I/O your application requires, along with graphical FPGA programming provided by LabVIEW. View a current list of NI and third-party adapter modules at ni.com/flexrio. This ability to easily create high-bandwidth P2P data streams helps provide scalable signal processing and I/O integration.

LabVIEW FPGA

With the high-level graphical programming capabilities of LabVIEW FPGA, programming for the NI 5751 is far simpler than low-level HDL programming. Acquiring samples from one NI FlexRIO digitizer adapter module's analog-to-digital converter at its configured rate and placing the data into an FPGA FIFO is depicted in Figure 3.

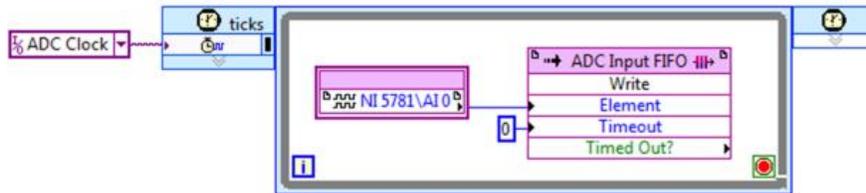


Figure 3. LabVIEW FPGA Code for Acquiring Data from an NI FlexRIO Digitizer Adapter Module

From this point, you may implement your own processing, filtering, fast Fourier transform (FFT), or control. Figure 4 shows custom demodulation using IP from the FPGA RF Communications Library on ni.com/labs.

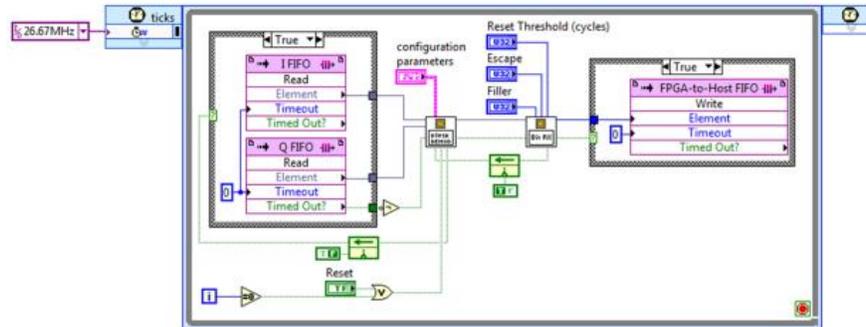


Figure 4. LabVIEW FPGA Code for Demodulating and Decoding I and Q Signals after 4X Decimation

For implementing a real-time spectrum analyzer, Figure 5 shows code that performs windowing, conversion to the frequency domain, comparison against a frequency mask, and assertion of a trigger when that mask is exceeded.

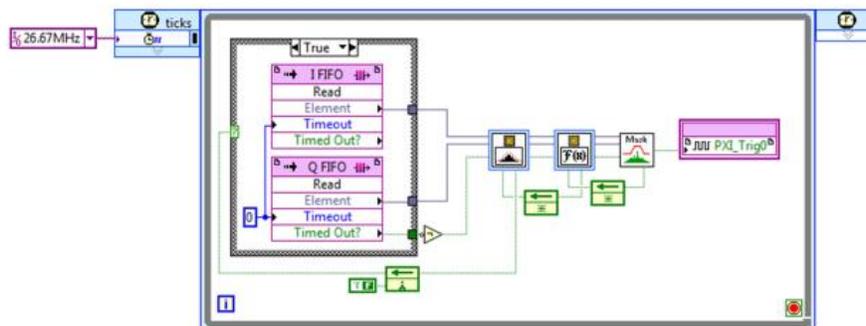


Figure 5. LabVIEW FPGA Code for a Real-Time Spectrum Analyzer

Finally, Figure 6 shows a custom, 128-tap inline finite impulse response (FIR) filter with reloadable coefficients. After filtering, the data is generated through a digital-to-analog converter.

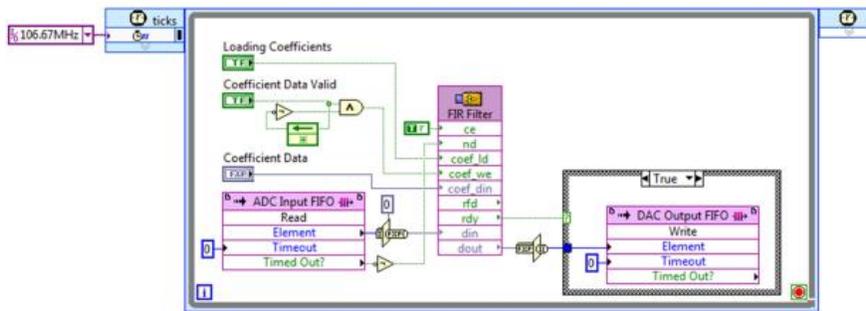


Figure 6. LabVIEW FPGA Code for an Inline Filter

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Support and Services

System Assurance Programs

NI system assurance programs are designed to make it even easier for you to own an NI system. These programs include configuration and deployment services for your NI PXI, CompactRIO, or Compact FieldPoint system. The NI Basic System Assurance Program provides a simple integration test and ensures that your system is delivered completely assembled in one box. When you configure your system with the NI Standard System Assurance Program, you can select from available NI system driver sets and application development environments to create customized, reorderable software configurations. Your system arrives fully assembled and tested in one box with your software preinstalled. When you order your system with the standard program, you also receive system-specific documentation including a bill of materials, an integration test report, a recommended maintenance plan, and frequently asked question documents. Finally, the standard program reduces the total cost of owning an NI system by providing three years of warranty coverage and calibration service. Use the online product advisors at ni.com/advisor to find a system assurance program to meet your needs.

Technical Support

Get answers to your technical questions using the following National Instruments resources.

- **Support** - Visit ni.com/support to access the NI KnowledgeBase, example programs, and tutorials or to contact our applications engineers who are located in NI sales offices around the world and speak the local language.
- **Discussion Forums** - Visit forums.ni.com for a diverse set of discussion boards on topics you care about.
- **Online Community** - Visit community.ni.com to find, contribute, or collaborate on customer-contributed technical content with users like you.

Repair

While you may never need your hardware repaired, NI understands that unexpected events may lead to necessary repairs. NI offers repair services performed by highly trained technicians who quickly return your device with the guarantee that it will perform to factory specifications. For more information, visit ni.com/repair.

Training and Certifications

The NI training and certification program delivers the fastest, most certain route to increased proficiency and productivity using NI software and hardware. Training builds the skills to more efficiently develop robust, maintainable applications, while certification validates your knowledge and ability.

- **Classroom training in cities worldwide** - the most comprehensive hands-on training taught by engineers.
- **On-site training at your facility** - an excellent option to train multiple employees at the same time.
- **Online instructor-led training** - lower-cost, remote training if classroom or on-site courses are not possible.
- **Course kits** - lowest-cost, self-paced training that you can use as reference guides.
- **Training memberships** and training credits - to buy now and schedule training later.

Visit ni.com/training for more information.

Extended Warranty

NI offers options for extending the standard product warranty to meet the life-cycle requirements of your project. In addition, because NI understands that your requirements may change, the extended warranty is flexible in length and easily renewed. For more information, visit ni.com/warranty.

OEM

NI offers design-in consulting and product integration assistance if you need NI products for OEM applications. For information about special pricing and services for OEM customers, visit ni.com/oem.

Alliance

Our Professional Services Team is comprised of NI applications engineers, NI Consulting Services, and a worldwide National Instruments Alliance Partner program of more than 700 independent consultants and integrators. Services range from start-up assistance to turnkey system integration. Visit ni.com/alliance.

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Detailed Specifications

This section lists the specifications of the NI FlexRIO adapter module (NI 5751). Pair these specifications with the specifications listed in the *NI FlexRIO FPGA Module Installation Guide and Specifications*. For more information about safety and electromagnetic compatibility refer to the *Read Me First: Safety and Electromagnetic Compatibility* document included in your hardware kit or available at ni.com/manuals.

Maximum and *minimum* specifications are warranted not to exceed these values within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

Characteristic specifications are unwarranted values that are representative of an average unit operating at room temperature.

Typical specifications are unwarranted values that are representative of a majority (90%) of units within certain operating conditions and include the effects of temperature and uncertainty unless otherwise noted.

These specifications are characteristic at 25 °C unless otherwise noted.

Absolute Maximum Ratings



Caution Stresses beyond those listed in this section may cause permanent damage to the adapter module. Avoid swapping the analog and digital cables because doing so will short the digital output terminals to ground.

Analog input overload	±2 V
External clock input	-0.5 V to 3.5 V
Digital input	-0.5 V to 3.5 V
Digital output current	2 mA

Analog Input (AI 0 to AI 15)

General Characteristics

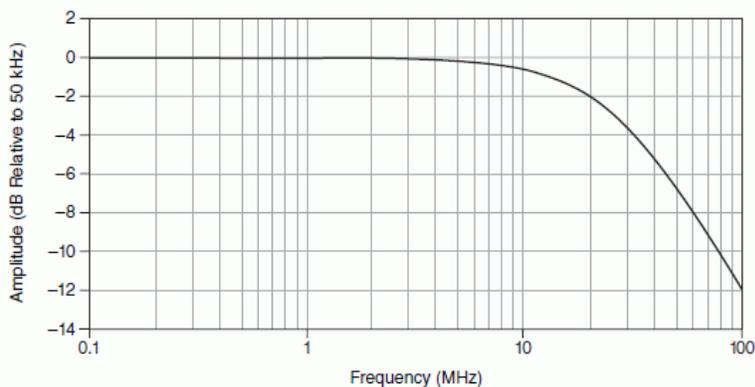
Type of connector	VHDCI. For pinout, refer to <i>NI 5751 Pinout—Analog Input CH 0 to 15</i>
Number of channels	16 single-ended
Max input voltage swing	2 V _{pp}
Input impedance	50 Ω ±2%
Coupling	DC coupled
ADC manufacturer part number	AD9252, 14-bit pipelined analog-to-digital converter



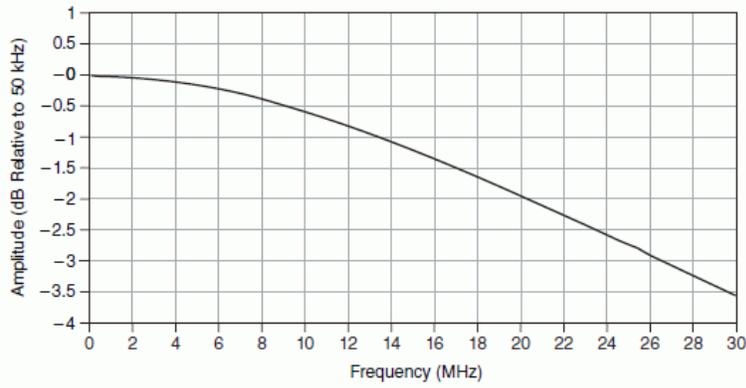
Note For additional information on the AD9252, refer to the device datasheet at www.analog.com.

Specific Characteristics

NI 5751 Characteristic Frequency Response

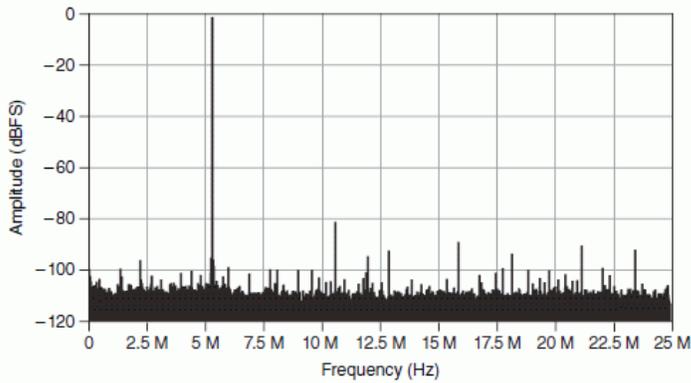


NI 5751 Characteristic Frequency Response

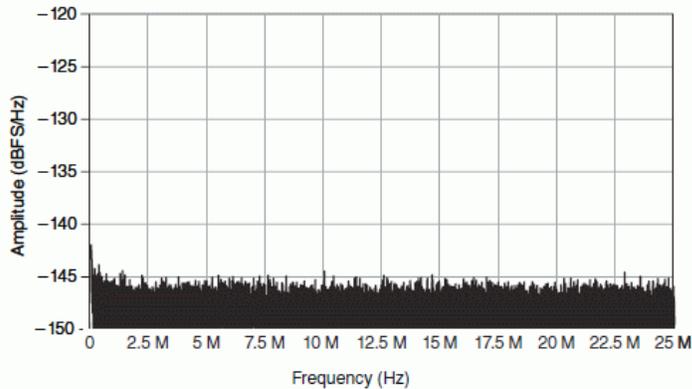


Bandwidth (-3 dB)	26 MHz
DC gain error	±2% of input
DC offset error	±2% of FS
Crosstalk	-75 dB at 1 MHz, -65 dB at 5 MHz, Measured on one channel with test signal applied to another channel
Signal-to-noise ratio (SNR)	71 dB, -1 dBFS input signal, $f_{in} = 5$ MHz
Spurious-free dynamic range (SFDR)	73 dBc, -1 dBFS input signal, $f_{in} = 5$ MHz
Total harmonic distortion (THD)	73 dBc, -1 dBFS input signal, $f_{in} = 5$ MHz
Average noise density	-147 dBFS/Hz

NI 5751 Characteristic Dynamic Performance, Spectrum-64 k Samples, 5.3 MHz, -1 dBFS Input Signal



NI 5751 Characteristic Noise Density, Spectrum-64 k Samples

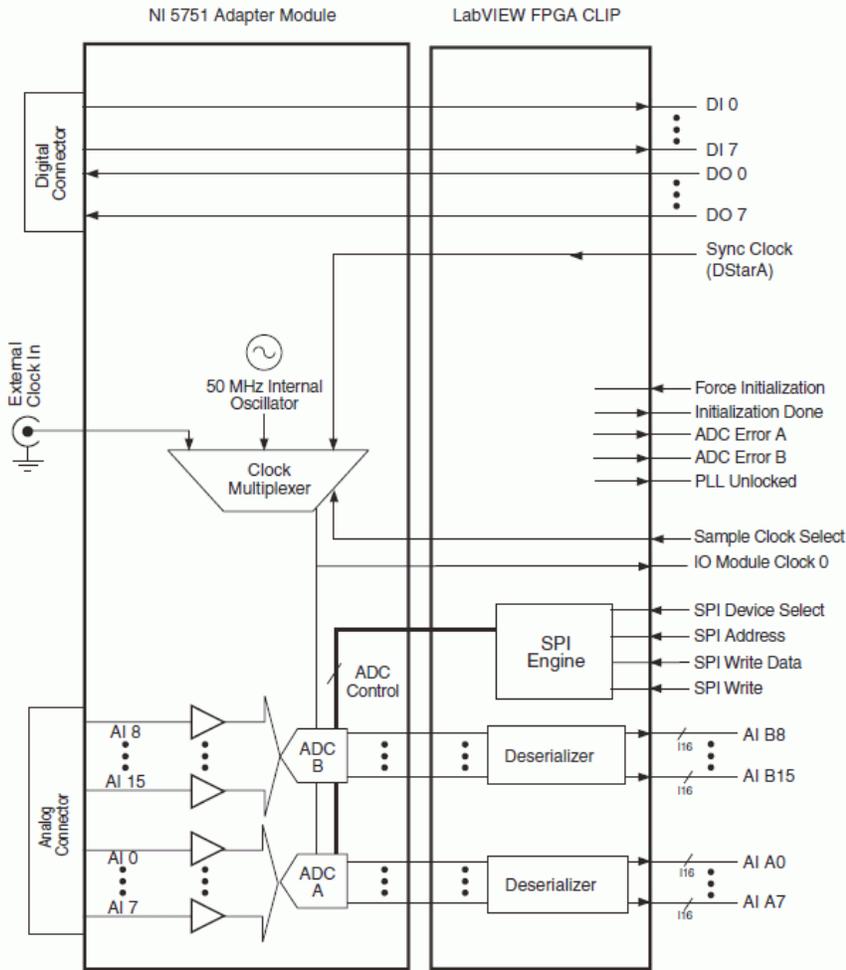


Sample Clock

Sample clock sources

- 50 MHz onboard clock
- Sync Clock (DStarA) ¹ ²
- CLK IN ² (front panel SMB)

Sample clock frequency range	30 MHz to 50 MHz ²
CLK IN	
General Characteristics	
Connector	SMB
Logic Level	3.3 V CMOS
V_{IH}	2.2 V
V_{IL}	0.6 V
Input impedance	> 50 k Ω
Input coupling	DC
Duty cycle	45% to 55%
Digital Input Terminals	
General Characteristics	
Number of channels	8
Connector	VHDCI. For pinout, refer to <i>NI 5751 Pinout—Digital Connector</i>
Minimum high-level input voltage	
V_{IH} (min)	2.0 V
Maximum low-level input voltage	
V_{IL} (max)	0.8 V
Digital Output Terminals	
General Characteristics	
Number of channels	8
Connector	VHDCI. For pinout, refer to <i>NI 5751 Pinout—Digital Connector</i>
Minimum high-level output voltage	
V_{OH} (min)	2.4 V
Maximum low-level output voltage	
V_{OL} (max)	0.55 V
Maximum output current	1 mA
Minimum pulse width	10 ns
Maximum toggle frequency	1 MHz, All outputs toggling
Hardware Block Diagram	
NI 5751 Hardware Block Diagram	



NI 5751 FlexRIO CLIP Node Wire Descriptions

NI 5751 CLIP Node IO Descriptions												
Port Name	Type	Function										
AI A<0..7>	116	Data from each of the eight channels on ADC A. If you are using the NI 5751 CLIP , data is clocked out of the CLIP on IO Module Clock 0. If you are using the NI 5751 Multidevice Synchronization CLIP , data is clocked out of the CLIP on DStarA. After Initialization Done is asserted the data is valid on every clock cycle.										
AI B<8..15>	116	Data from each of the eight channels on ADC B. If you are using the NI 5751 CLIP , data is clocked out of the CLIP on IO Module Clock 0. If you are using the NI 5751 Multidevice Synchronization CLIP , data is clocked out of the CLIP on DStarA. After Initialization Done is asserted the data is valid on every clock cycle.										
DI <0..7>	Boolean	Digital Input. Refer to the <i>Digital Input Terminals</i> section for more information.										
DO <0..7>	Boolean	Digital Output. Refer to the <i>Digital Output Terminals</i> section for more information.										
Digital Output Enable	Boolean	Enables the digital outputs.										
IO Module Clock 0	FPGA Clock	The ADC sample clock.										
Sample Clock Select	U8	Selects which clock is used as the ADC sample clock. When Sample Clock Select is changed, the data capture circuit is reinitialized. ³ This signal should be inside a single-cycle timed loop with a clock source of the 40 MHz onboard clock. <table border="1" style="margin-top: 10px;"> <thead> <tr> <th>Sample Clock Select (hex)</th> <th>Clock Source</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Internal Oscillator</td> </tr> <tr> <td>0x01</td> <td>Sync Clock (DSTAR A)</td> </tr> <tr> <td>0x02</td> <td>External Clock In</td> </tr> <tr> <td>other</td> <td>Reserved</td> </tr> </tbody> </table>	Sample Clock Select (hex)	Clock Source	0x00	Internal Oscillator	0x01	Sync Clock (DSTAR A)	0x02	External Clock In	other	Reserved
Sample Clock Select (hex)	Clock Source											
0x00	Internal Oscillator											
0x01	Sync Clock (DSTAR A)											
0x02	External Clock In											
other	Reserved											
Force Initialization	Boolean	Forces a CLIP initialization. ³ If you are using an external clock and the clock frequency changes, this signal must be manually asserted. ADC registers retain their values when Force Initialization is manually asserted. This signal should be inside a single-cycle timed loop with a clock source of the 40 MHz onboard clock.										
Initialization Done	Boolean	When this signal is asserted, initialization ³ of the CLIP has completed. This signal should be inside a single-cycle timed loop with a clock source of the 40 MHz onboard clock.										

NI 5751 CLIP Node IO Descriptions								
Port Name	Type	Function						
ADC Error A	Boolean	When ADC Error A is asserted the width of the sampling window from ADC A has shrunk below its required value, which does not guarantee that the data can be sampled correctly. This could be caused by a noisy clock source, a damaged ADC, or an incompatible NI FlexRIO FPGA module. ADC Error A is a sticky bit and is cleared upon reinitialization. ³						
ADC Error B	Boolean	When ADC Error B is asserted the width of the sampling window from ADC B has shrunk below its required value, which does not guarantee that the data can be sampled correctly. This could be caused by a noisy clock source, a damaged ADC, or an incompatible NI FlexRIO FPGA module. ADC Error B is a sticky bit and is cleared upon reinitialization. ³						
PLL Unlocked	Boolean	Indicates that the PLL has become unlocked since the board was initialized. When the PLL is unlocked IO Mod Clock 0 is disabled. When set, PLL Unlocked is cleared upon reinitialization. ³ This signal should be inside a single-cycle timed loop with a clock source of the 40 MHz onboard clock.						
SPI Idle ⁴	Boolean	Indicates the SPI engine is idle and ready for a SPI read or write transaction. This signal should be inside a single-cycle timed loop with a clock source of the 40 MHz onboard clock.						
SPI Device Select ⁴	U8	Selects which ADC the SPI port will communicate with. This signal should be inside a single-cycle timed loop with a clock source of the 40 MHz onboard clock. <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SPI Device</th> <th>ADC target</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>ADC A</td> </tr> <tr> <td>0x01</td> <td>ADC B</td> </tr> </tbody> </table>	SPI Device	ADC target	0x00	ADC A	0x01	ADC B
SPI Device	ADC target							
0x00	ADC A							
0x01	ADC B							
SPI Address ⁴	U8	The address of the register in the ADC selected. This signal should be inside a single-cycle timed loop with a clock source of the 40 MHz onboard clock.						
SPI Write Data ⁴	U16	Data to be written to the register in the ADC selected. This signal should be inside a single-cycle timed loop with a clock source of the 40 MHz onboard clock.						
SPI Write ⁴	Boolean	Begin SPI write transaction. The SPI Write signal should be inside a single-cycle timed loop with a clock source of the 40 MHz onboard clock.						

Initialization

During initialization, the CLIP does the following:

- Resets a PLL in the CLIP that is used to receive data from the ADCs.
- Resets the deserialization circuit.
- Recalibrates the data delays for capturing the data using dynamic phase alignment.
- Aligns the two ADC ICs to each other.
- Clears ADC Error X.

Manual Initialization

The user FPGA code must manually start initialization in the following instance:

- When using DStarA or CLK IN as the ADC sample clock and the frequency of the clock has changed since the last initialization.

To manually start initialization, the user FPGA code must assert Force Initialization.



Note When initialization starts, the Initialization Done signal deasserts within 100 ns. Initialization Done does not assert again until initialization has completed. You can expect a delay of up to 2 seconds before Initialization Done asserts again, depending on your clock rate. If you read the Initialization Done indicator before it has had time to deassert (100 ns), you may get a false positive.

Automatic Initialization

The CLIP performs initialization automatically in the following instances:

- The FPGA IO is enabled to the NI 5751
- The user FPGA code changes the Sample Clock Select signal

FPGA IO is enabled automatically when the CLIP is loaded into the FPGA. You can also programmatically enable and disable the FPGA IO from the host VI. When FPGA IO is enabled, the CLIP resets all ADC registers.



Caution Do *not* execute user FPGA code using IO Module Clock 0 until Initialization Done is True. While Initialization Done is False, the clocks are not stable.

If the user FPGA code changes the Sample Clock Select signal, the CLIP begins initialization automatically; you do not need to assert Force Initialization.



Note When initialization starts, the Initialization Done signal deasserts within 100 ns. Initialization Done does not assert again until initialization has completed. You can expect a delay of up to 2 seconds before Initialization Done asserts again, depending on your clock rate. If you read the Initialization Done indicator before it has had time to deassert (100 ns), you may get a false positive.

Accessing SPI Registers

The ADC register maps are included in the AD9252 datasheet. The following application note found on Analog Devices' Web site contains more information and SPI functionality for the AD9252: AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

SPI reads from the AD9252 are not supported on the NI 5751. The SPI access does not actually take effect until the software transfer bit (bit 0) of the device_update (offset 0xFF) register is written.

To access a register in an ADC, complete the following steps:

1. Configure the following:
 - SPI Device Select with which ADC to access.
 - SPI Address with the register offset.
 - SPI Write Data with the write data.
2. Set SPI Write for a write transaction.
3. Poll for SPI Idle to be True.

Power

Power requirements from the NI FlexRIO FPGA module

+12 V	200 mA, 2.4 W max
+3.3 V	900 mA, 2.97 W max
Total power	5.37 W

Physical

Dimensions	12.9 × 2.0 × 12.1 cm (5.1 × 0.8 × 4.7 in.)
Weight	284 g (10 oz)
Front panel connectors	One SMB connector and two 68-pin VHDCI connectors

Environmental

This device is intended for indoor use only.

Operating environment	0 °C to 55 °C, Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.
Relative humidity range	10% to 90%, noncondensing, Tested in accordance with IEC-60068-2-56.
Altitude	2,000 m
Pollution Degree	2
Storage environment	
Ambient temperature range	–20 °C to 70 °C, Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2.
Relative humidity range	5% to 95%, noncondensing, Tested in accordance with IEC-60068-2-56.



Note Clean the device with a soft, non-metallic brush. Make sure that the device is completely dry and free from contaminants before returning it to service.

Compliance and Certifications

Safety Standards

This product is designed to meet the requirements of the following standards of safety for electrical equipment for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA 61010-1



Note For UL and other safety certifications, refer to the product label or the *Online Product Certification* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions



Note For EMC declarations and certifications, refer to the *Online Product Certification* section.



Note When operating this product, use shielded cables and accessories.

CE Compliance

This product meets the essential requirements of applicable European Directives, as amended for CE marking, as follows:

- 2006/95/EC; Low-Voltage Directive (safety)

Online Product Certification

To obtain product certifications and the DoC for this product, visit ni.com/certification, search by module number or product line, and click the appropriate link in the Certification column.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial not only to the environment but also to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste Electrical and Electronic Equipment, visit ni.com/environment/weee.htm.

电子信息产品污染控制管理办法（中国 RoHS）



中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。
关于 National Instruments 中国 RoHS 合规性信息, 请登录 ni.com/environment/rohs_china。
(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

¹ Sync Clock (DStarA) is *only* available on NI PXI Express FlexRIO FPGA modules (such as the NI PXIe-796xR). On PXI Express modules, Sync Clock is driven by the DStarA from the PXI/PXIe backplane. For PXI modules (such as the NI PXI-795xR), Sync Clock (DStarA) is not available.

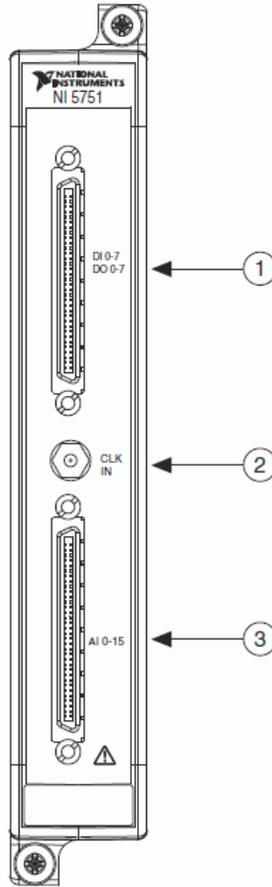
² If you change the frequency of Sync Clock (DStarA) or CLK IN (when used as the sample clock), you must assert Force Initialization. For more information, refer to the *Initialization* section.

³ For more information, refer to the *Initialization* section.

⁴ For more information, refer to the *Accessing SPI Registers* section.

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Pinouts/Front Panel Connections

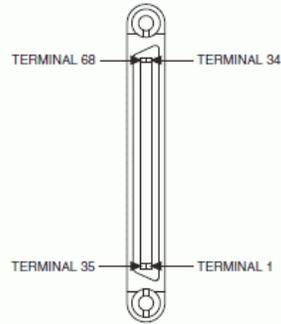


NI 5751 Front Panel Connectors

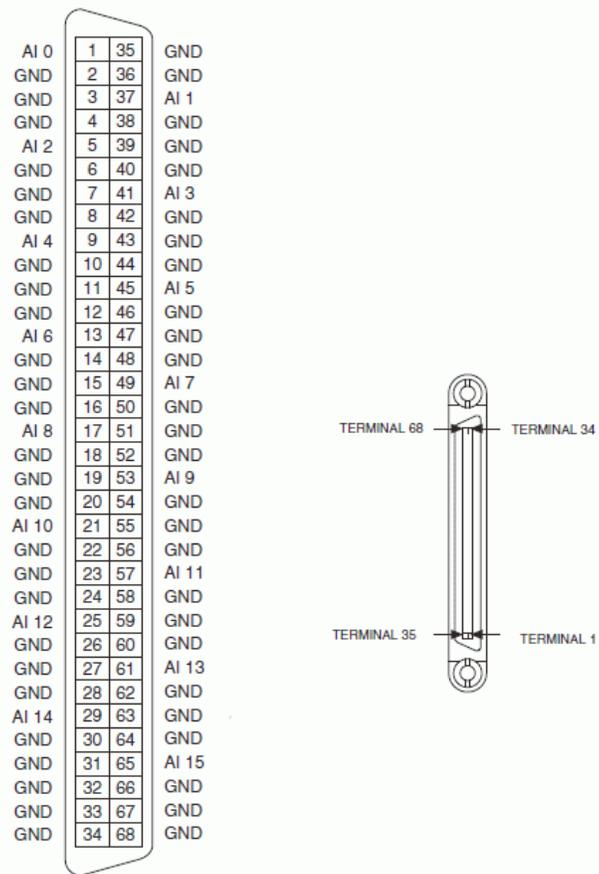
Number	Signal	Description
1	DI 0-7	Digital input terminals
	DO 0-7	Digital output terminals
2	CLK IN	External sample clock input
3	AI 0 through AI 15	Single-ended analog input channels

D GND	68	34	D GND
D GND	67	33	D GND
D GND	66	32	D GND
DO 0	65	31	DO 1
D GND	64	30	D GND
DO 2	63	29	DO 3
D GND	62	28	D GND
DO 4	61	27	DO 5
D GND	60	26	D GND
DO 6	59	25	DO 7
D GND	58	24	D GND
DO 8	57	23	DO 9
D GND	56	22	D GND
DO 10	55	21	DO 11
D GND	54	20	D GND
DO 12	53	19	DO 13
D GND	52	18	D GND
DO 14	51	17	DO 15
D GND	50	16	D GND
DI 0	49	15	DI 1
D GND	48	14	D GND
D GND	47	13	D GND
D GND	46	12	D GND
D GND	45	11	D GND
D GND	44	10	D GND
D GND	43	9	D GND
D GND	42	8	D GND
D GND	41	7	D GND
D GND	40	6	D GND
D GND	39	5	D GND
RSVD	38	4	RSVD
RSVD	37	3	RSVD
RSVD	36	2	RSVD
RSVD	35	1	RSVD

RSVD = Reserved



NI 5751 Pinout-Digital Connector



NI 5751 Pinout-Analog Input CH 0 to 15

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