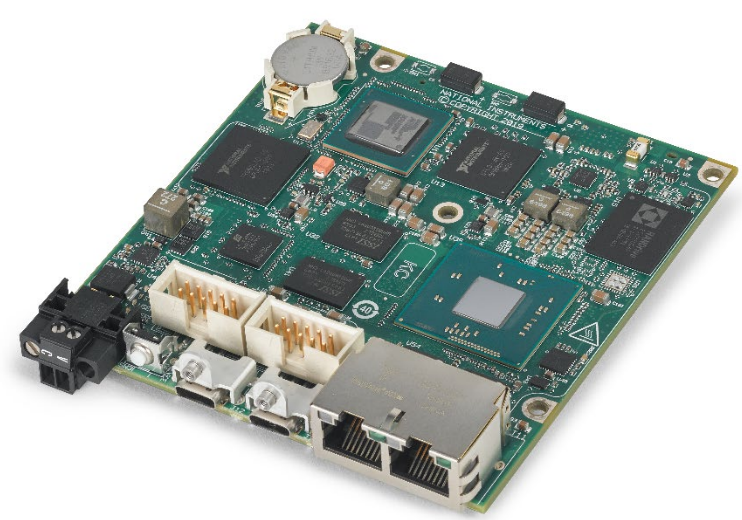
Cooling NI Single-Board RIO Systems

Appendix: Reference Examples
NI sbRIO-9603/08

3/5/2020



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1. Introduction

The NI sbRIO-9603/08 product typically operates as a component in a higher-level system, in which the thermal performance of the sbRIO is greatly influenced by several factors including, resource utilization, mounting, and adjacent power dissipation. It is the responsibility of the system integrator to consider enclosure size, materials, heat spreading or sinking solutions, and other mounting conditions when designing a system to ensure the sbRIO remains within maximum allowed temperature ranges.

The following document is intended to provide high-level examples of the thermal limits for an sbRIO-9603/08 product when integrated into a few example system configurations, and assuming maximum achievable thermal dissipation. These thermal reference examples explore enclosure choice, RMC expansion board power dissipation, heat spreaders, and LVDS output as factors in the overall thermal performance of the NI sbRIO-9603/08.

It will be shown that integrating an sbRIO into an enclosure introduces self-heating around the sbRIO, resulting in a lower achievable external ambient for the system, and further, that the enclosure material can play a role in the magnitude of the self-heating. Additional RMC expansion board power dissipation adjacent to the sbRIO-9603/08, or use of advanced features such as LVDS output, can further increase the self-heating and further reduce the achievable external ambient.

Finally, it is noted that the introduction of a heat spreading solution, such as the NI Thermal Kit for CompactRIO Single Board Controller with DAQmx, can substantially reduce the component temperatures of the sbRIO-9603/08, and is highly recommended if integrating the sbRIO-9603/08 into higher temperature environments.

When comparing the most favorable test results to the least favorable, an sbRIO-9603/08 mounted with little consideration to thermals may induce a 46 °C, or greater, penalty to the system’s achievable external ambient when compared to an sbRIO-9603/08 integrated in an ideal manner.

It is important to acknowledge the following results are specific to the enclosure size, enclosure material, mounting orientation, and resource utilization used for testing. The system integrator should weigh these considerations when determining how relevant the reference examples may be to any additional system configurations.

2. NI sbRIO-9608 General Setup

Device Under Test (DUT): NI sbRIO-9608

Equipment and Testing Supplies:

Test Equipment:

- Power Supply
- I/O Connectors and Cables
- RMC Resistor Load Test Board (used to simulate added power from an RMC)
- Thermal Kit for sbRIO-9603/08/09/28/29/38 (NI P/N 787331-01)

Enclosures:

- Large Fiberglass Enclosure – 12.0"x10.0"x6.34"
- Aluminum Panel (To mount the NI sbRIO-9608 for open air and inside the large enclosure)
- Small Metal Enclosure – 10.2"x6.3"x3.6"

NI sbRIO-9608 DUT Preparation:

- Thermocouples were mounted to critical IC cases.

- Four local ambient thermocouples were mounted approximately 0.2" away from the PCB on either side of the NI sbRIO-9608
- Wires were connected in order to measure the power dissipated by the DUT

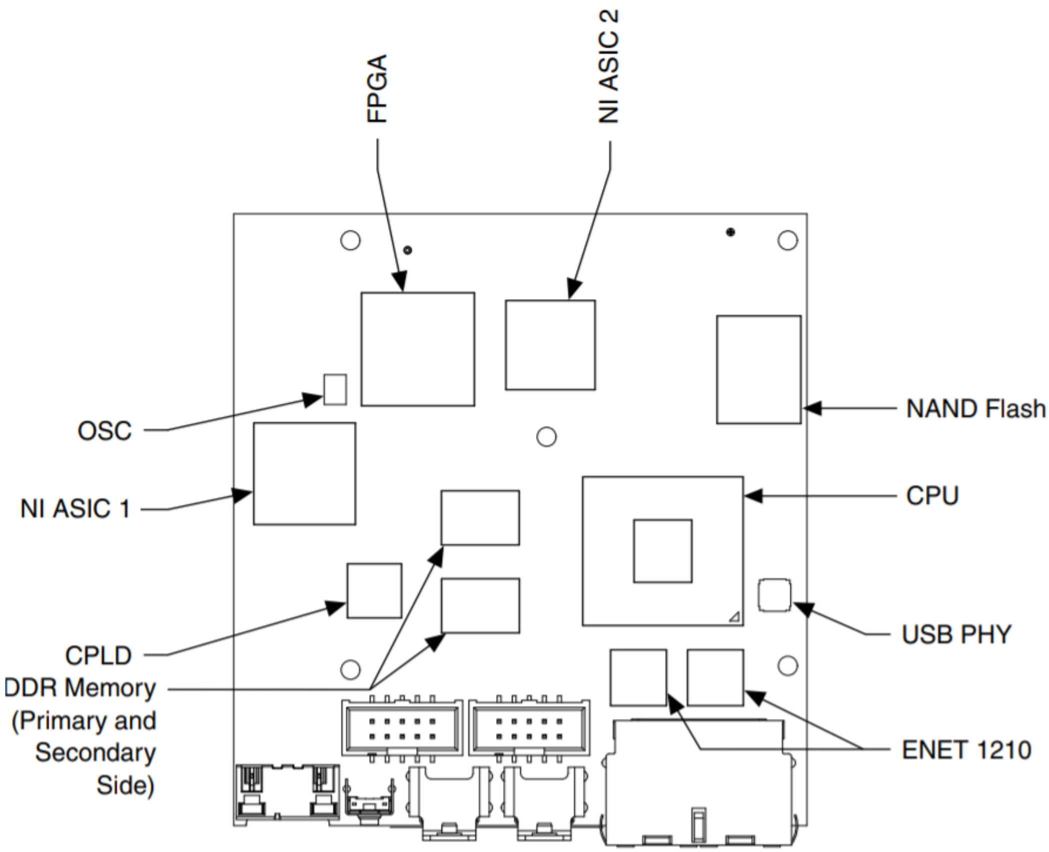


Figure 1: Thermally relevant component designation on NI sbRIO-9603/08

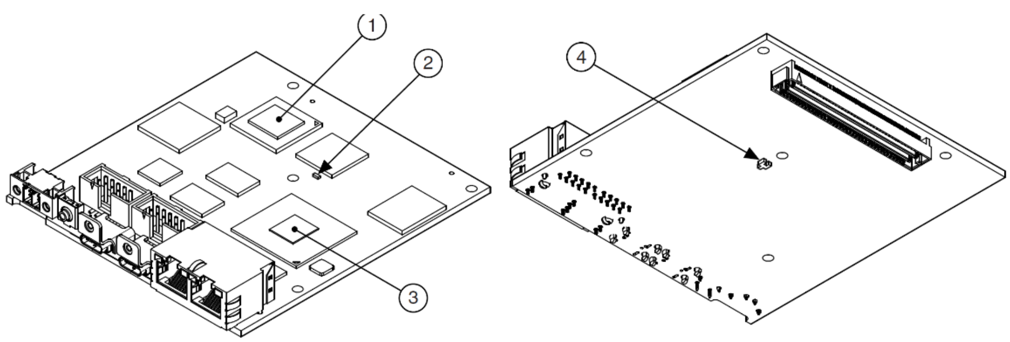


Figure 2: Digital thermal sensors designation on NI sbRIO-9603/08

Designation	Components
1	FPGA Sensor, U11
2	Primary System Sensor, U18
3	CPU Sensor, U36
4	Secondary System Sensor, Q24

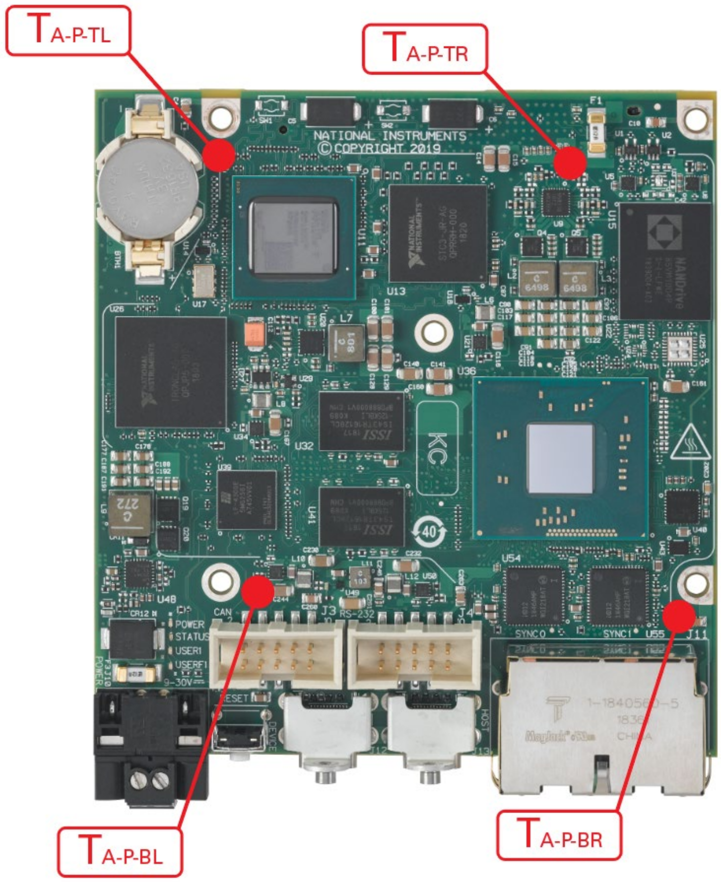


Figure 3: Thermocouple locations for Local Ambient temperature measurement, Primary Side shown. Measurements repeated on secondary side.

RMC Resistor Load Test Board Preparation:

- 4.05"x6.05" PCB
- Load resistors to provide even power distribution on both sides of PCB (e.g. 3W RMC test board is 1.5W on each side)

Software:

- A system stress-and-verify VI is run
  - Stresses the CPU and FPGA to max achievable power*
  - Performs write, read back, and verify tests to USB Flash drives, DDR memory, and the NAND flash
  - Stresses and verifies all I/O

*The power dissipation of the FPGA is drastically increased when utilizing LVDS outputs. Utilization of all 45 channels of LVDS outputs is a rare use case and could have substantial impacts on the achievable external ambient of an sbRIO installation. For this reason, Examples 1 – 4 below only exercised the FPGA to max achievable power without any channels of LVDS output. Example 5 below explores the additional impact to achievable external ambient when adding LVDS output to an installation. Due to Artix 7 FPGA technology used, LVDS inputs have a near negligible effect on thermal performance when compared to LVDS outputs.

Measurements:

The following table provides the channel, name, and description of the thermocouples that were measured during the tests, as well as the maximum allowed temperature for critical ICs and ambient locations for the NI sbRIO-9608 as defined in the user manual.

NI recommends using digital validation. The sbRIO-9608 includes four onboard temperature monitoring sensors to simplify validation of a thermal solution. The sensors measure the CPU and FPGA junction temperatures as well as printed circuit board temperatures that can be used to approximate the primary and secondary side local ambient temperatures. This approach is called digital validation.

The digital approach is more accurate for determining the performance of the CPU/FPGA but is more conservative for determining the local ambient temperatures. If the reported Primary System temperature or reported Secondary System temperature exceed the maximum temperatures listed in this document, then analog validation using thermocouples may be used for further verification.

Table 1: Monitored components on sbRIO-9608

Name	Description	Max Allowed (°C)	Comments
$T_{SEN\text{-}CPU\text{-}0}$	CPU Core 0 On-Chip Temperature Reading	108	Use digital approach to ensure the on-chip temperature reading is below 108°C*
$T_{SEN\text{-}CPU\text{-}1}$	CPU Core 1 On-Chip Temperature Reading	108	Use digital approach to ensure the on-chip temperature reading is below 108°C*
$T_{SEN\text{-}FPGA}$	FPGA On-Chip Temperature Reading	98	Use digital approach to ensure the on-chip temperature reading is below 98°C
$T_{C\text{-}DDR\text{-}1}$	DDR Case, First Primary Side Chip	95	One of two DDR chips located on primary side
$T_{C\text{-}DDR\text{-}2}$	DDR Case, Second Primary Side Chip	95	One of two DDR chips located on primary side
$T_{C\text{-}NAND}$	NAND Flash Case	91	
$T_{C\text{-}CPLD}$	CPLD Case	94	
$T_{C\text{-}USB}$	USB PHY Case	120	
$T_{C\text{-}ENET\text{-}1}$	ENET I210 Case, First Chip	95	
$T_{C\text{-}ENET\text{-}2}$	ENET I210 Case, Second Chip	95	
$T_{C\text{-}ASIC\text{-}1}$	NI ASIC 1 Case	120	
$T_{C\text{-}ASIC\text{-}2}$	NI ASIC 2 Case	116	
$T_{C\text{-}OSC}$	OSC Case	112	
$T_{A\text{-}P\text{-}SEN}$	Digitally Reported Primary Side Local Ambient	85	Conservative approximation of the local ambient temperature
$T_{A\text{-}S\text{-}SEN}$	Digitally Reported Secondary Side Local Ambient	85	Conservative approximation of the local ambient temperature
$T_{A\text{-}P\text{-}TL}$	Primary Side, Top Left Local Ambient	85	Mounted 0.2" off PCB
$T_{A\text{-}P\text{-}TR}$	Primary Side, Top Right Local Ambient	85	Mounted 0.2" off PCB
$T_{A\text{-}P\text{-}BL}$	Primary Side, Bottom Left Local Ambient	85	Mounted 0.2" off PCB
$T_{A\text{-}P\text{-}BR}$	Primary Side, Bottom Right Local Ambient	85	Mounted 0.2" off PCB
$T_{A\text{-}S\text{-}TL}$	Secondary Side, Top Left Local Ambient	85	Mounted 0.2" off PCB

$T_{A\text{-}S\text{-}TR}$	Secondary Side, Top Right Local Ambient	85	Mounted 0.2" off PCB
$T_{A\text{-}S\text{-}BL}$	Secondary Side, Bottom Left Local Ambient	85	Mounted 0.2" off PCB
$T_{A\text{-}S\text{-}BR}$	Secondary Side, Bottom Right Local Ambient	85	Mounted 0.2" off PCB
$T_{A\text{-}Ext}$	External Ambient (Room Ambient)	NA	Average of two thermocouple measurements

* The CPU reduces its operating frequency when the die temperature reaches 108 °C. NI recommends keeping the die temperature below 108 °C to guarantee optimal performance. Refer to the *CompactRIO Single Board Controller with DAQmx Hardware Installation Manual* for information about monitoring the CPU die temperature.

Note: IC case temperatures were either obtained from manufacturer's datasheets or calculated using the formula:
$T_J = T_C + P \times \Theta_{J\text{-}C}$
Where:
T_J – Junction Temperature
T_C – Case Temperature
P – Power Dissipation (From Datasheet, Measured or Estimated)
$\Theta_{J\text{-}C}$ – Junction-Case Thermal Resistance

Test Procedure:

- Testing was conducted at room temperature
- The NI sbRIO-9608 was mounted as described by the examples in the following sections
- The NI sbRIO-9608 was powered at 30V
- The system stressing VI was configured and run
- The system was allowed to reach steady state
- Temperature measurements were logged

3. Example 1 – NI sbRIO-9608, Open Air vs. Enclosure

3.1. *Test Description*

In this example, the NI sbRIO-9608 was configured in open air and with a large fiberglass enclosure to show how the enclosure affects the self-heating around the circuit card. This Example does not exercise the LVDS features of the FPGA. See Example 5 for more information on the additional thermal impacts of using LVDS.

3.2. *Test Results Summary*

The self-heating around the NI sbRIO-9608 is increased by adding an enclosure, resulting in a lower achievable external ambient.

In this set of examples, without a thermal solution, the FPGA has the lowest margin. Extrapolating to the maximum allowed temperature of the FPGA, the estimated maximum achievable external ambient for each configuration is shown in the following table.

Table 2: sbRIO-9608 maximum achievable ambient – open air vs. enclosure

Configuration	**A** **(Open Air)**	**B** **(Large Fiberglass Enclosure)**
Max Achievable $T_{A\text{-}Ext}$ (°C)	39.9	33.5

In addition, the margin of the digitally reported primary side local ambient was the next lowest margin temperature measurement. Less stressful applications or the addition of a thermal solution such as a heat sink or heat spreader may improve the max achievable external ambient. Later in this document, examples showing the impact of adding a thermal solution will be examined. See Examples 3 and 4 for more information.

3.3. *Test Setup*

In this example, the NI sbRIO-9608 was installed without an RMC (i.e. controller only).

- The NI sbRIO-9608 was mounted to the panel using 18mm standoffs.
- (A) Open Air Configuration – The NI sbRIO-9608 was mounted to a metal panel and oriented vertically, as shown in the following images.
- (B) Large Fiberglass Enclosure – The NI sbRIO-9608 was mounted to a metal panel and installed into a large fiberglass enclosure. The enclosure was oriented such that the PCB was vertical during testing, as shown in the following images.

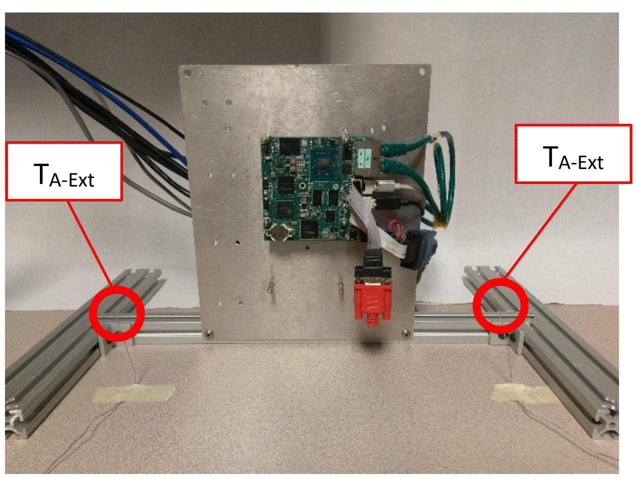


Figure 4: Configuration A – NI sbRIO-9608 in open air

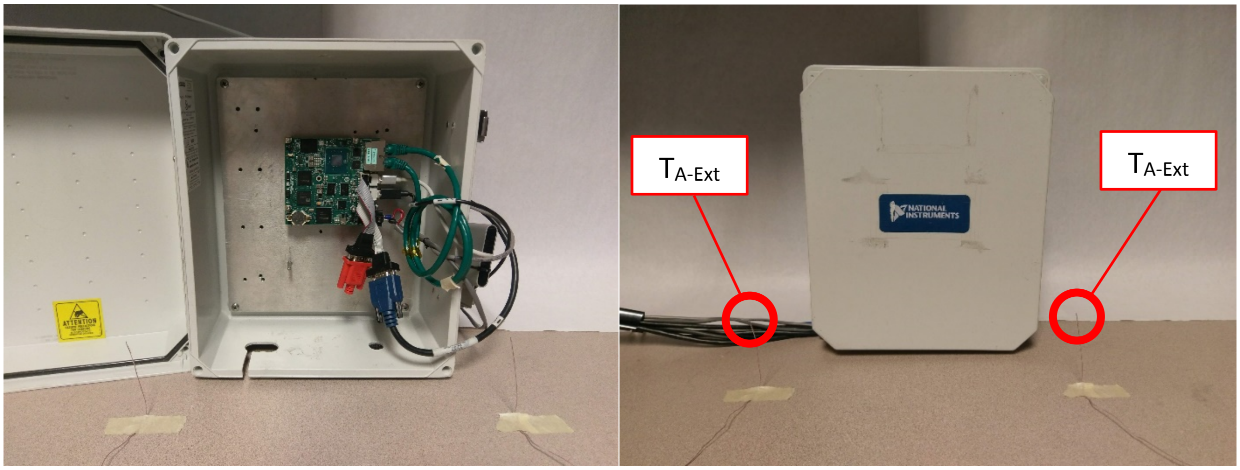


Figure 5: Configuration B – NI sbRIO-9608 in a large fiberglass enclosure

3.4. *Results*

The following table shows the test results normalized to T_{A-Ext}=25°C. In addition, it includes the margin of the temperature reading compared to the maximum allowed values for each component or ambient measurement. In the "margin" column, the lowest margin component is highlighted.

Table 3: sbRIO-9608 component measurements and margin – open air vs. enclosure

	A Open Air		B Large Fiberglass Encl.	
Component	Measurement (°C)	Margin (°C)	Measurement (°C)	Margin (°C)
$T_{SEN-CPU-0}$	68.4	39.6	76.0	32.0
$T_{SEN-CPU-1}$	71.3	36.7	78.0	30.0
$T_{SEN-FPGA}$	83.1	14.9	89.5	8.5
$T_{C-DDR-1}$	66.2	28.8	72.8	22.2
$T_{C-DDR-2}$	62.6	32.4	69.5	25.5
T_{C-NAND}	61.9	29.6	68.7	22.8
T_{C-CPLD}	62.8	31.1	69.9	24.1
T_{C-USB}	61.3	58.3	67.8	51.8
$T_{C-ENET-1}$	63.2	31.8	69.9	25.1
$T_{C-ENET-2}$	62.0	33.0	68.7	26.3
$T_{C-ASIC-1}$	68.0	51.9	74.9	45.0
$T_{C-ASIC-2}$	73.0	43.3	79.6	36.7
T_{C-OSC}	68.3	44.1	75.0	37.4
$T_{A-P-SEN}$	67.4	17.6	74.1	10.9
$T_{A-S-SEN}$	65.0	20.0	71.7	13.3
T_{A-P-TL}	55.2	29.8	64.1	20.9
T_{A-P-TR}	51.4	33.6	58.5	26.5
T_{A-P-BL}	50.2	34.8	53.6	31.4
T_{A-P-BR}	50.8	34.2	58.0	27.0
T_{A-S-TL}	54.0	31.0	60.6	24.4

$T_{A\text{-}S\text{-}TR}$	57.9	27.1	65.2	19.8
$T_{A\text{-}S\text{-}BL}$	45.9	39.1	53.1	31.9
$T_{A\text{-}S\text{-}BR}$	49.5	35.5	56.2	28.8
$T_{A\text{-}Ext}$	25.0	-	25.0	-

The measured system power draw of the NI sbRIO-9608 was approximately 13.1W for each configuration.

The first thing to note is that the FPGA has the lowest margin in both configurations. Also, the self-heating caused by the addition of an enclosure results in an additional temperature rise within the system.

Comparing configuration B to A, the added self-heating temperature rise of the large fiberglass enclosure is approximately 6 to 7 °C.

Using this data, we can estimate the maximum achievable external ambient for each configuration, as shown in the following table.

Table 2: Maximum achievable ambient – open air vs. enclosure

Configuration	**A** **(Open Air)**	**B** **(Large Fiberglass Enclosure)**
Max Achievable $T_{A\text{-}Ext}$ (°C)	39.9	33.5

4. Example 2 – NI sbRIO-9608, Open Air vs. Enclosure, With RMC

4.1. Test Description

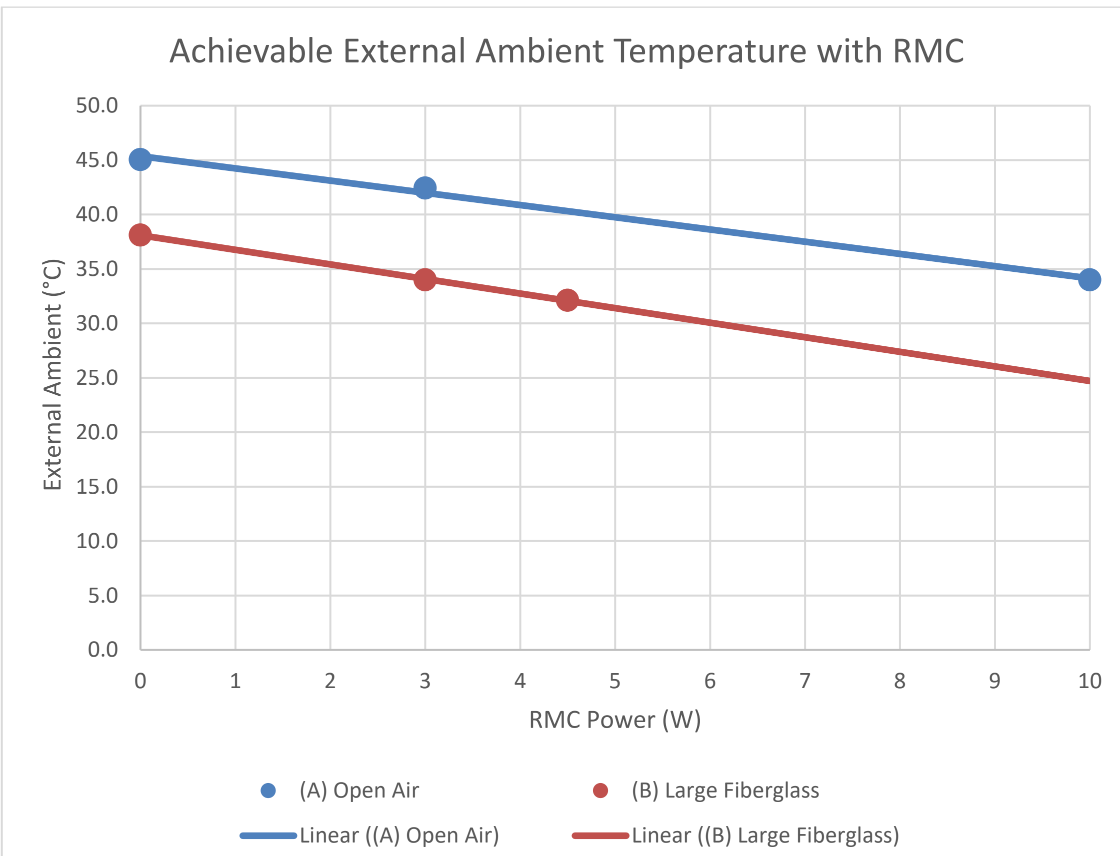
In this example, the NI sbRIO-9608 was configured with an RMC, loaded at varying power levels to show the impact of adding an expansion card. The same open air and enclosure configurations from Example 1 were used. This Example does not exercise the LVDS features of the FPGA. See Example 5 for more information on the additional thermal impacts of using LVDS.

4.2. Test Results Summary

The self-heating around the NI sbRIO-9608 is increased within an enclosure, resulting in a lower achievable external ambient. In addition, the rate of self-heating increases with increasing RMC power, resulting in a larger change in the achievable external ambient between the 0W RMC and 10W RMC within an enclosure.

In this set of examples, the digitally reported FPGA temperature has the lowest margin for all test cases, followed by the digitally reported primary side local ambient. Extrapolating to the maximum allowed temperature of the FPGA, the estimated maximum achievable external ambient for each configuration is shown in the following chart.

Chart 1: sbRIO-9608 achievable ambient vs. RMC power – open air vs. enclosure with RMC



Less stressful applications or the addition of a thermal solution such as a heat sink or heat spreader may improve the max achievable external ambient. Later in this document, examples showing the impact of adding a thermal solution will be examined. See Examples 3 and 4 for more information.

4.3. Test Setup

In this example, the NI sbRIO-9608 was installed with a resistor load RMC test board.

- The circuit cards were mounted such that the RMC was between the mounting panel and the NI sbRIO-9608.
- The RMC was mounted to the panel using 18mm standoffs.
- The NI sbRIO-9608 was mounted to the RMC using 9.65mm standoffs.
- The same open air and enclosure configurations as in Example 1 were used.
- Tests were performed with the RMC load at 0W, 3W, and 10W for the open air configuration and 0W, 3W, and 4.5W for the large fiberglass. Increasing RMC power to 10W in the fiberglass enclosure without a thermal solution, and at room temperature risked causing the CPU to exceed 108 °C and reduce its operating frequency. Data collected while the CPU operating frequency is reduced cannot be extrapolated. Therefore, data for a 4.5W RMC load was substituted for 10W in this case.
- In the test results, the subscript number for each test configuration corresponds to the RMC power load used for that test. So, A_0 corresponds to the unpowered, 0W RMC, A_3 corresponds to the 3W RMC, and so on.
- (A) Open Air Configuration – The NI sbRIO-9608 with RMC was mounted to a metal panel and oriented vertically, as shown in the following images.
- (B) Large Fiberglass Enclosure – The NI sbRIO-9608 with RMC was mounted to a metal panel and installed into a large fiberglass enclosure. The enclosure was oriented such that the PCB was vertical during testing, as shown in the following images.

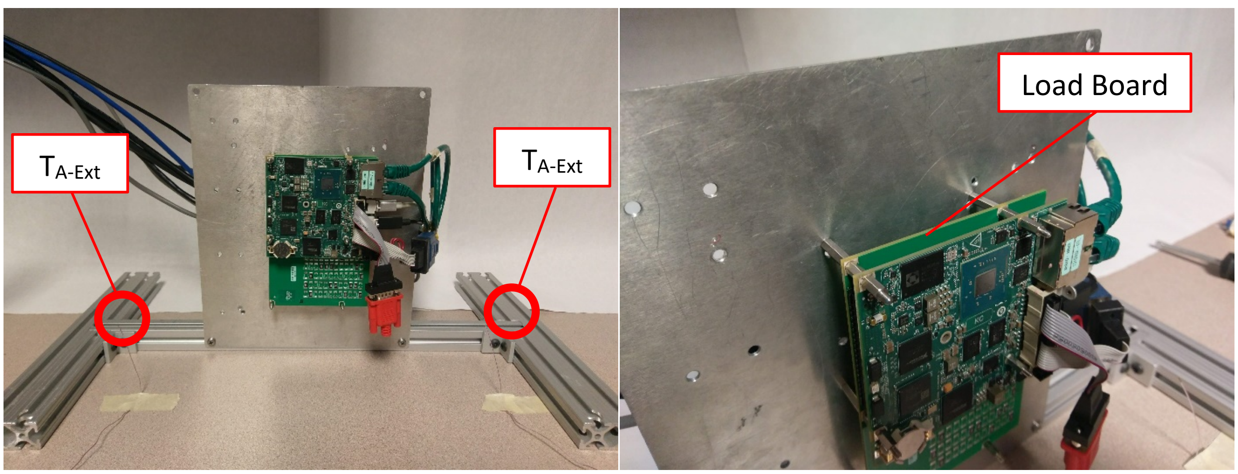


Figure 6: Configuration A – NI sbRIO-9608 with RMC load board in open air

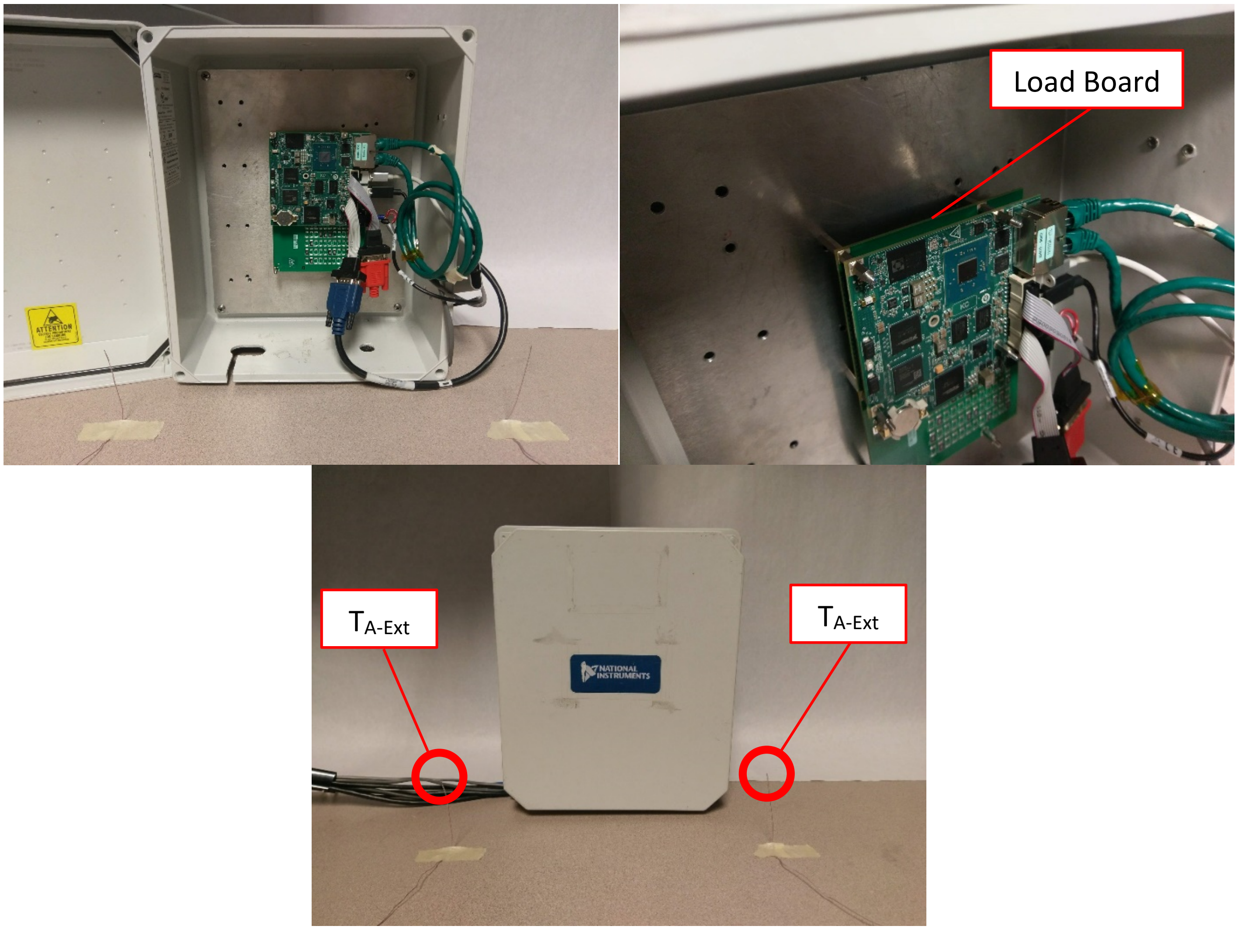


Figure 7: Configuration B – NI sbRIO-9608 with RMC load board in a large fiberglass enclosure

4.4. *Results*

The following table shows the test results normalized to $T_{A\text{-}Ext}$=25°C. It includes the power draw measured by both the sbRIO board and the RMC test board, along with the margin of the temperature reading compared to the maximum allowed values for each component or ambient measurement. In the "margin" column, the lowest margin component is highlighted.

Table 4: sbRIO-9608 component measurements and margin – configuration A with RMC

Open Air with RMC						
Configuration	A_0		A_3		A_{10}	
NI sbRIO-9608 Power (W)	12.7		12.6		14.6	
RMC Power (W)	0		3		10	
Total System Power (W)	12.7		15.6		24.6	
Component	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**
$T_{SEN\text{-}CPU\text{-}0}$	65.6	42.4	67.3	40.7	76.5	31.5

$T_{SEN-CPU-1}$	68.4	39.6	70.8	37.2	79.4	28.6
$T_{SEN-FPGA}$	77.9	20.1	80.6	17.4	89.0	9.0
$T_{C-DDR-1}$	62.9	32.1	65.3	29.7	73.7	21.3
$T_{C-DDR-2}$	60.0	35.0	62.2	32.8	70.7	24.3
T_{C-NAND}	57.8	33.6	60.2	31.2	68.4	23.1
T_{C-CPLD}	60.2	33.7	62.5	31.5	71.9	22.1
T_{C-USB}	59.0	60.7	61.3	58.4	68.6	51.1
$T_{C-ENET-1}$	60.9	34.1	63.0	32.0	70.7	24.3
$T_{C-ENET-2}$	59.9	35.1	62.0	33.0	69.5	25.5
$T_{C-ASIC-1}$	64.9	55.0	67.0	52.9	75.5	44.4
$T_{C-ASIC-2}$	67.5	48.8	70.2	46.1	78.7	37.6
T_{C-OSC}	64.5	48.0	66.7	45.7	74.5	37.9
$T_{A-P-SEN}$	62.9	22.1	65.5	19.5	74.0	11.0
$T_{A-S-SEN}$	61.3	23.7	63.9	21.1	72.5	12.5
T_{A-P-TL}	50.5	34.5	52.0	33.0	58.3	26.7
T_{A-P-TR}	46.7	38.3	47.8	37.2	54.2	30.8
T_{A-P-BL}	48.9	36.1	50.2	34.8	57.2	27.8
T_{A-P-BR}	48.3	36.7	49.8	35.2	55.9	29.1
T_{A-S-TL}	50.6	34.4	52.7	32.3	58.2	26.8
T_{A-S-TR}	55.8	29.2	58.4	26.6	68.0	17.0
T_{A-S-BL}	43.5	41.5	45.3	39.7	50.9	34.1
T_{A-S-BR}	48.0	37.0	49.9	35.1	57.2	27.8
T_{A-Ext}	25.0	-	25.0	-	25.0	-

Table 5: sbRIO-9608 component measurements and margin – configuration B with RMC

Large Fiberglass Enclosure with RMC						
Configuration	**B_0**		**B_3**		**$B_{4.5}$**	
NI sbRIO-9608 Power (W)	13.5		13.7		13.8	
RMC Power (W)	0		3		4.5	
Total System Power (W)	13.5		16.7		18.3	
Component	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**
$T_{SEN-CPU-0}$	72.3	35.7	77.7	30.3	79.5	28.5
$T_{SEN-CPU-1}$	75.1	32.9	80.5	27.5	82.6	25.4
$T_{SEN-FPGA}$	84.9	13.1	89.0	9.0	90.9	7.1
$T_{C-DDR-1}$	69.7	25.3	73.9	21.1	75.7	19.3
$T_{C-DDR-2}$	66.8	28.2	71.0	24.0	72.8	22.2
T_{C-NAND}	64.9	26.6	69.2	22.3	71.0	20.5
T_{C-CPLD}	67.1	26.9	71.2	22.8	72.9	21.0

T_{C-USB}	65.9	53.7	70.2	49.5	71.9	47.8
$T_{C-ENET-1}$	67.8	27.2	71.9	23.1	73.8	21.2
$T_{C-ENET-2}$	66.9	28.1	71.1	23.9	72.9	22.1
$T_{C-ASIC-1}$	71.7	48.2	75.7	44.2	77.3	42.6
$T_{C-ASIC-2}$	74.4	41.9	78.8	37.5	80.7	35.6
T_{C-OSC}	71.3	41.1	75.2	37.2	76.9	35.5
$T_{A-P-SEN}$	69.8	15.2	74.2	10.8	76.1	8.9
$T_{A-S-SEN}$	68.2	16.8	72.7	12.3	74.6	10.4
T_{A-P-TL}	57.7	27.3	61.8	23.2	62.8	22.2
T_{A-P-TR}	54.8	30.2	58.3	26.7	59.8	25.2
T_{A-P-BL}	51.9	33.1	54.9	30.1	56.2	28.8
T_{A-P-BR}	55.9	29.1	58.8	26.2	60.4	24.6
T_{A-S-TL}	57.4	27.6	61.1	23.9	62.6	22.4
T_{A-S-TR}	62.8	22.2	67.5	17.5	69.5	15.5
T_{A-S-BL}	49.0	36.0	53.0	32.0	54.7	30.3
T_{A-S-BR}	54.6	30.4	59.0	26.0	61.0	24.0
T_{A-Ext}	25.0	-	25.0	-	25.0	-

The tests above shown with a 0W RMC had the RMC board installed, but not powered. The measured power draw of the NI sbRIO-9608 increases slightly as the RMC power increases due to the added load on the power supply. With a 10W RMC, this resulted in 1.9W additional power being dissipated on the sbRIO board.

The first thing to note is that additional loads nearby to the sbRIO-9608 can both impact the component margins and cause the lowest margin component to change. Also, the self-heating caused by the addition of an enclosure results in an additional temperature rise within the system.

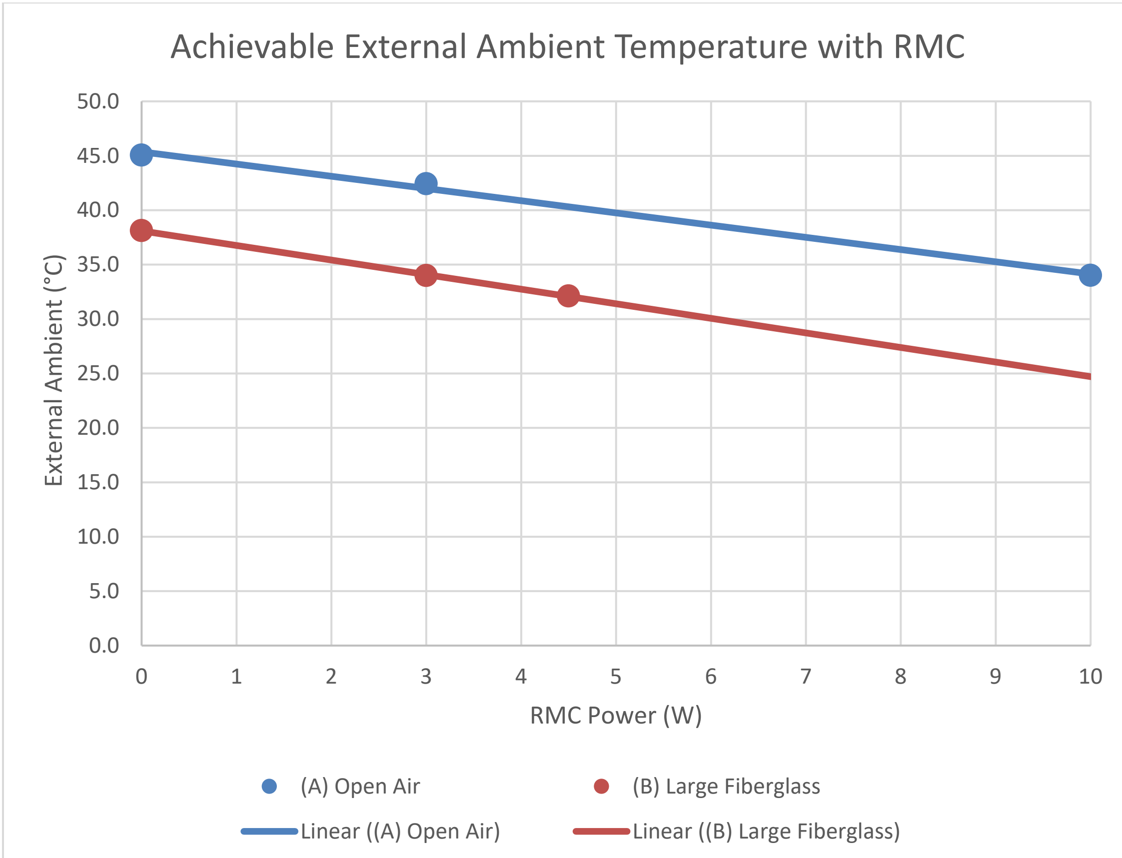
Using this data, the maximum achievable external ambient for each configuration is estimated, as shown in the following table.

Table 6: Maximum achievable ambient – open air vs. enclosure with RMC

RMC Power (W)	**Max Achievable T_{A-Ext} (°C)**	
	A	**B**
0.0	45.1	38.1
3.0	42.4	34.0
4.5	-	32.1
10.0	34.0	-

The following chart plots the achievable external ambient compared with RMC power levels for each configuration. The results may be approximated with a linear extrapolation to estimate the ambient at different RMC power levels within the different enclosures.

Chart 1: sbRIO-9608 achievable ambient vs. RMC power – open air vs. enclosure with RMC


Achievable External Ambient Temperature with RMC
External Ambient (°C)
50.0
45.0
40.0
35.0
30.0
25.0
20.0
15.0
10.0
5.0
0.0
0
1
2
3
4
5
6
7
8
9
10
RMC Power (W)
(A) Open Air
(B) Large Fiberglass
Linear ((A) Open Air)
Linear ((B) Large Fiberglass)

5. Example 3 – NI sbRIO-9608, Open Air vs. Enclosure Size, With Thermal Solution

5.1. *Test Description*

In this example, the NI sbRIO-9608 was configured with a heat spreader and installed in open air and with varying enclosure sizes/materials to show how a heat spreader can improve the thermal performance. This Example does not exercise the LVDS features of the FPGA. See Example 5 for more information on the additional thermal impacts of using LVDS.

5.2. *Test Results Summary*

With the addition of a heat spreader, the impact of self-heating is greatly reduced compared to the tests in Example 1. In addition, the heat spreader greatly reduces the junction temperature of the CPU, FPGA and case temperature of other critical ICs, resulting in a higher achievable external ambient temperature. Extrapolating to the maximum allowed temperature of the lowest margin measurements, the estimated maximum achievable external ambient for each configuration is shown in the following table.

Table 7: Maximum achievable ambient – open air vs. enclosure size with thermal solution

Configuration	**A** **(Open Air)**	**B** **(Large Fiberglass Enclosure)**	**C** **(Small Metal Enclosure)**
Max Achievable $T_{A\text{-}Ext}$ (°C)	68.5	60.6	69.3

Comparing to Example 1, the addition of a thermal solution when operating in both open air (configuration A) and a large fiberglass enclosure (configuration B) resulted in approximately 28°C increase in the achievable external ambient. Further, when using a thermal solution, moving from a large fiberglass enclosure (configuration B) to a small metal enclosure (configuration C) resulted in an additional 9°C increase in the achievable external ambient.

5.3. *Test Setup*

- In this example, the NI sbRIO-9608 was installed with a heat spreader attached (NI P/N 787331-01). No RMC was installed (i.e. controller only).
- The NI sbRIO-9608 was mounted such that the heat spreader directly contacted the metal mounting surface.
- (A) Open Air Configuration – The NI sbRIO-9608 was mounted to a metal panel and oriented vertically, as shown in the following images.
- (B) Large Fiberglass Enclosure – The NI sbRIO-9608 was mounted to a metal panel and installed into a large fiberglass enclosure. The enclosure was oriented such that the PCB was vertical during testing, as shown in the following images.
- (C) Small Metal Enclosure – The NI sbRIO-9608 was mounted directly to the side wall of a small aluminum enclosure. The enclosure was oriented such that the PCB was vertical during testing, as shown in the following images.

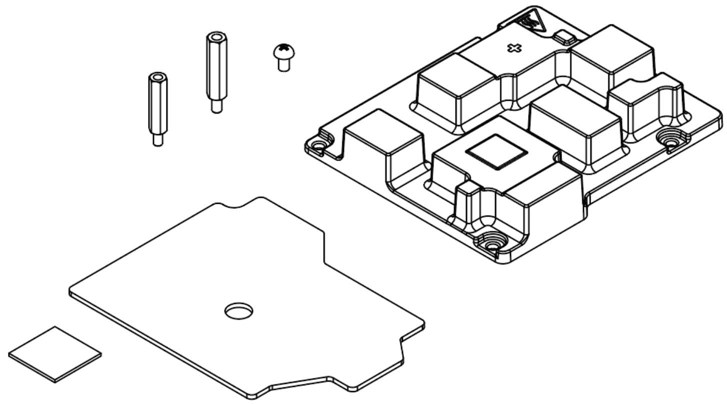


Figure 8: Thermal Kit (NI P/N 787331-01)

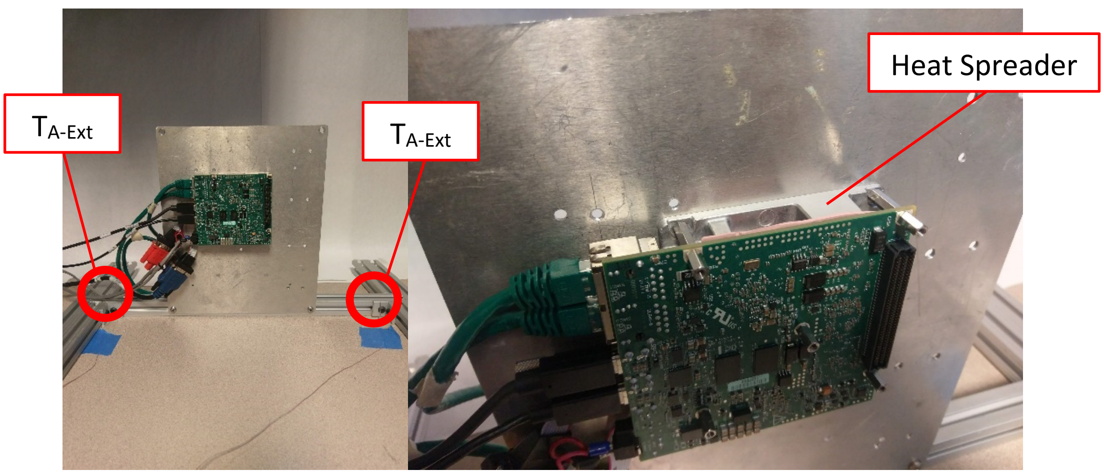


Figure 9: Configuration A – NI sbRIO-9608 with heat spreader in open air

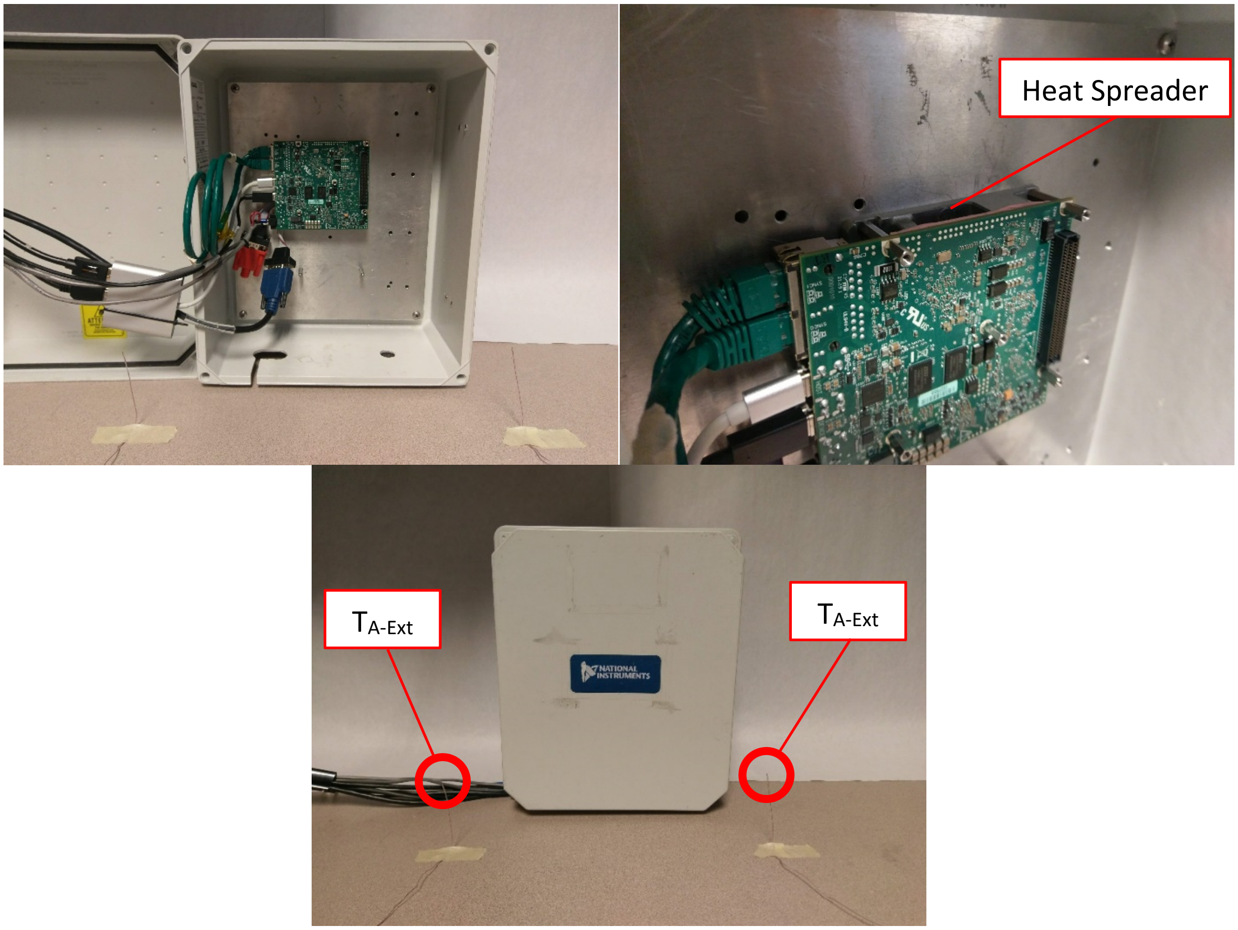


Figure 10: Configuration B – NI sbRIO-9608 with heat spreader in a large fiberglass enclosure

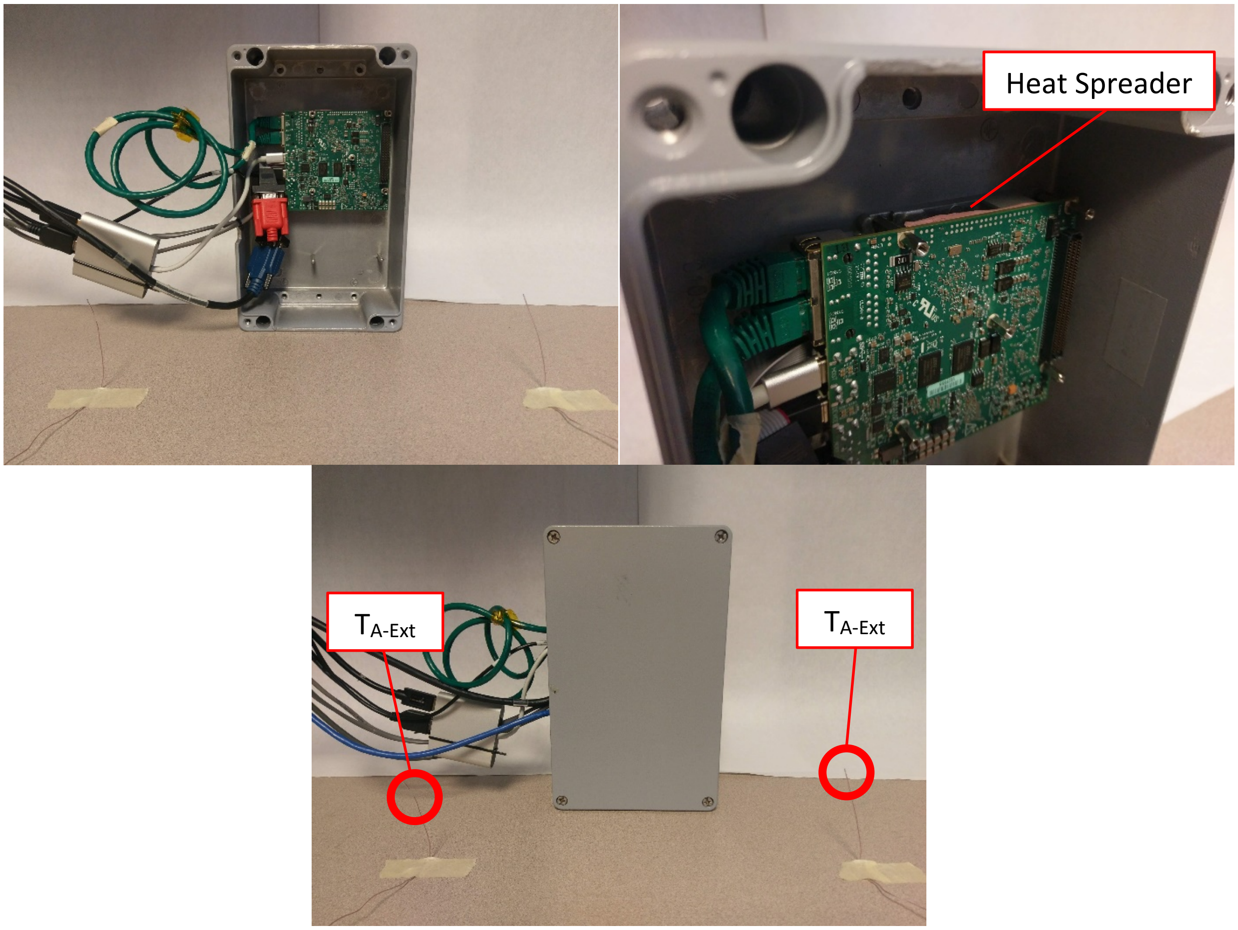


Figure 11: Configuration C – NI sbRIO-9608 with heat spreader in a small metal enclosure

5.4. *Results*

The following table shows the test results normalized to $T_{A\text{-}Ext}$=25°C. In addition, it includes the margin of the temperature reading compared to the maximum allowed values for each component or ambient measurement. In the "margin" column, the lowest margin component is highlighted.

Table 8: sbRIO-9608 component measurements and margin – open air vs. enclosure size with thermal solution

	A Open Air		B Large Fiberglass Encl.		C Small Metal Encl.	
Component	Measurement (°C)	Margin (°C)	Measurement (°C)	Margin (°C)	Measurement (°C)	Margin (°C)
$T_{SEN\text{-}CPU\text{-}0}$	40.1	67.9	47.6	60.4	38.9	69.1
$T_{SEN\text{-}CPU\text{-}1}$	43.1	64.9	50.6	57.4	41.3	66.7
$T_{SEN\text{-}FPGA}$	45.3	52.7	53.3	44.7	44.0	54.0
$T_{C\text{-}DDR\text{-}1}$	39.7	55.3	47.8	47.2	38.2	56.8
$T_{C\text{-}DDR\text{-}2}$	39.8	55.2	47.8	47.2	38.3	56.7
$T_{C\text{-}NAND}$	39.3	52.2	47.1	44.3	37.4	54.1
$T_{C\text{-}CPLD}$	39.9	54.1	47.8	46.1	38.7	55.3
$T_{C\text{-}USB}$	39.7	80.0	47.5	72.1	37.9	81.8
$T_{C\text{-}ENET\text{-}1}$	41.1	53.9	48.9	46.1	39.5	55.5

$T_{C\text{-}ENET\text{-}2}$	40.7	54.3	48.6	46.4	39.1	55.9
$T_{C\text{-}ASIC\text{-}1}$	40.9	79.0	48.8	71.1	39.6	80.3
$T_{C\text{-}ASIC\text{-}2}$	41.7	74.6	49.7	66.6	40.3	76.0
$T_{C\text{-}OSC}$	40.2	72.2	48.1	64.3	39.0	73.5
$T_{A\text{-}P\text{-}SEN}$	41.5	43.5	49.4	35.6	40.7	44.3
$T_{A\text{-}S\text{-}SEN}$	39.8	45.2	48.0	37.0	39.2	45.8
$T_{A\text{-}P\text{-}TL}$	39.7	45.3	47.6	37.4	39.0	46.0
$T_{A\text{-}P\text{-}TR}$	39.7	45.3	47.3	37.7	39.6	45.4
$T_{A\text{-}P\text{-}BL}$	38.1	46.9	45.2	39.8	40.4	44.6
$T_{A\text{-}P\text{-}BR}$	39.3	45.7	47.3	37.7	37.9	47.1
$T_{A\text{-}S\text{-}TL}$	38.0	47.0	45.2	39.8	40.1	44.9
$T_{A\text{-}S\text{-}TR}$	39.1	45.9	46.1	38.9	40.1	44.9
$T_{A\text{-}S\text{-}BL}$	36.5	48.5	43.9	41.1	39.7	45.3
$T_{A\text{-}S\text{-}BR}$	36.3	48.7	43.7	41.3	38.4	46.6
$T_{A\text{-}Ext}$	25.0	-	25.0	-	25.0	-

The measured system power draw of the NI sbRIO-9608 was approximately 12.9W for each configuration.

With the addition of a heat spreader, the die junction temperature of the CPU, FPGA, and case temperature of other critical ICs are greatly reduced. In all three configurations the digitally reported primary side local ambient is the lowest margin component.

Extrapolating to the maximum allowed temperature of the lowest margin measurements, the estimated maximum achievable external ambient for each configuration is shown in the following table.

Table 7: Maximum achievable ambient – open air vs. enclosure size with thermal solution

Configuration	**A** **(Open Air)**	**B** **(Large Fiberglass Enclosure)**	**C** **(Small Metal Enclosure)**
Max Achievable $T_{A\text{-}Ext}$ (°C)	68.5	60.6	69.3

6. Example 4 – NI sbRIO-9608, Open Air vs. Enclosure Size, With Thermal Solution and RMC

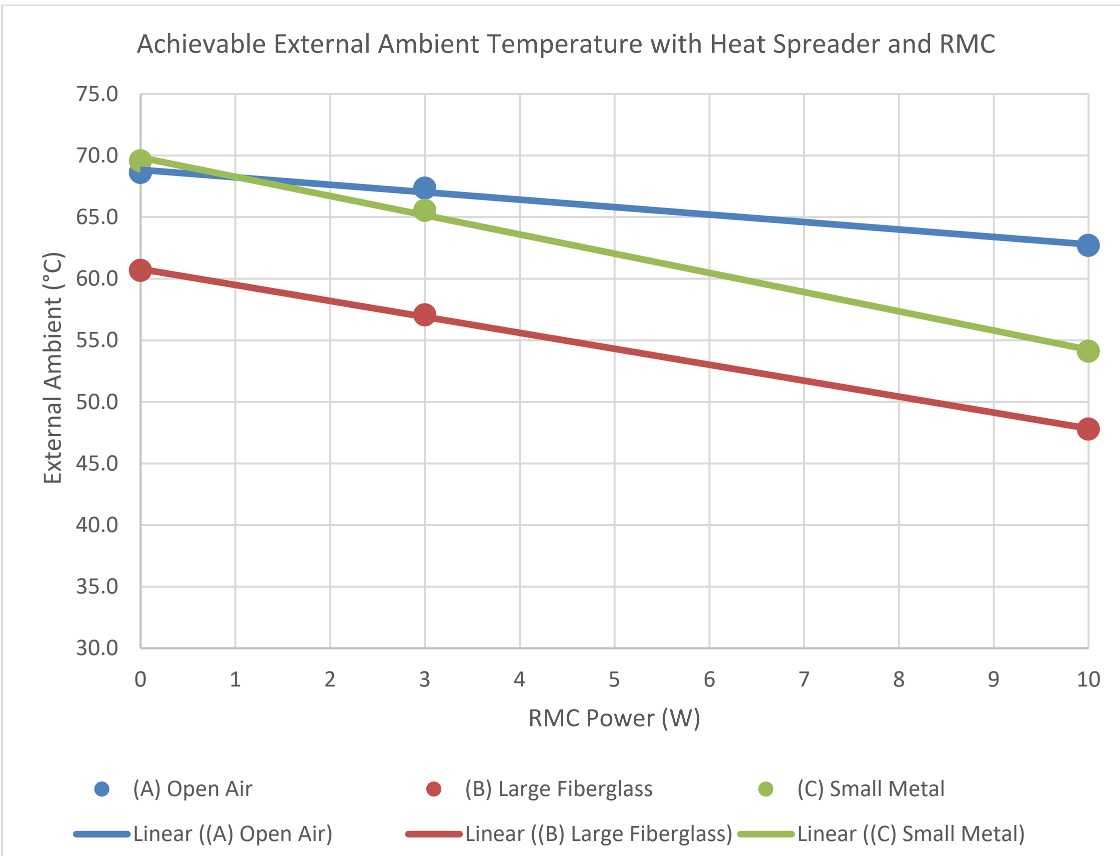
6.1. *Test Description*

In this example, the NI sbRIO-9608 was configured with a heat spreader and an RMC loaded at varying power levels to show the impact of adding an expansion card. The same open air and enclosure configurations from Example 3 were used. This Example does not exercise the LVDS features of the FPGA. See Example 5 for more information on the additional thermal impacts of using LVDS.

6.2. *Test Results Summary*

With the addition of a heat spreader, the impact of self-heating is greatly reduced compared to the tests in Example 2. The heat spreader greatly reduces the die junction temperature of the CPU, FPGA, and case temperature of other critical ICs, making the digitally reported primary side local ambient the lowest margin in all configurations when the RMC power is small, and one of the secondary side local ambient measurements the lowest margin measurement when the RMC power is high. Extrapolating to the maximum allowed temperature of the lowest margin component, the estimated maximum achievable external ambient for each configuration is shown in the following chart.

Chart 2: sbRIO-9608 achievable ambient vs. RMC power – open air vs. enclosure size with thermal solution and RMC



Compared to Example 2, configurations A and B result in approximately 23-29°C and 22-23°C increase in the achievable external ambient, respectively, by adding a thermal solution. Comparing configuration B from Example 2 to configuration C in this example there is approximately 29-32°C increase in the achievable external ambient by changing from a large fiberglass enclosure without a heat spreader to a small metal enclosure with a heat spreader, depending on the RMC power.

These configurations did not include a thermal solution on the RMC thermal load board. Adding a thermal solution to the RMC may result in additional improvements in the max achievable external ambient temperature.

6.3. *Test Setup*

In this example, the NI sbRIO-9608 was installed with a heat spreader (NI P/N 787331-01) and a resistor load RMC test board.

- The circuit cards were mounted such that the heat spreader on the NI sbRIO-9608 directly contacted the metal mounting surface.
- The RMC was mounted to the NI sbRIO-9608 using 9.65mm tall standoffs. No thermal solution was attached to the RMC load board.
- The same open air and enclosure configurations as in Example 3 were used.
- Tests were performed with the RMC load at 0W, 3W, and 10W. In the test results, the subscript number for each test configuration corresponds to the RMC power load used for that test. So, A_0 corresponds to the 0W RMC, A_{10} corresponds to the 10W RMC, and so on.
- (A) Open Air Configuration – The NI sbRIO-9608 with RMC was mounted to a metal panel and oriented vertically, as shown in the following images.
- (B) Large Fiberglass Enclosure – The NI sbRIO-9608 with RMC was mounted to a metal panel and installed into a large fiberglass enclosure. The enclosure was oriented such that the PCBs were vertical during testing, as shown in the following images.
- (C) Small Metal Enclosure – The NI sbRIO-9608 was mounted directly to the side wall of a small aluminum enclosure. The enclosure was oriented such that the PCBs were vertical during testing, as shown in the following images.

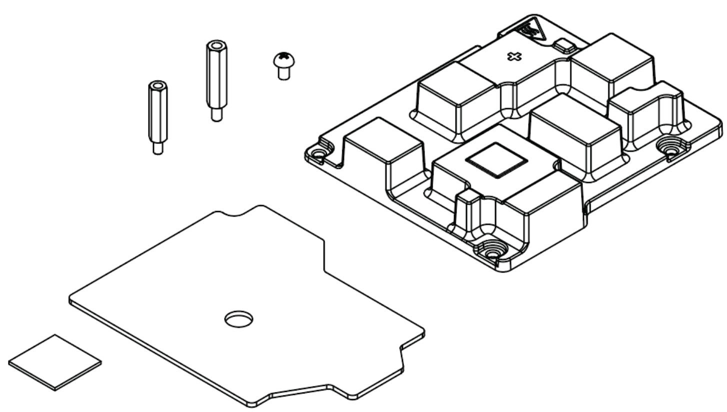


Figure 12: Thermal Kit (NI P/N 787331-01)

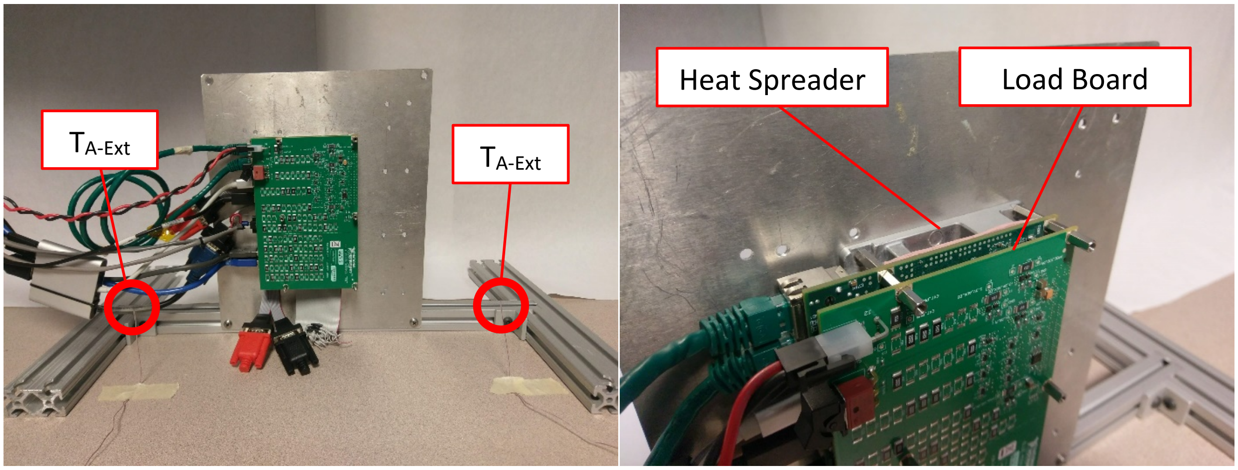


Figure 13: Configuration A – NI sbRIO-9608 with RMC load board and heat spreader in open air

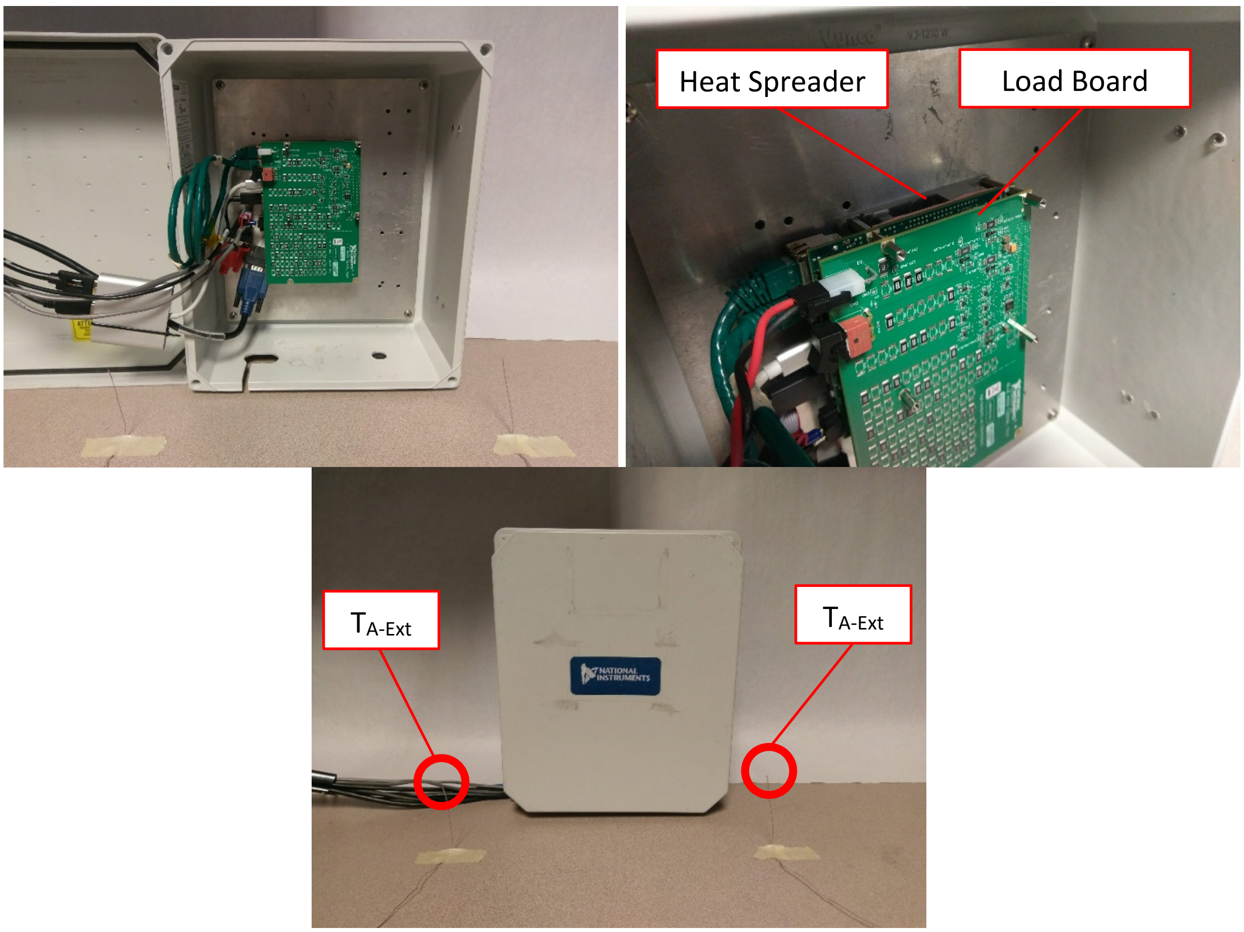


Figure 14: Configuration B – NI sbRIO-9608 with RMC load board and heat spreader in a large fiberglass enclosure

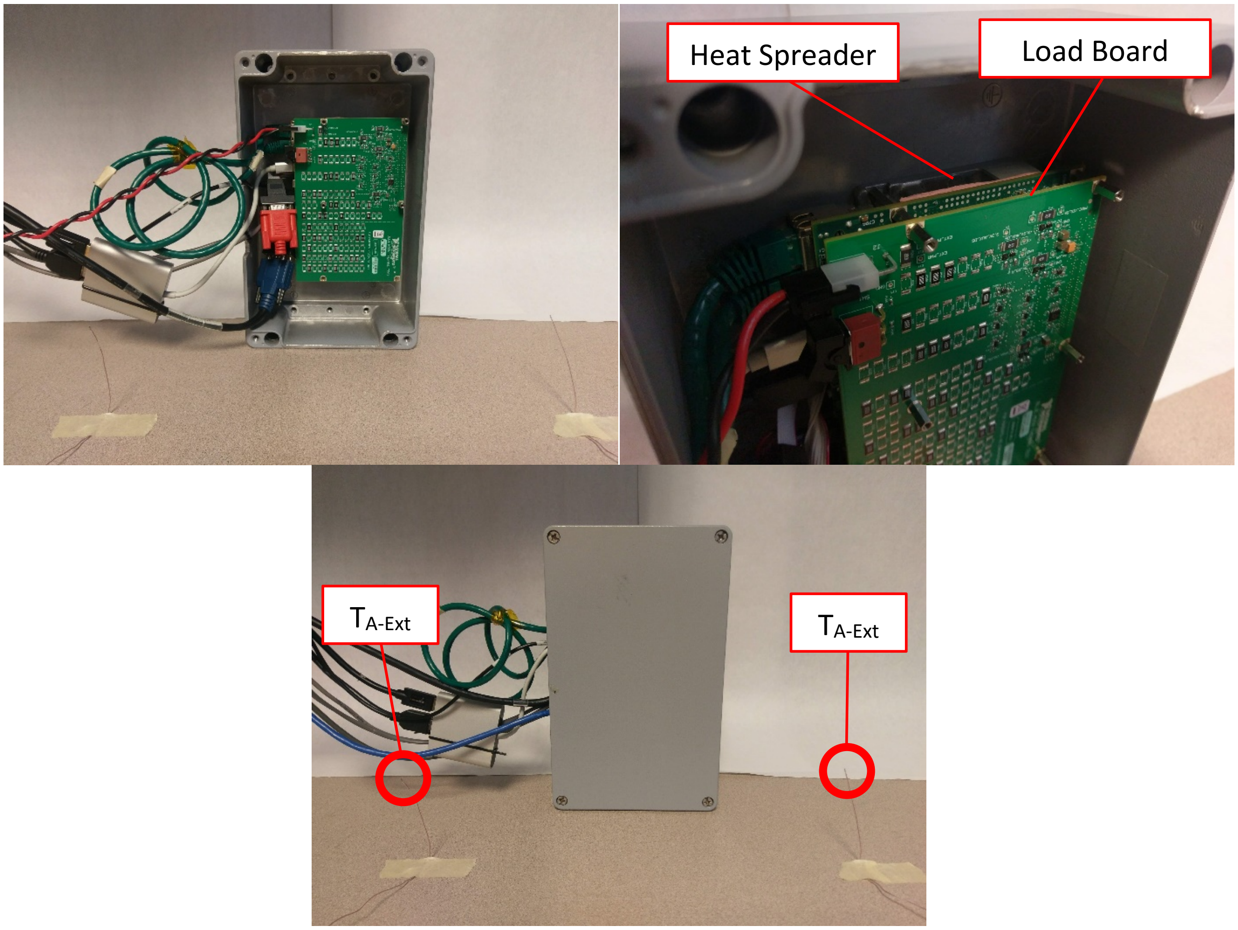


Figure 15: Configuration C – NI sbRIO-9608 with RMC load board and heat spreader in a small metal enclosure

6.4. *Results*

The following table shows the test results normalized to $T_{A\text{-}Ext}$=25°C. It includes the power draw measured by both the sbRIO board and the RMC test board, along with the margin of the temperature reading compared to the maximum allowed values for each component or ambient measurement. In the "margin" column, the lowest margin component is highlighted.

Table 9: sbRIO-9608 component measurements and margin – configuration A with thermal solution and RMC

Open Air with Heat Spreader and RMC						
Configuration	**A_0**		**A_3**		**A_{10}**	
NI sbRIO-9608 Power (W)	13.3		13.3		14.7	
RMC Power (W)	0		3		10	
Total System Power (W)	13.3		16.3		24.7	
Component	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**
$T_{SEN\text{-}CPU\text{-}0}$	40.2	67.8	40.7	67.3	44.3	63.7
$T_{SEN\text{-}CPU\text{-}1}$	42.9	65.1	44.0	64.0	46.7	61.3
$T_{SEN\text{-}FPGA}$	45.1	52.9	46.2	51.8	49.6	48.4

$T_{C\text{-}DDR\text{-}1}$	39.8	55.2	40.8	54.2	44.0	51.0
$T_{C\text{-}DDR\text{-}2}$	39.7	55.3	40.7	54.3	44.1	50.9
$T_{C\text{-}NAND}$	39.1	52.4	40.1	51.4	43.2	48.2
$T_{C\text{-}CPLD}$	39.8	54.1	40.8	53.2	44.3	49.6
$T_{C\text{-}USB}$	39.6	80.1	40.6	79.1	43.8	75.9
$T_{C\text{-}ENET\text{-}1}$	41.0	54.0	42.1	52.9	45.4	49.6
$T_{C\text{-}ENET\text{-}2}$	40.7	54.3	41.7	53.3	45.0	50.0
$T_{C\text{-}ASIC\text{-}1}$	40.7	79.2	41.7	78.2	45.0	74.9
$T_{C\text{-}ASIC\text{-}2}$	41.5	74.8	42.5	73.8	45.9	70.4
$T_{C\text{-}OSC}$	40.0	72.4	41.0	71.5	44.2	68.2
$T_{A\text{-}P\text{-}SEN}$	41.4	43.6	42.7	42.3	46.8	38.2
$T_{A\text{-}S\text{-}SEN}$	40.2	44.8	41.5	43.5	45.7	39.3
$T_{A\text{-}P\text{-}TL}$	39.3	45.7	40.4	44.6	43.8	41.2
$T_{A\text{-}P\text{-}TR}$	38.7	46.3	40.2	44.8	44.8	40.2
$T_{A\text{-}P\text{-}BL}$	37.9	47.1	39.1	45.9	43.1	41.9
$T_{A\text{-}P\text{-}BR}$	39.2	45.8	40.2	44.8	43.5	41.5
$T_{A\text{-}S\text{-}TL}$	37.5	47.5	38.8	46.2	42.6	42.4
$T_{A\text{-}S\text{-}TR}$	39.5	45.5	41.3	43.7	47.3	37.7
$T_{A\text{-}S\text{-}BL}$	36.3	48.7	38.1	46.9	42.6	42.4
$T_{A\text{-}S\text{-}BR}$	36.9	48.1	38.9	46.1	43.8	41.2
Key$T_{A\text{-}Ext}$	25.0	-	25.0	-	25.0	-

Table 10: sbRIO-9608 component measurements and margin – configuration B with thermal solution and RMC

Large Fiberglass Enclosure with Heat Spreader and RMC						
Configuration	**B_0**		**B_3**		**B_{10}**	
NI sbRIO-9608 Power (W)	12.3		13.1		14.4	
RMC Power (W)	0		3		10	
Total System Power (W)	12.3		16.1		24.4	
Component	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**
$T_{SEN\text{-}CPU\text{-}0}$	47.5	60.5	50.8	57.2	59.0	49.0
$T_{SEN\text{-}CPU\text{-}1}$	50.5	57.5	53.8	54.2	61.9	46.1
$T_{SEN\text{-}FPGA}$	53.2	44.8	56.5	41.5	64.8	33.2
$T_{C\text{-}DDR\text{-}1}$	47.9	47.1	51.2	43.8	59.2	35.8
$T_{C\text{-}DDR\text{-}2}$	47.9	47.1	51.2	43.8	59.3	35.7
$T_{C\text{-}NAND}$	47.1	44.3	50.4	41.1	58.3	33.2
$T_{C\text{-}CPLD}$	47.9	46.0	51.2	42.8	59.4	34.5
$T_{C\text{-}USB}$	47.6	72.0	51.0	68.7	58.9	60.8
$T_{C\text{-}ENET\text{-}1}$	49.1	45.9	52.5	42.5	60.7	34.3

$T_{C\text{-}ENET\text{-}2}$	48.8	46.2	52.2	42.8	60.3	34.7
$T_{C\text{-}ASIC\text{-}1}$	48.9	71.0	52.1	67.8	60.1	59.7
$T_{C\text{-}ASIC\text{-}2}$	49.6	66.8	52.9	63.4	60.9	55.4
$T_{C\text{-}OSC}$	48.1	64.3	51.3	61.1	59.2	53.2
$T_{A\text{-}P\text{-}SEN}$	49.3	35.7	52.9	32.1	61.8	23.2
$T_{A\text{-}S\text{-}SEN}$	48.2	36.8	51.8	33.2	60.9	24.1
$T_{A\text{-}P\text{-}TL}$	47.3	37.7	50.6	34.4	58.7	26.3
$T_{A\text{-}P\text{-}TR}$	46.4	38.6	50.1	34.9	59.2	25.8
$T_{A\text{-}P\text{-}BL}$	45.7	39.3	49.3	35.7	58.6	26.4
$T_{A\text{-}P\text{-}BR}$	47.4	37.6	50.7	34.3	58.6	26.4
$T_{A\text{-}S\text{-}TL}$	45.3	39.7	48.9	36.1	57.6	27.4
$T_{A\text{-}S\text{-}TR}$	47.0	38.0	51.3	33.7	62.2	22.8
$T_{A\text{-}S\text{-}BL}$	44.1	40.9	48.5	36.5	58.3	26.7
$T_{A\text{-}S\text{-}BR}$	44.9	40.1	49.7	35.3	60.0	25.0
$T_{A\text{-}Ext}$	25.0	-	25.0	-	25.0	-

Table 11: sbRIO-9608 component measurements and margin – configuration C with thermal solution and RMC

Small Metal Enclosure with Heat Spreader and RMC						
Configuration	C_0		C_3		C_{10}	
NI sbRIO-9608 Power (W)	13.4		12.3		14.5	
RMC Power (W)	0		3		10	
Total System Power (W)	13.4		15.3		24.5	
Component	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**
$T_{SEN\text{-}CPU\text{-}0}$	38.8	69.2	40.7	67.3	46.7	61.3
$T_{SEN\text{-}CPU\text{-}1}$	40.9	67.1	42.9	65.1	49.7	58.3
$T_{SEN\text{-}FPGA}$	43.7	54.3	46.0	52.0	53.0	45.0
$T_{C\text{-}DDR\text{-}1}$	38.1	56.9	40.1	54.9	46.8	48.2
$T_{C\text{-}DDR\text{-}2}$	38.2	56.8	40.2	54.8	47.0	48.0
$T_{C\text{-}NAND}$	37.2	54.3	39.2	52.3	45.7	45.8
$T_{C\text{-}CPLD}$	38.5	55.5	40.6	53.3	47.7	46.3
$T_{C\text{-}USB}$	37.7	82.0	39.7	79.9	46.3	73.4
$T_{C\text{-}ENET\text{-}1}$	39.4	55.6	41.6	53.4	48.5	46.5
$T_{C\text{-}ENET\text{-}2}$	39.0	56.0	41.2	53.8	48.0	47.0
$T_{C\text{-}ASIC\text{-}1}$	39.4	80.5	41.5	78.4	48.4	71.5
$T_{C\text{-}ASIC\text{-}2}$	40.1	76.2	42.2	74.1	49.1	67.2
$T_{C\text{-}OSC}$	38.7	73.7	40.8	71.6	47.5	64.9
$T_{A\text{-}P\text{-}SEN}$	40.4	44.6	43.0	42.0	51.0	34.0
$T_{A\text{-}S\text{-}SEN}$	39.1	45.9	41.8	43.2	50.0	35.0

$T_{A\text{-}P\text{-}TL}$	38.7	46.3	41.0	44.0	48.2	36.8
$T_{A\text{-}P\text{-}TR}$	39.1	45.9	41.9	43.1	50.6	34.4
$T_{A\text{-}P\text{-}BL}$	40.3	44.7	43.6	41.4	53.5	31.5
$T_{A\text{-}P\text{-}BR}$	37.7	47.3	39.8	45.2	46.6	38.4
$T_{A\text{-}S\text{-}TL}$	40.1	44.9	43.7	41.3	54.1	30.9
$T_{A\text{-}S\text{-}TR}$	40.1	44.9	43.4	41.6	54.1	30.9
$T_{A\text{-}S\text{-}BL}$	39.6	45.4	44.5	40.5	55.9	29.1
$T_{A\text{-}S\text{-}BR}$	38.7	46.3	43.2	41.8	54.7	30.3
$T_{A\text{-}Ext}$	25.0	-	25.0	-	25.0	-

The measured power draw of the NI sbRIO-9608 increases slightly as the RMC power increases due to the added load on the power supply. With a 10W RMC, this results in approximately 1.5W additional power being dissipated on the sbRIO board.

The heat spreader greatly reduces the die junction temperature of the CPU, FPGA, and the case temperature of other critical ICs, making the local board ambient temperatures generally the lowest margin components.

With the heat spreader present, the metal enclosure is even able to outperform an open air case, but only when the total system power is low. At a total system power of 14-15W, the self-heating within the metal enclosure outpaces the increased conduction and/or natural-convection effectiveness of the metal enclosure and the open air configuration becomes the cooler configuration.

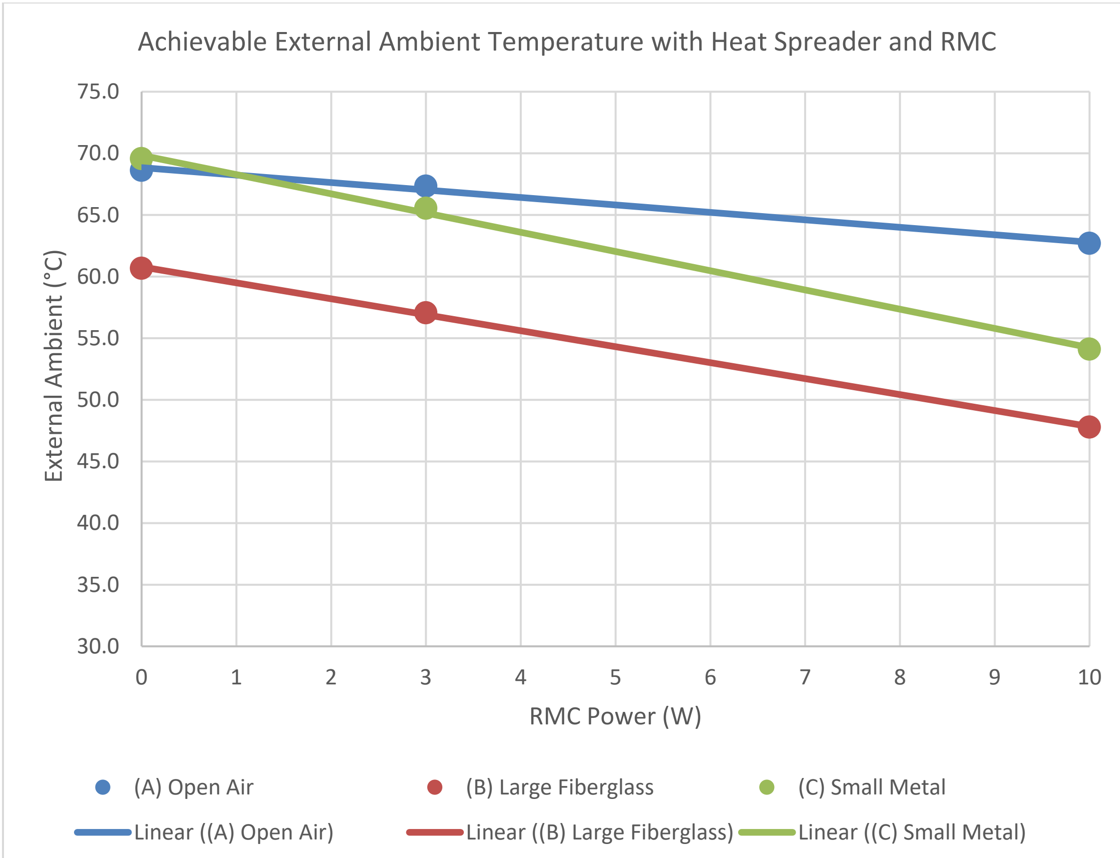
Using this data, the maximum achievable external ambient for each configuration is estimated, as shown in the following table.

Table 12: Maximum achievable ambient – open air vs. enclosure size with thermal solution and RMC

RMC Power (W)	Max Achievable $T_{A\text{-}Ext}$ (°C)		
	A	B	C
0.0	68.6	60.7	69.6
3.0	67.3	57.1	65.5
10.0	62.7	47.8	54.1

The following chart plots the achievable external ambient compared with RMC power levels for each configuration. The results may be approximated with a linear extrapolation to estimate the ambient at different RMC power levels within the different enclosures.

Chart 2: sbRIO-9608 achievable ambient vs. RMC power – open air vs. enclosure size with thermal solution and RMC


Achievable External Ambient Temperature with Heat Spreader and RMC
External Ambient (°C)
75.0
70.0
65.0
60.0
55.0
50.0
45.0
40.0
35.0
30.0
0
1
2
3
4
5
6
7
8
9
10
RMC Power (W)
(A) Open Air
(B) Large Fiberglass
(C) Small Metal
Linear ((A) Open Air)
Linear ((B) Large Fiberglass)
Linear ((C) Small Metal)

7. Example 5 – NI sbRIO-9608, LVDS Output Impact

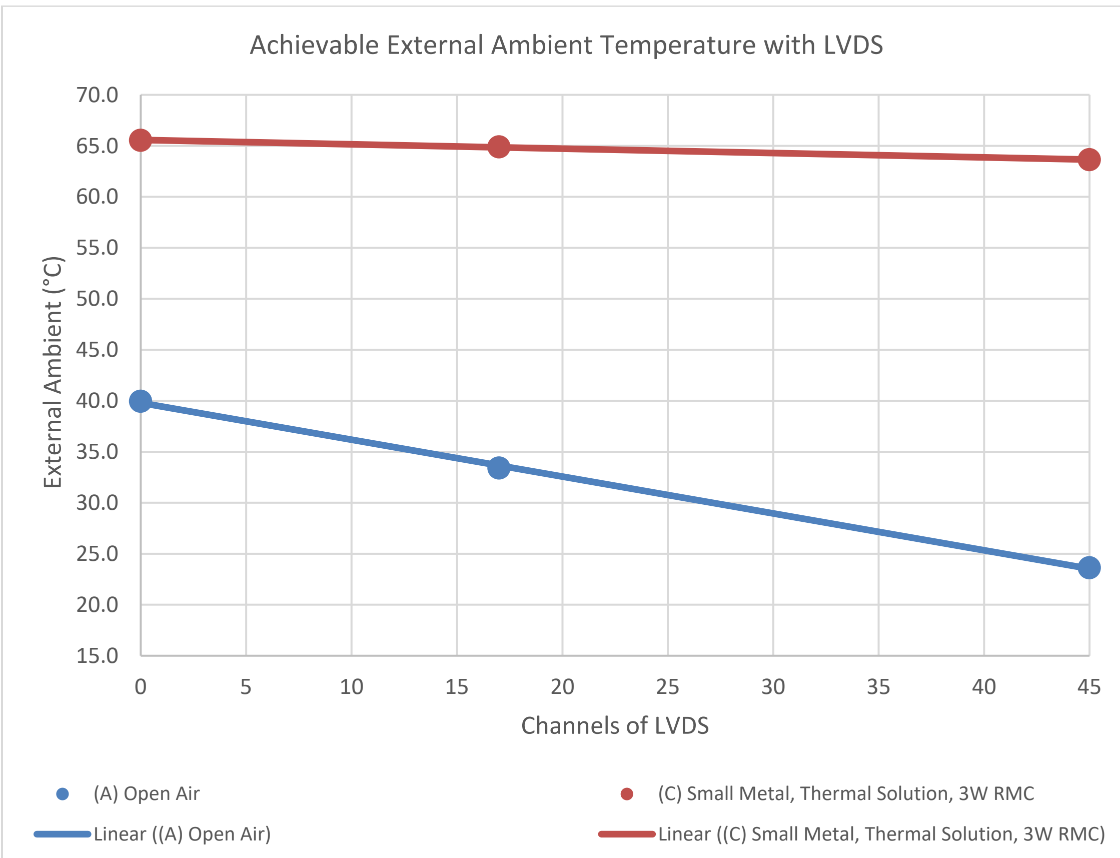
7.1. *Test Description*

The power dissipation of the FPGA is drastically increased when utilizing LVDS outputs. In this example, the NI sbRIO-9608 was configured in the same manner as configuration A from Example 1 and configuration C from Example 4. Configuration A did not include a thermal solution or RMC load, while configuration C included both a thermal solution and the RMC load powered at 3W. For each configuration the power consumption of the FPGA was adjusted to simulate varying channel counts of LVDS output in order to explore the impact of LVDS output on achievable external ambient.

7.2. *Test Results Summary*

The presence of the heat spreader greatly reduces the impact LVDS output has on the achievable external ambient. The lowest margin component in configuration A at all levels of LVDS utilization is the FPGA. For configuration C the lowest margin component remains one of the local ambient measurements regardless of the LVDS utilization. Extrapolating to the maximum allowed local ambient temperature of the lowest margin component, the estimated maximum achievable external ambient for each configuration is shown in the following chart.

Chart 3: sbRIO-9608 achievable ambient vs. LVDS output



Compared to Example 1, adding 45 channels of LVDS output to an sbRIO operating in open air (configuration A) results in approximately a 16°C reduction in achievable external ambient. Compared to Example 4, adding 45 channels of LVDS output to an sbRIO operating in a small metal enclosure with a thermal solution (configuration C) and 3W of RMC power results in approximately a 2°C reduction in the achievable external ambient.

7.3. *Test Setup*

In this example, the NI sbRIO-9608 was installed with a heat spreader (NI P/N 787331-01) and a resistor load RMC test board for configuration C only.

- The circuit cards were mounted such that the heat spreader on the NI sbRIO-9608 directly contacted the metal mounting surface.
- The RMC was mounted to the NI sbRIO-9608 using 9.65mm tall standoffs. No thermal solution was attached to the RMC load board.
- The same open air and small metal enclosure configurations as in Example 1 and D, respectively, were used.
- Tests were performed with the RMC load at 3W for configuration C only.
- Power consumption of the FPGA was adjusted to represent max achievable load assuming either 0, 17, or 45 channels of LVDS. In the test results, the subscript number for each test configuration corresponds to the channel count used for that test. So, A_0 corresponds to 0 channels of LVDS, A_{45} corresponds to the 45 channels of LVDS, and so on.
- (A) Open Air Configuration – The NI sbRIO-9608 with no thermal solution or RMC was mounted to a metal panel and oriented vertically, as shown in the following images.
- (C) Small Metal Enclosure – The NI sbRIO-9608 was mounted directly to the side wall of a small aluminum enclosure, along with the heat spreader and RMC. The enclosure was oriented such that the PCBs were vertical during testing, as shown in the following images.

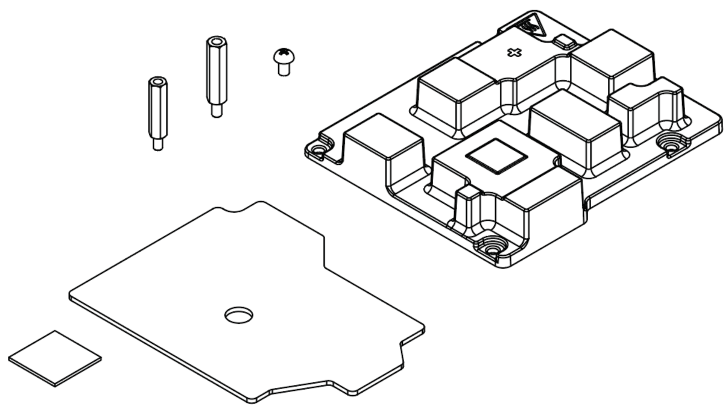


Figure 16: Thermal Kit (NI P/N 787331-01)

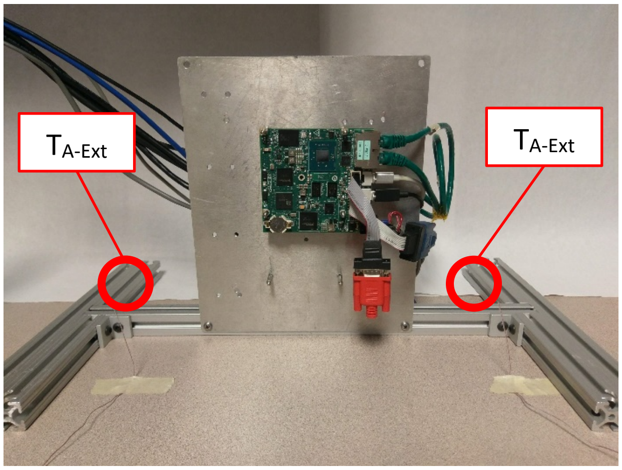


Figure 17: Configuration A – NI sbRIO-9608 in open air

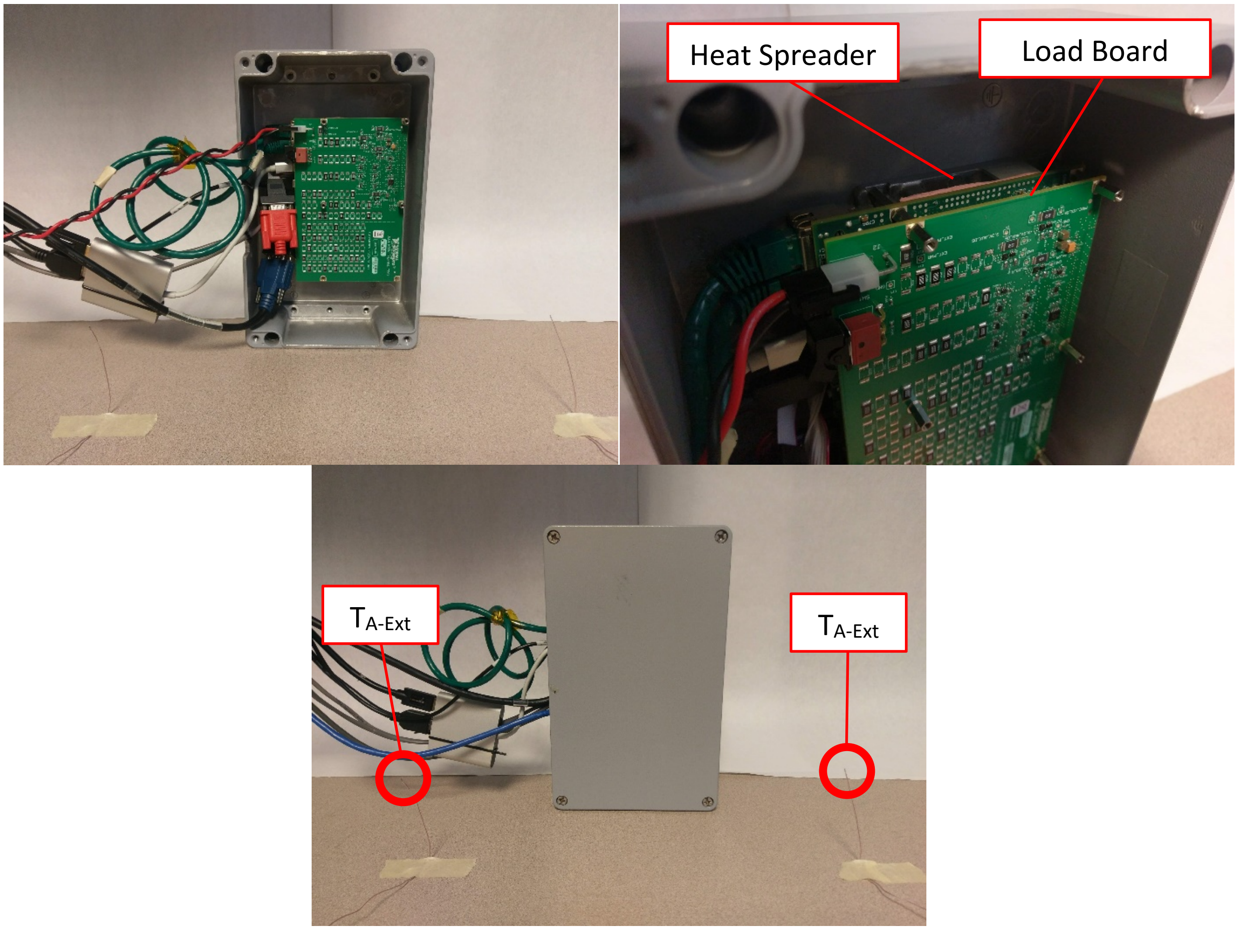


Figure 18: Configuration C – NI sbRIO-9608 with RMC load board and heat spreader in a small metal enclosure

7.4. Results

The following table shows the test results normalized to $T_{A\text{-}Ext}$=25°C. It includes the power draw measured, along with the margin of the temperature reading compared to the maximum allowed values for each component or ambient measurement. In the "margin" column, the lowest margin component is highlighted.

Table 13: sbRIO-9608 component measurements and margin – configuration A with LVDS output

Open Air with LVDS						
Configuration	A_0		A_{17}		A_{45}	
NI sbRIO-9608 Power (W)	12.5		13.3		14.6	
Component	Measurement (°C)	Margin (°C)	Measurement (°C)	Margin (°C)	Measurement (°C)	Margin (°C)
$T_{SEN\text{-}CPU\text{-}0}$	68.4	39.6	71.2	36.8	73.7	34.3
$T_{SEN\text{-}CPU\text{-}1}$	71.3	36.7	73.5	34.5	76.8	31.2
$T_{SEN\text{-}FPGA}$	83.1	14.9	89.6	8.4	99.4	-1.4
$T_{C\text{-}DDR\text{-}1}$	66.2	28.8	69.1	25.9	73.3	21.7
$T_{C\text{-}DDR\text{-}2}$	62.6	32.4	64.8	30.2	68.0	27.0
$T_{C\text{-}NAND}$	61.9	29.6	64.1	27.4	67.2	24.3

$T_{C\text{-}CPLD}$	62.8	31.1	65.2	28.7	68.5	25.4
$T_{C\text{-}USB}$	61.3	58.3	63.1	56.6	65.4	54.2
$T_{C\text{-}ENET\text{-}1}$	63.2	31.8	65.0	30.0	67.4	27.6
$T_{C\text{-}ENET\text{-}2}$	62.0	33.0	63.7	31.3	66.1	28.9
$T_{C\text{-}ASIC\text{-}1}$	68.0	51.9	71.1	48.8	75.3	44.6
$T_{C\text{-}ASIC\text{-}2}$	73.0	43.3	76.3	40.0	81.1	35.2
$T_{C\text{-}OSC}$	68.3	44.1	72.0	40.4	77.4	35.0
$T_{A\text{-}P\text{-}SEN}$	67.4	17.6	70.4	14.6	74.9	10.1
$T_{A\text{-}S\text{-}SEN}$	65.0	20.0	67.9	17.1	72.1	12.9
$T_{A\text{-}P\text{-}TL}$	55.2	29.8	56.7	28.3	60.6	24.4
$T_{A\text{-}P\text{-}TR}$	51.4	33.6	52.5	32.5	55.4	29.6
$T_{A\text{-}P\text{-}BL}$	50.2	34.8	51.7	33.3	53.5	31.5
$T_{A\text{-}P\text{-}BR}$	50.8	34.2	52.8	32.2	54.7	30.3
$T_{A\text{-}S\text{-}TL}$	54.0	31.0	56.7	28.3	60.1	24.9
$T_{A\text{-}S\text{-}TR}$	57.9	27.1	60.2	24.8	63.1	21.9
$T_{A\text{-}S\text{-}BL}$	45.9	39.1	46.5	38.5	47.8	37.2
$T_{A\text{-}S\text{-}BR}$	49.5	35.5	50.4	34.6	52.1	32.9
$T_{A\text{-}Ext}$	25.0	-	25.0	-	25.0	-

Table 14: sbRIO-9608 component measurements and margin – configuration C with thermal solution, RMC, and LVDS output

Small Metal Enclosure with Heat Spreader, RMC, and LVDS						
Configuration	**C_0**		**C_{17}**		**C_{45}**	
NI sbRIO-9608 Power (W)	12.3		13.0		14.8	
RMC Power (W)	3.0		3.0		3.0	
Total System Power (W)	15.3		16.0		17.8	
Component	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**	**Measurement (°C)**	**Margin (°C)**
$T_{SEN\text{-}CPU\text{-}0}$	40.7	67.3	41.4	66.6	42.4	65.6
$T_{SEN\text{-}CPU\text{-}1}$	42.9	65.1	43.8	64.2	45.4	62.6
$T_{SEN\text{-}FPGA}$	46.0	52.0	47.6	50.4	50.4	47.6
$T_{C\text{-}DDR\text{-}1}$	40.1	54.9	40.9	54.1	42.3	52.7
$T_{C\text{-}DDR\text{-}2}$	40.2	54.8	41.0	54.0	42.3	52.7
$T_{C\text{-}NAND}$	39.2	52.3	39.9	51.6	41.1	50.4
$T_{C\text{-}CPLD}$	40.6	53.3	41.4	52.6	42.7	51.2
$T_{C\text{-}USB}$	39.7	79.9	40.4	79.2	41.6	78.1
$T_{C\text{-}ENET\text{-}1}$	41.6	53.4	42.3	52.7	43.5	51.5
$T_{C\text{-}ENET\text{-}2}$	41.2	53.8	41.9	53.1	43.1	51.9
$T_{C\text{-}ASIC\text{-}1}$	41.5	78.4	42.4	77.5	43.8	76.1
$T_{C\text{-}ASIC\text{-}2}$	42.2	74.1	43.1	73.2	44.6	71.8

$T_{C\text{-}OSC}$	40.8	71.6	41.7	70.7	43.3	69.1
$T_{A\text{-}P\text{-}SEN}$	43.0	42.0	43.9	41.1	45.5	39.5
$T_{A\text{-}S\text{-}SEN}$	41.8	43.2	42.7	42.3	44.4	40.6
$T_{A\text{-}P\text{-}TL}$	41.0	44.0	42.0	43.0	43.7	41.3
$T_{A\text{-}P\text{-}TR}$	41.9	43.1	42.7	42.3	44.1	40.9
$T_{A\text{-}P\text{-}BL}$	43.6	41.4	44.4	40.6	45.7	39.3
$T_{A\text{-}P\text{-}BR}$	39.8	45.2	40.5	44.5	41.7	43.3
$T_{A\text{-}S\text{-}TL}$	43.7	41.3	44.7	40.3	46.4	38.6
$T_{A\text{-}S\text{-}TR}$	43.4	41.6	44.2	40.8	45.6	39.4
$T_{A\text{-}S\text{-}BL}$	44.5	40.5	45.1	39.9	46.3	38.7
$T_{A\text{-}S\text{-}BR}$	43.2	41.8	43.9	41.1	45.0	40.0
$T_{A\text{-}Ext}$	25.0	-	25.0	-	25.0	-

The measured power draw of the NI sbRIO-9608 increases slightly as the LVDS output channel count increases due to the added load on the FPGA. With 45 channels of LVDS output, this results in roughly 2.3W additional power being dissipated on the sbRIO board.

The heat spreader greatly reduces the impact of the LVDS output load. In configuration C the local board ambients remained the lowest margin measurements despite the added load to the FPGA. While the introduction of LVDS output to configuration A, which lacks a thermal solution, causes the FPGA to rapidly reduce the achievable external ambient as channel count rises.

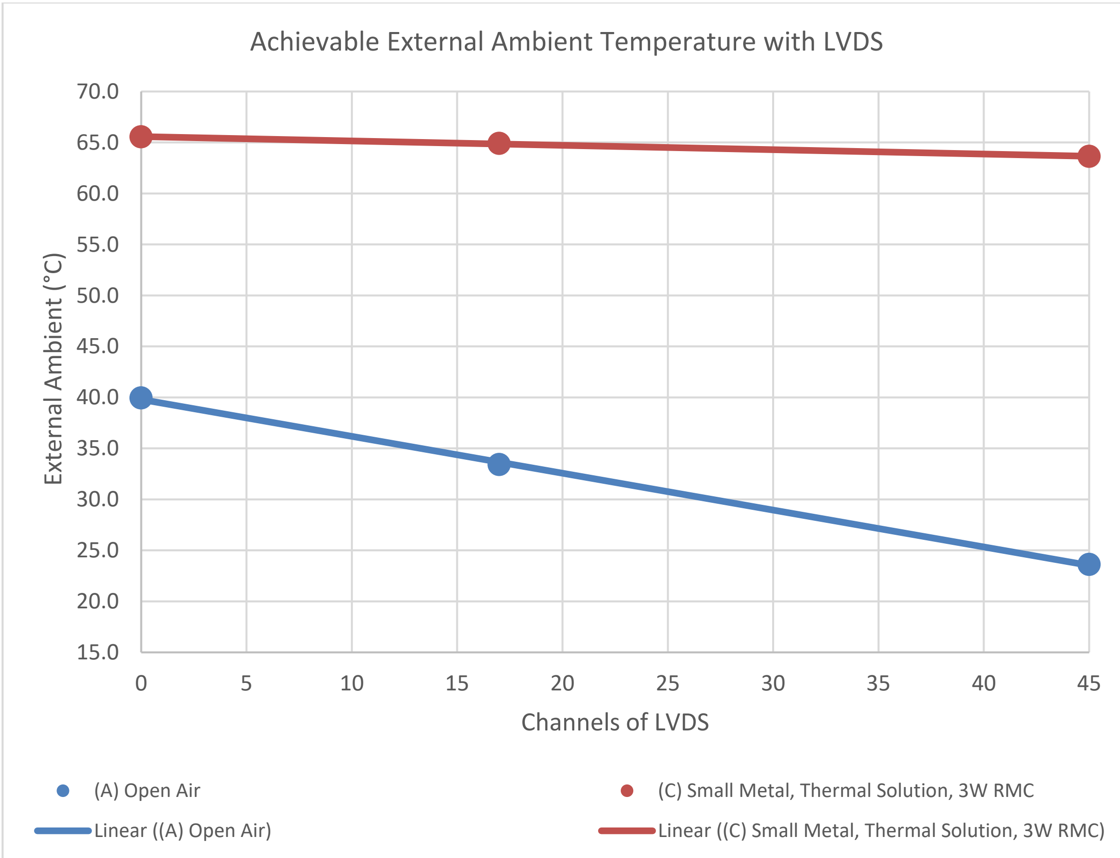
Using this data, the maximum achievable external ambient for each configuration is estimated, as shown in the following table.

Table 15: Maximum achievable ambient – with LVDS output

LVDS Channel Count	Max Achievable $T_{A\text{-}Ext}$ (°C)	
	A	C
0	39.9	65.5
17	33.4	64.9
45	23.6	63.6

The following chart plots the achievable external ambient compared with the LVDS output channel count for each configuration. The results may be approximated with a linear extrapolation to estimate the ambient at different LVDS output channel counts within the different configurations.

Chart 3: sbRIO-9608 achievable ambient vs. LVDS output


Achievable External Ambient Temperature with LVDS
70.0
65.0
60.0
55.0
50.0
45.0
40.0
35.0
30.0
25.0
20.0
15.0
External Ambient (°C)
0
5
10
15
20
25
30
35
40
45
Channels of LVDS
(A) Open Air
(C) Small Metal, Thermal Solution, 3W RMC
Linear ((A) Open Air)
Linear ((C) Small Metal, Thermal Solution, 3W RMC)